



ELECTRONICS II PROJECT *Phase1*

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Analysis of a Differential Amplifier Using MOSFETs

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Spring 2025

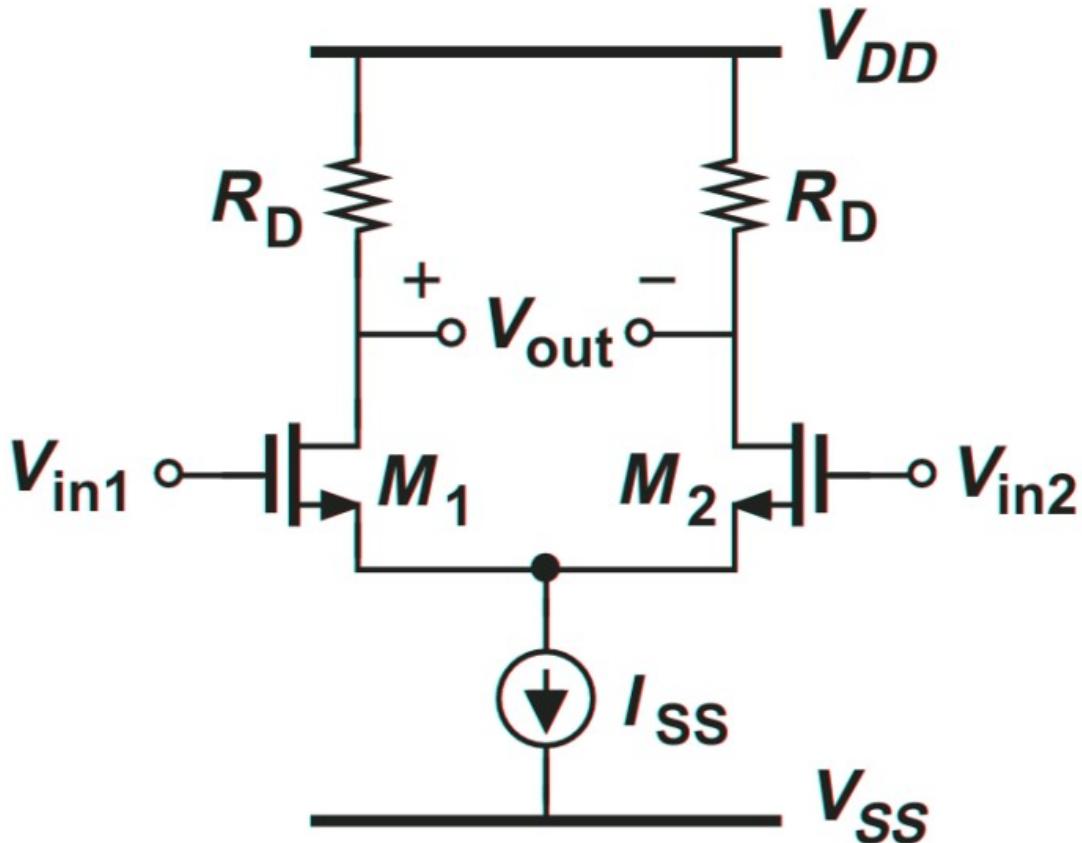
Introduction

In this project, the design and analysis of a differential amplifier using MOSFET transistors have been carried out. The objective is to evaluate the circuit's performance through theoretical analysis and simulation.

1 Section One: Initial Design

In this section, a basic differential amplifier structure has been designed. The circuit specifications are as follows:

- $V_{th} = 0.6V$
- $\mu_n C_{ox} = 250 \mu A/V^2$
- $\mu_p C_{ox} = 80 \mu A/V^2$
- $\lambda = 0.05V^{-1}$
- $V_{DD} = 1V, V_{SS} = -1V, I_{SS} = 1mA$



DC analysis and calculations of gain, input, and output resistance have been performed.

Questions:

- Determine the value of R_D such that the differential gain is maximized under saturation conditions.

we know that $V_{GS} - V_{th} \leq V_{DS}$ to ensure of saturation so we write it down as:

$$V_D = 1^v - \frac{R_D}{2} \rightarrow V_{DS} = V_D - V_S = V_G - V_S - V_{th}$$

$$\rightarrow V_D = -V_{th} \rightarrow R_D = 3.2^{k\Omega}$$

- Given $V_{CSmin} = 0.2V$, ensure that the voltage at the source of the differential pair is exactly the same on both sides.

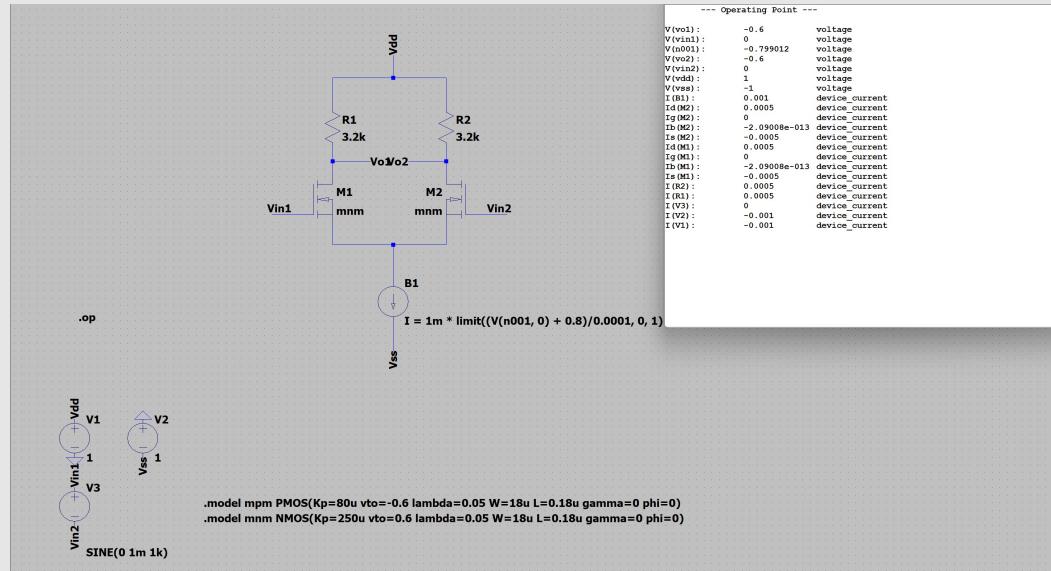
$$0.5^{mA} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2$$

$$1 = \frac{1}{4} \frac{W}{L} (0.8 - 0.6)^2 \leftrightarrow \frac{W}{L} = 100$$

- Perform a DC analysis of the circuit.

$$R_D = 3.2^{k\Omega} \rightarrow v_D = -0.6^v \rightarrow V_{DS} = 0.2^v, I_D = 0.5^{mA}$$

$$g_m = \frac{2 \times 0.5}{0.2} = 5^{m\Omega}, r_o = \frac{1}{0.05 \times 0.5} = 40^{k\Omega}$$



- Calculate the common-mode gain and differential gain of the circuit.

Common Mode with assuming $R_{SS} = 100^{k\Omega}$:

$$A_v = -\frac{R_D || r_o}{\frac{1}{g_m} + 2.R_{SS}} = -\frac{2.963}{0.2 + 200} = -0.015$$

Differential Mode :

$$A_v = -\frac{R_D || r_o}{\frac{1}{g_m}} = -\frac{2.963}{0.2} = -14.815$$

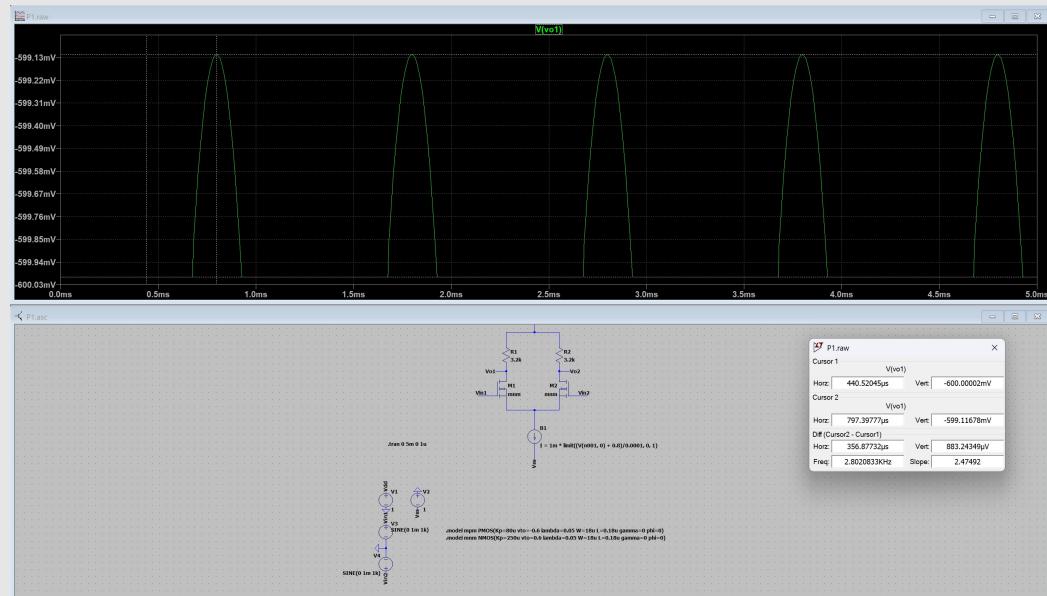


Figure 1: CM Mode

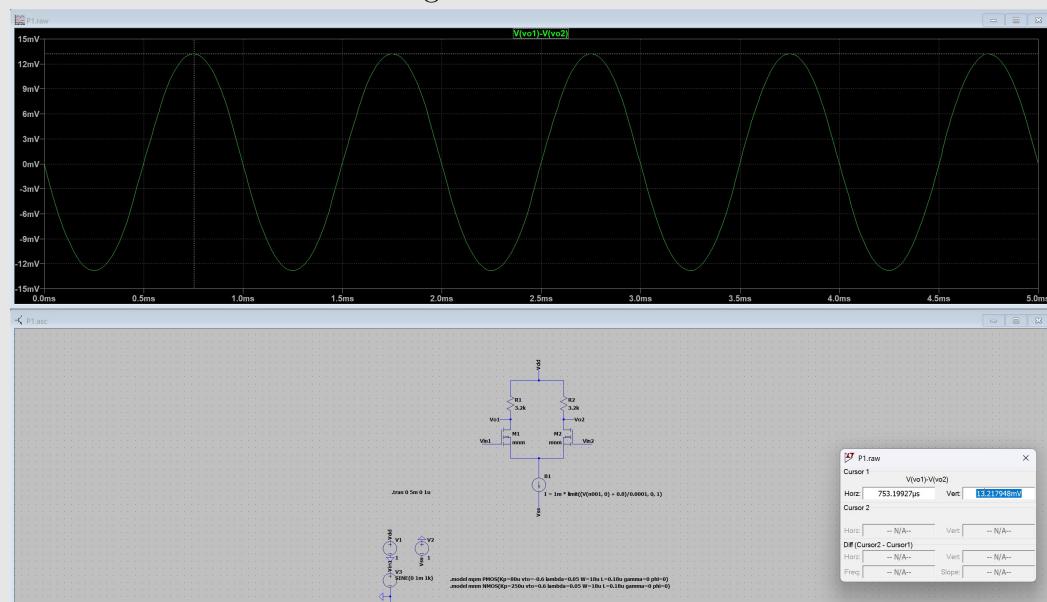


Figure 2: Diff Mode

5. Determine the input and output resistance of the circuit.

$$R_{in} = \infty$$

$$R_{out} = r_o || R_D$$

$$((1 + g_m R_s) + R_s = 40) || 3.2$$

$$R_{out} = 2.963^{k\Omega} \rightarrow \times 2 = 5.926^{k\Omega}$$

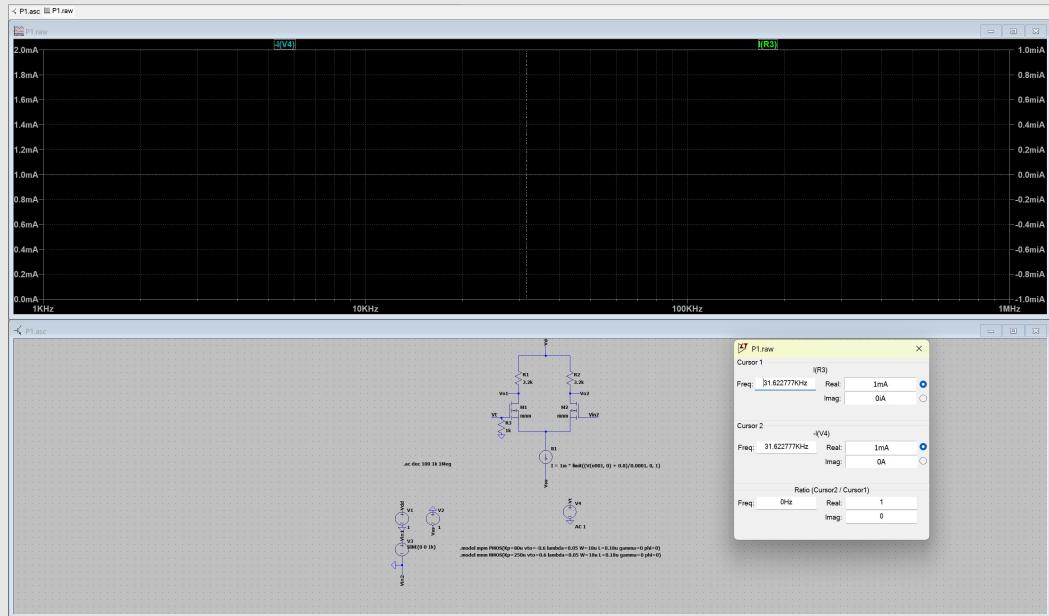


Figure 3: R_{in}

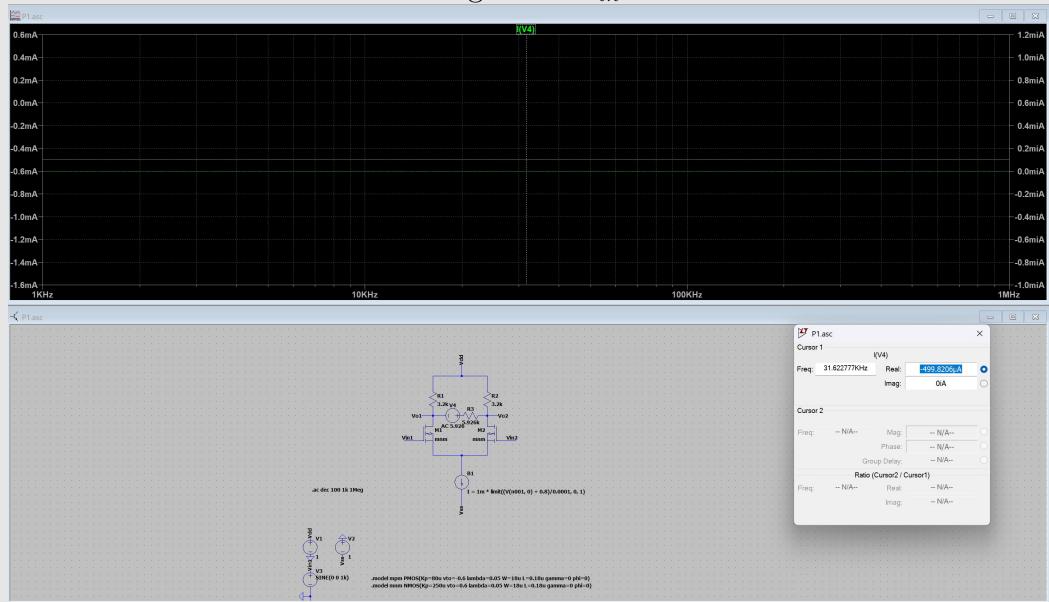


Figure 4: R_{out}

For R_{out} :

$$\frac{500\mu}{1m} = \frac{R_{out}}{R_{out} + 5.926k} \rightarrow R_{out1} = 5.926^{k\Omega}$$

6. Compute the peak-to-peak output swing.

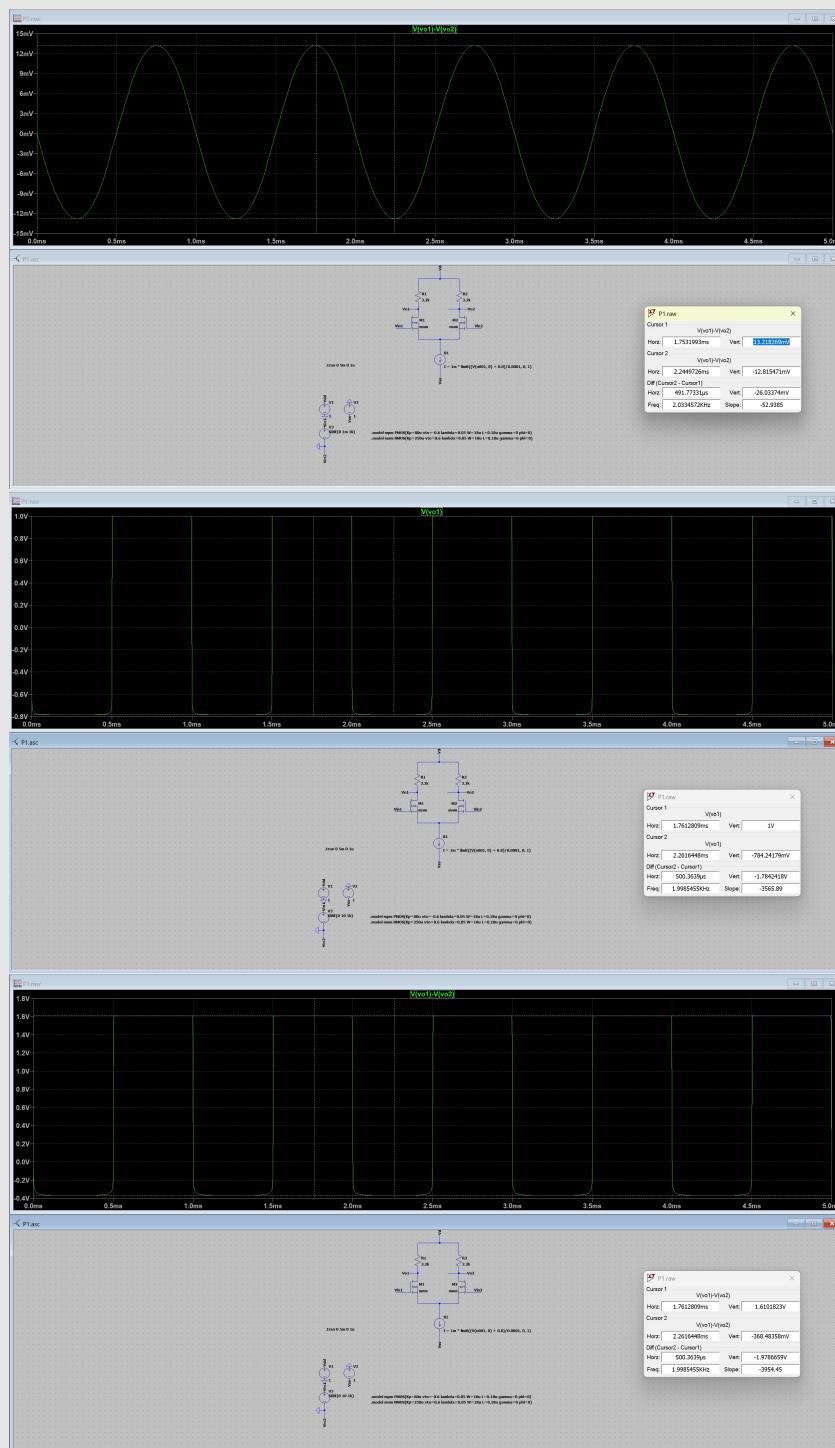
max Voltage $\rightarrow 1^v$

min Voltage $\rightarrow V_S + V_{DS_{min}} = V_S + V_{GS} - V_{th} = -0.8 + 0.2 = -0.6^v$

V_D is -0.6^v

so the p-p swing is zero.

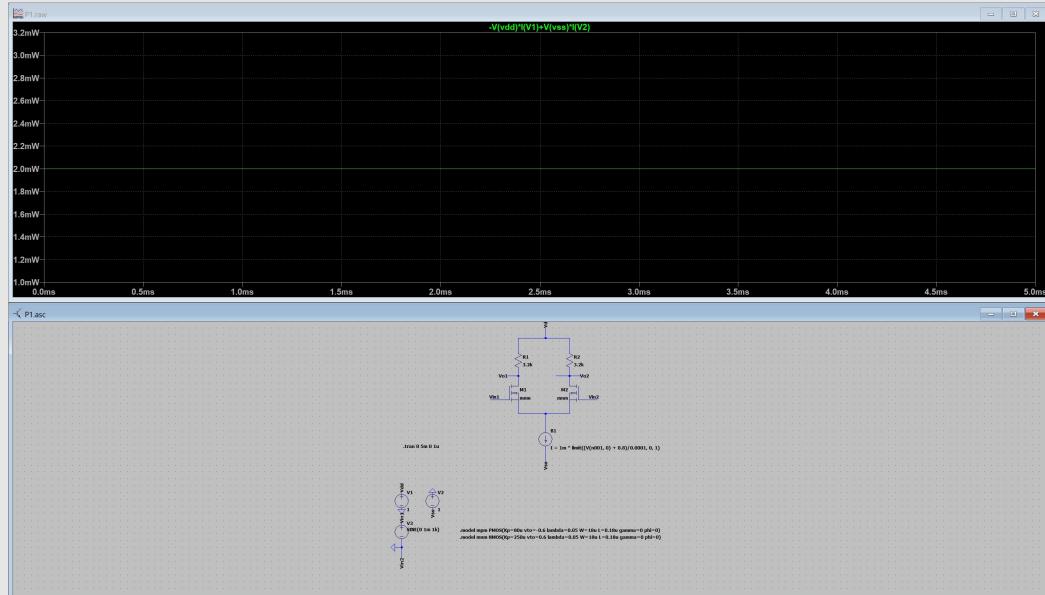
Off-course it doesn't swing because the R_D is in its maximum value.



As shown in Images, It can not have p-p swing

7. Calculate the total power consumption of the circuit.

$$P = VI \rightarrow P = 1^{mA} \times 2^V = 2^{mW}$$



8. Compute the common-mode range (CMR).

$$V_{min} \rightarrow V_G = 0^v$$

$$V_{max} \rightarrow V_{DS} = V_{GS} - V_{th} \rightarrow 0.2 = V_G + 0.8 - 0.6 \rightarrow V_G = 0$$

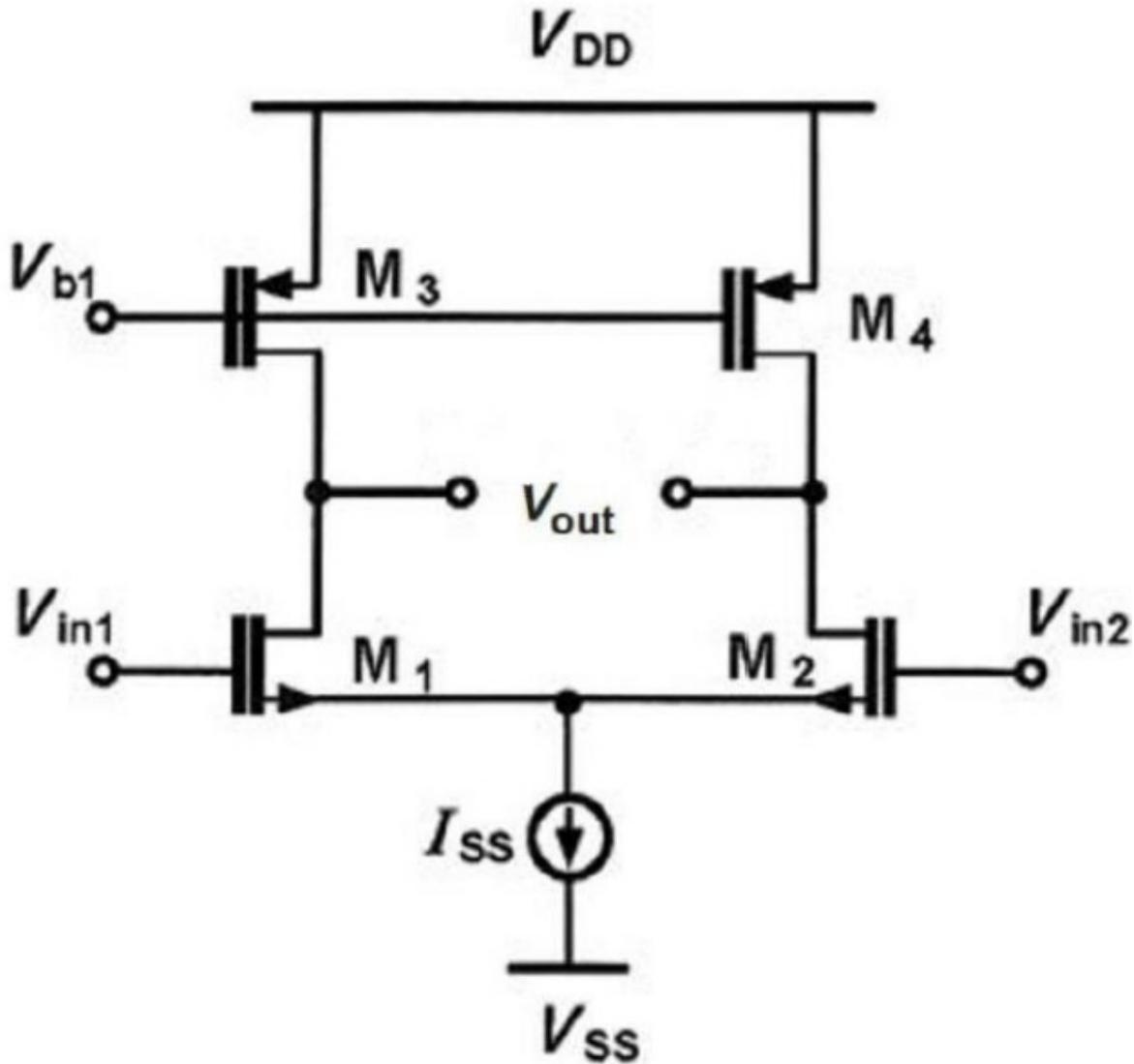
It has zero CMR.

9. Compare theoretical and simulated results, explaining any discrepancies.

There are some differences between them, since our formulas are based on approximations and may not capture all the exact details.

2 Section Two: Active Load

To enhance the performance of the amplifier, an active load has been employed. The gate voltage values for MOSFETs M3 and M4 have been determined, and circuit analysis has been conducted.



Questions:

1. Determine the bias voltage for M_3 and M_4 such that the positive CMR is exactly 1.113V.

saturation condition for M3 :

$$\begin{aligned}V_{DS} &\geq V_{GS} - V_{th} \rightarrow V_D \geq V_G - V_{th} \\V_D &\geq 1.113^v - 0.6^v \rightarrow V_{D_{max}} = 0.513^v \\V_{SD} &\geq V_{SG} - V_{th} \rightarrow V_D \leq V_{b1} + 0.6 \\V_{b1} &= 0.513 - 0.6 = -0.087^v\end{aligned}$$

2. Use saturation conditions to find the drain voltage range.

from last question we have $V_{D_{max}} = 0.513^v$.

we also have from M1 that :

$$V_{D_{min}} = V_{S_1} + V_{od} = -0.8 + 0.2 = -0.6^v \text{ the range is from } -0.6^v \text{ to } 0.513^v.$$

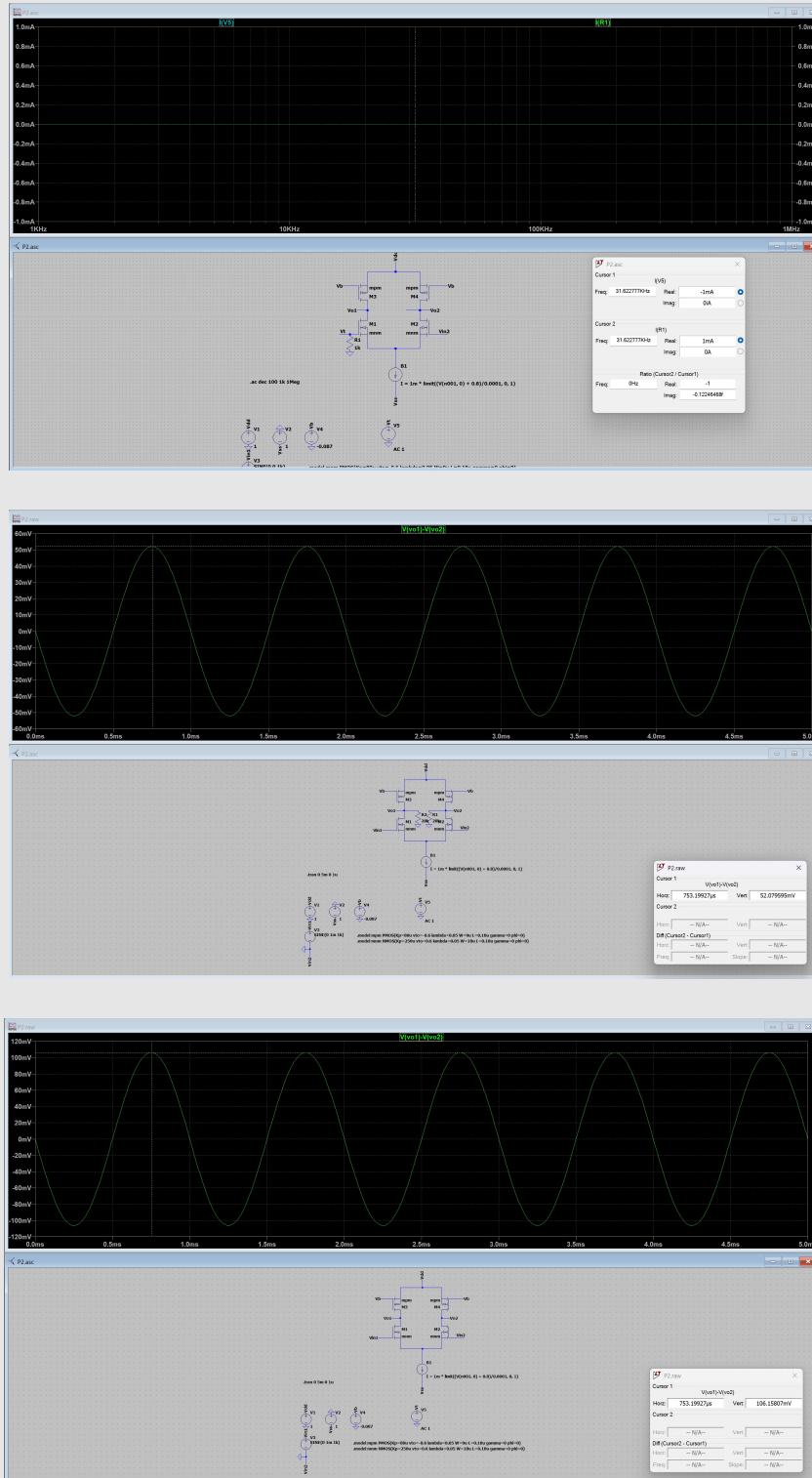
3. Determine the appropriate W/L ratios for M3 and M4.

$$0.5^{mA} = \frac{1}{2} \times \frac{8}{100} \times \frac{W}{L} \times (-0.087 - 1 + 0.6)^2 \rightarrow \frac{W}{L} = 52.7.$$

It is clear that we are using approximate formulas, so to ensure an efficient simulation and prevent the triode mode, we will use a value of 50.

4. Compute the input and output resistance.

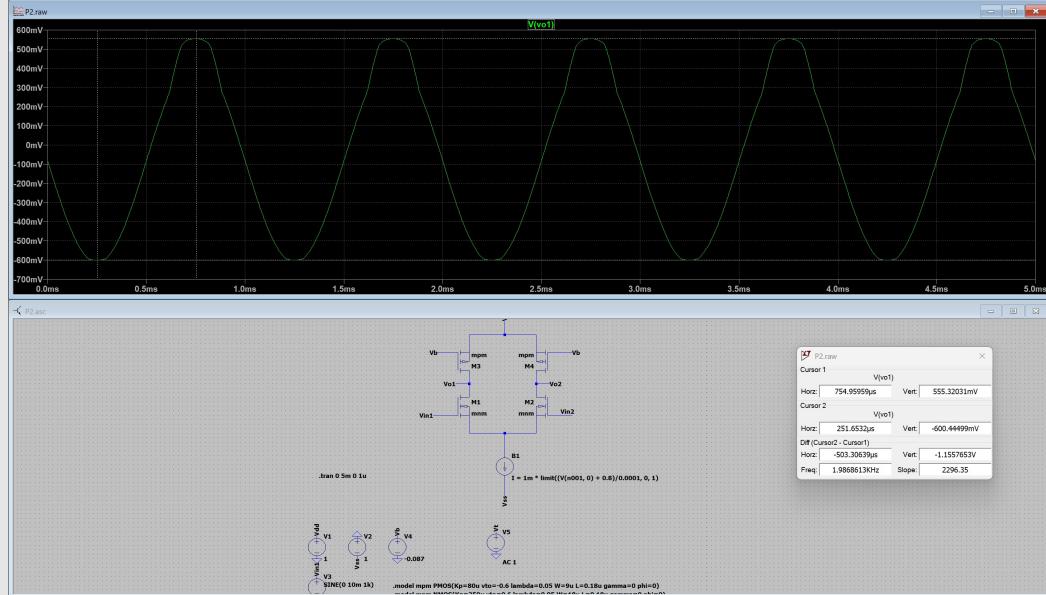
as we have computed in part 1 we know that $r_o = 40^{k\Omega}$ $R_{out} = r_{o_1}||r_{o_3} = 20^{k\Omega} \rightarrow \times 2 = 40^{k\Omega}$ and $R_{in} = \infty$



It is shown that A_v dropped by half, So the R_{out} is $40^{k\Omega}$.
And due to current flow, It is clear that $R_{in} = \infty$.

5. Determine the upper and lower output swing limits.

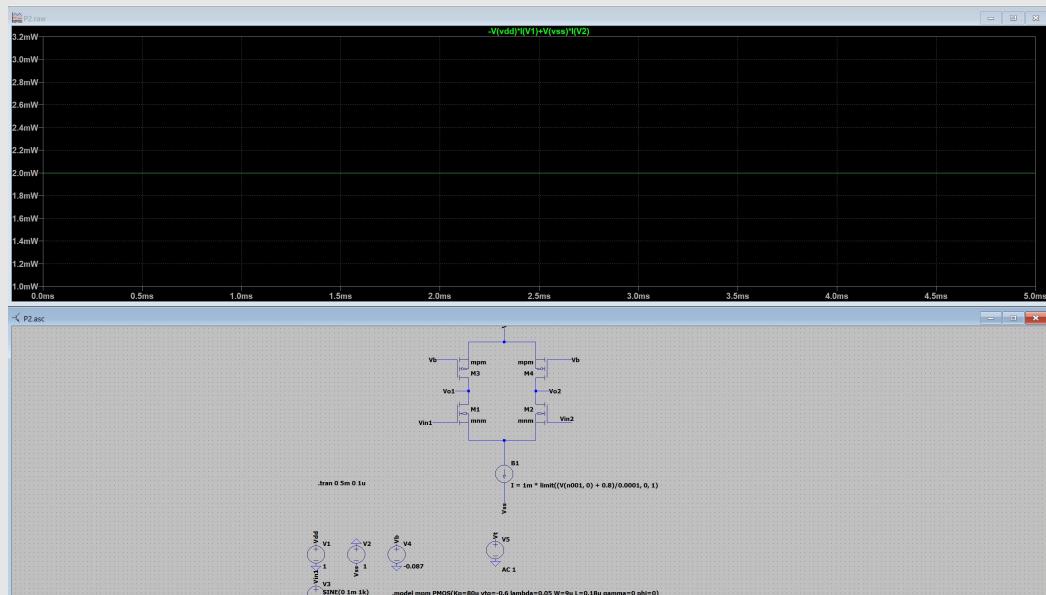
as we calculated in Q2 the swing range is equal to drain voltage range.



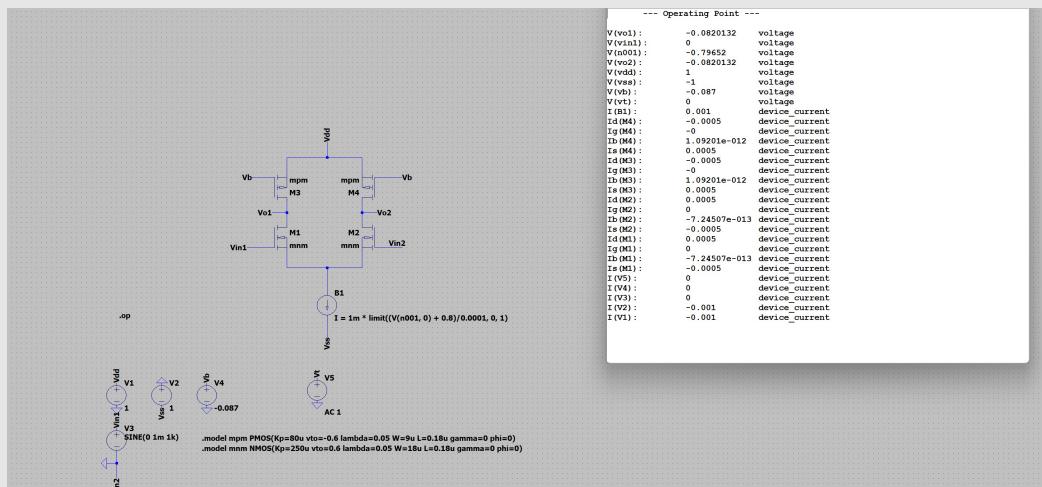
It has a little difference due to last assumed. ($W/L \approx 50$)

6. Compute the total power consumption.

$$P = VI \rightarrow P = 1^{mA} \times 2^V = 2^{mW}$$



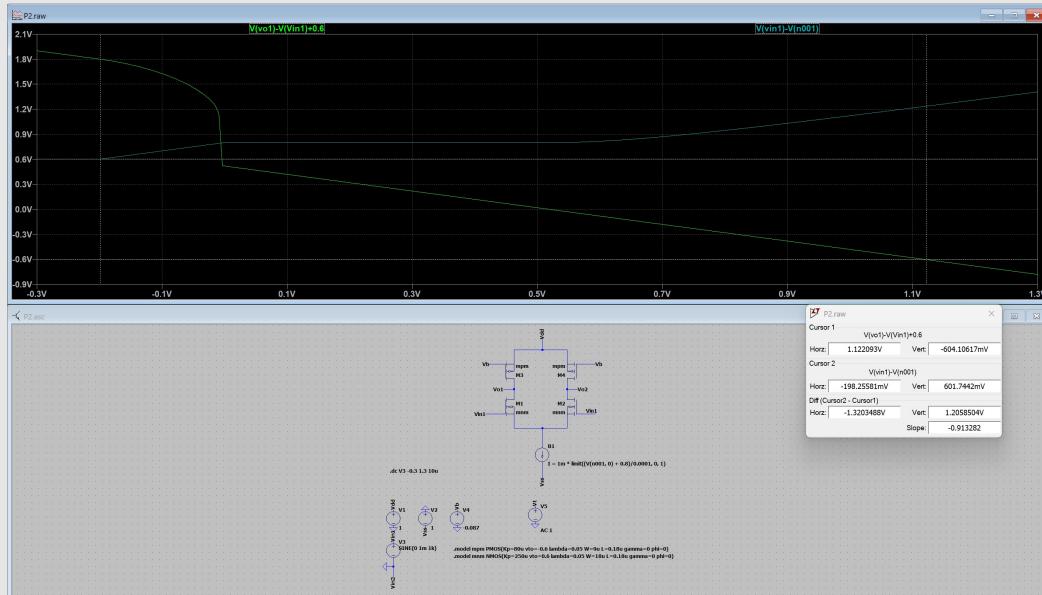
7. Perform a DC analysis of the circuit using simulations.



8. Compute the common-mode range (CMR).

$$I_D = 0 \rightarrow V_{od} = 0 \rightarrow V_G = -0.2^v$$

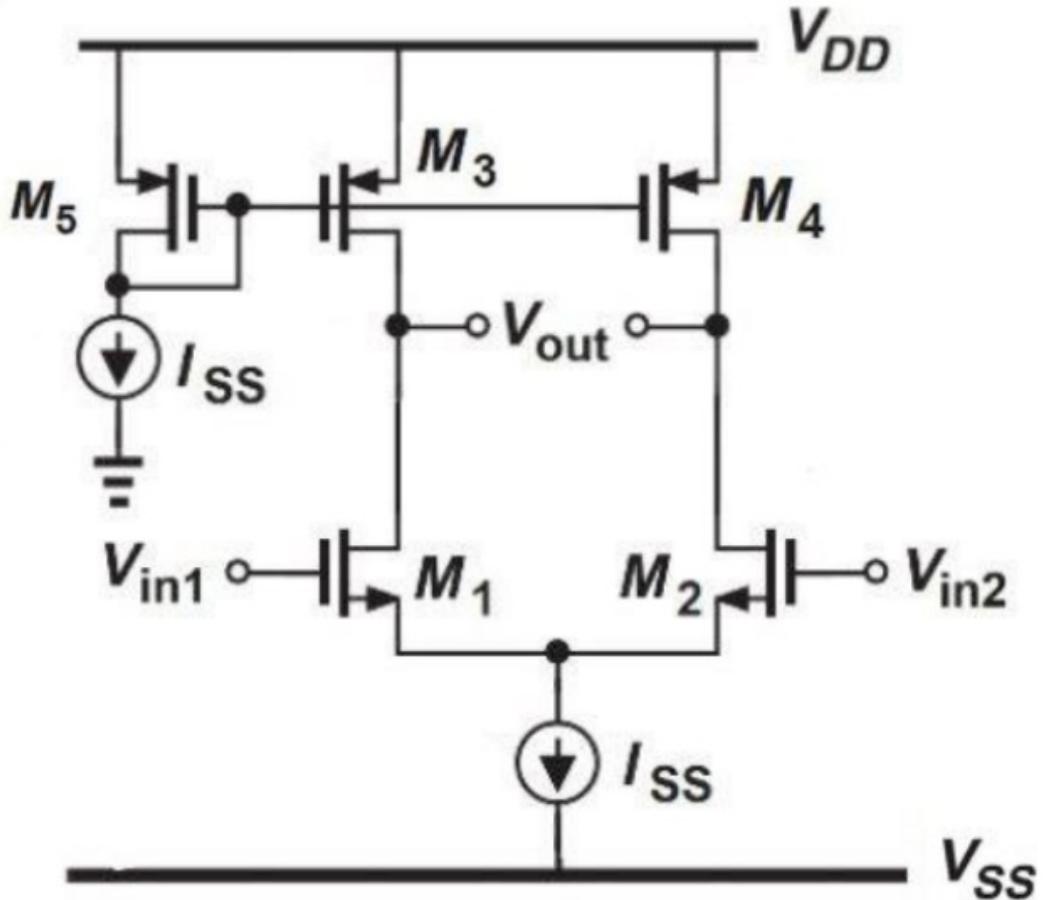
→ due to assumption we've reached to $V_{G_{max}} = 1.113$



9. Compare theoretical and simulated results, explaining any discrepancies.

3 Section Three: Current Mirror

A current mirror has been used to provide bias current. Theoretical analysis and simulation have been performed to evaluate this structure.



Questions:

1. Determine the W/L ratio for M5 if the current source is designed to provide 1mA.

For M3 we have :

$$0.5^{mA} = \frac{1}{2} \cdot \frac{8}{100} \cdot 50(V_{GS} - V_{th})^2$$

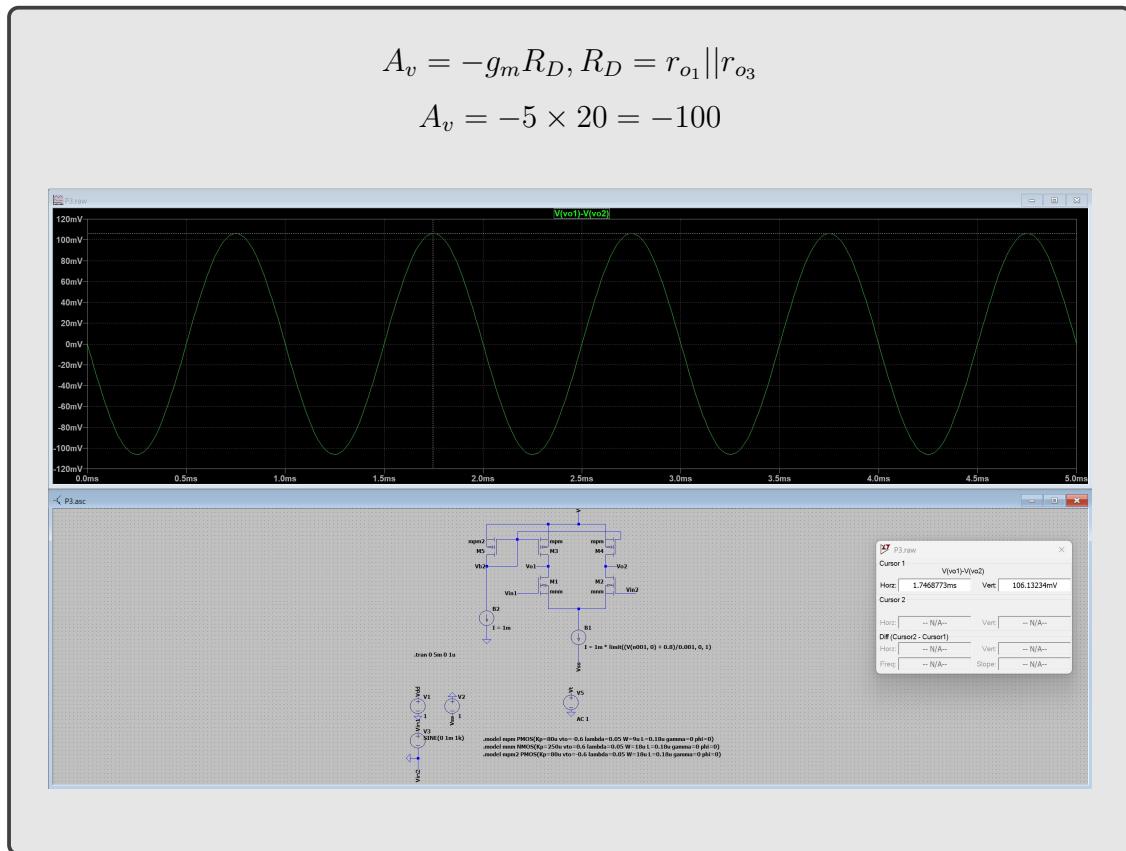
$$1 = 4 \times (V_G - 0.4)^2 \rightarrow V_G = -0.1^v$$

So for M5 :

$$1 = \frac{1}{2} \times \frac{8}{100} \times \frac{W}{L} \cdot (V_G - 0.4)^2$$

$$\frac{W}{L} = 100$$

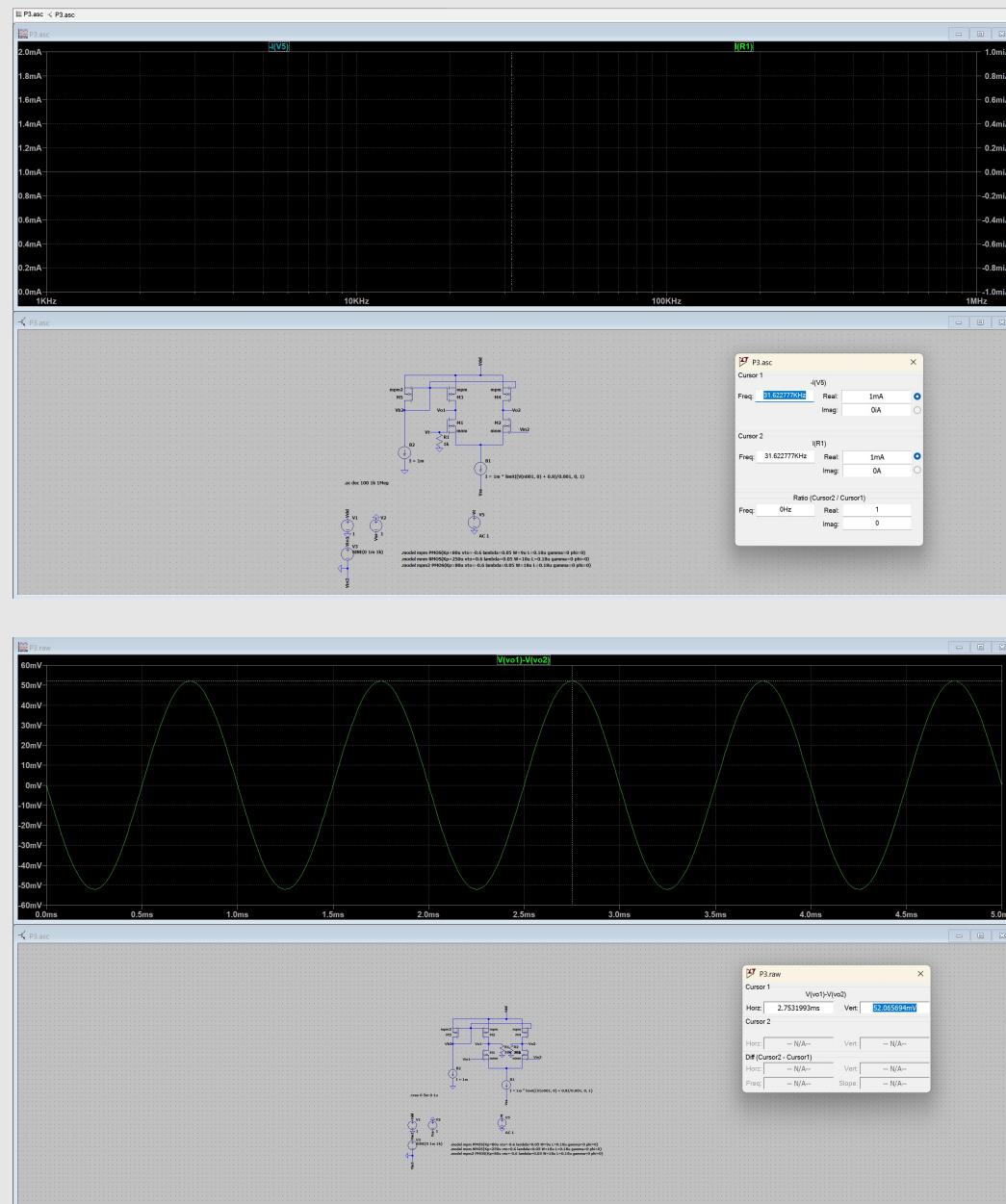
2. Compute the differential gain.



3. Determine the input and output resistance.

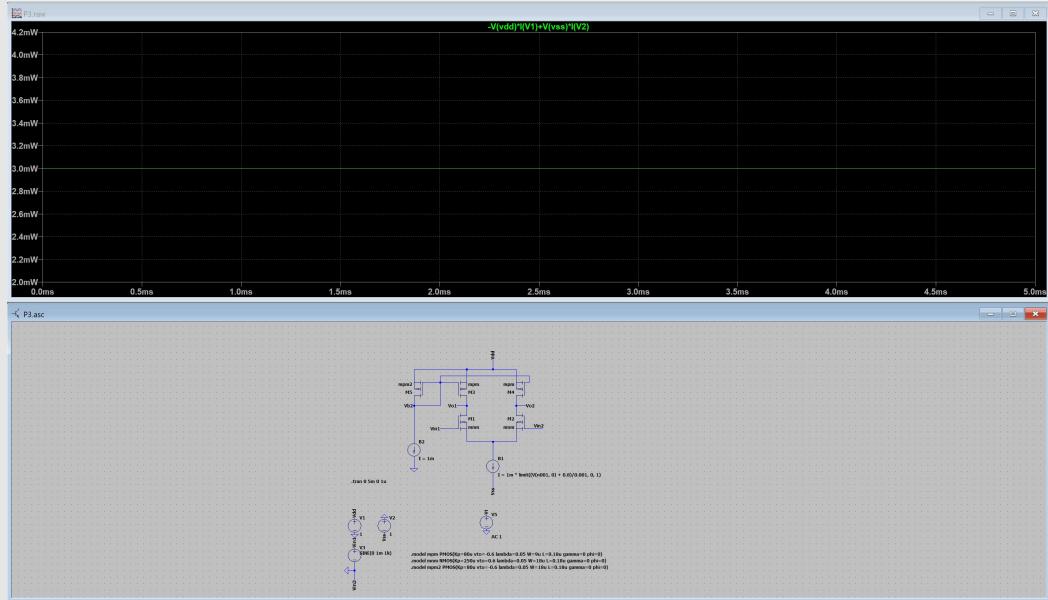
$$R_{in} = \infty$$

$$R_{out} = r_{o_1} || r_{o_3} = 20^{k\Omega} \rightarrow \times 2 = 40^{k\Omega}$$



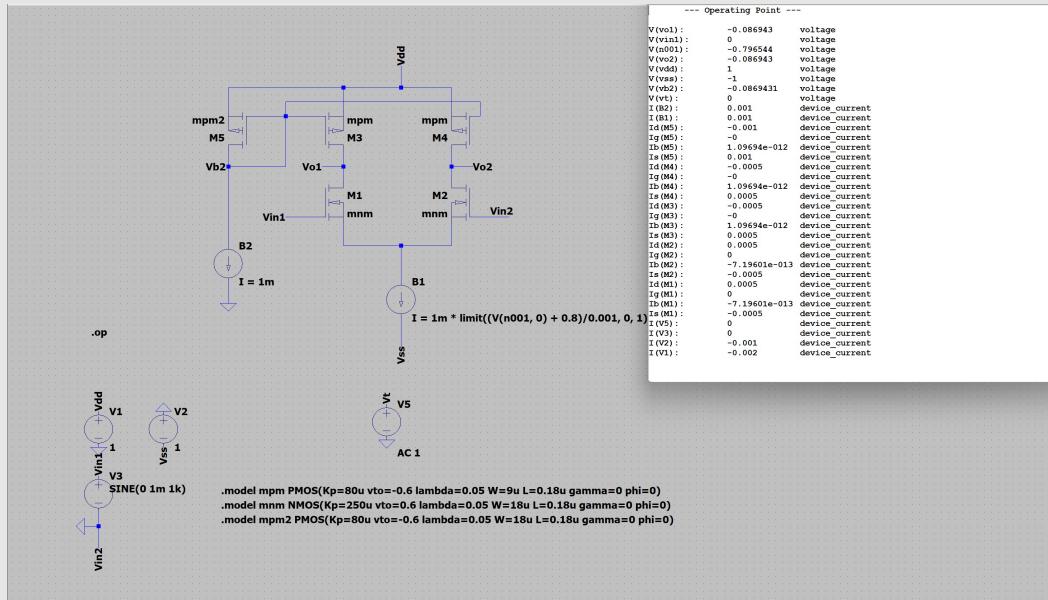
4. Calculate the total power consumption.

$$P = VI \rightarrow P = 2^{mA} \times 1^V + 1^{mA} \times 1^V = 3^{mW}$$



5. Perform a DC analysis using simulations.

$$P = VI \rightarrow P = 2^{mA} \times 1^V + 1^{mA} \times 1^V = 3^{mW}$$



6. Compare theoretical and simulated results, explaining any discrepancies.
 7. Compare the advantages and disadvantages of using an active load in this circuit compared to the previous configuration.

- **Advantages :**

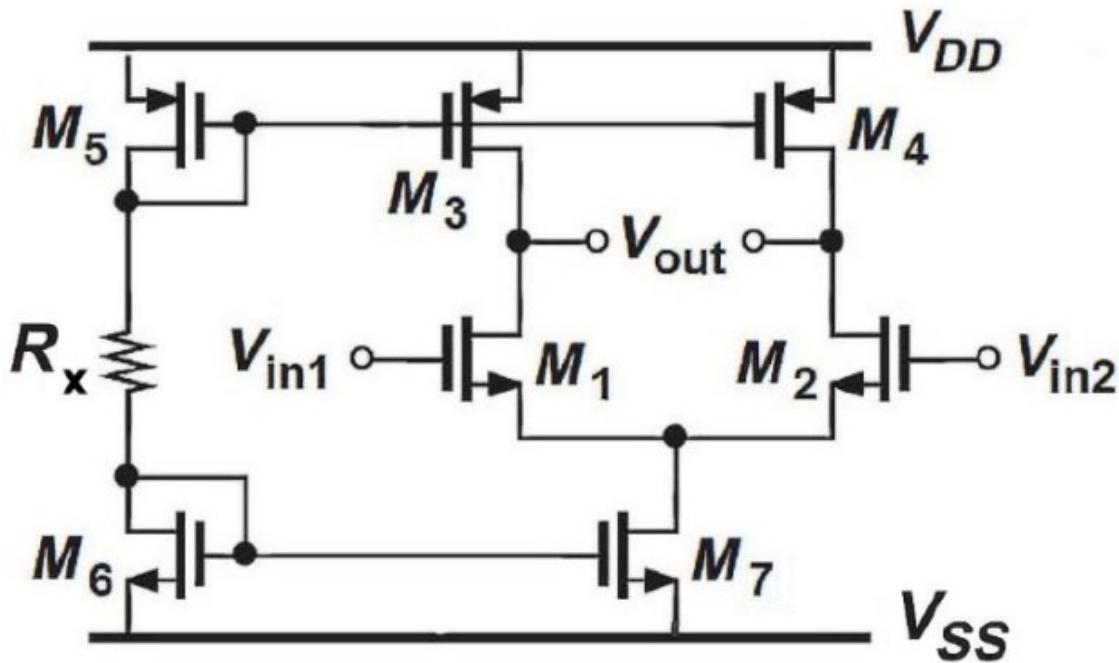
- Higher Gain
- Better Common-Mode Rejection Ratio (CMRR)
- Smaller Circuit Size (Due to using only MOSFETS)

- **Disadvantages :**

- Higher power consumption

4 Section Four: Circuit Optimization

In this section, ideal current sources have been removed and replaced with current mirrors. Analyses related to circuit performance improvement have been presented.



Questions:

1. Assume W/L for M6 is 280. Determine the resistance R_X such that a 1mA current passes through both transistors. Provide results in k with three decimal places.

For M5 we have :

$$1 = \frac{1}{2} \cdot \frac{8}{100} \cdot 100 \cdot (V_G - 1 + 0.6)^2 \rightarrow V_G = -0.1^v$$

So For M6 we have :

$$1 = \frac{1}{2} \cdot \frac{1}{4} \cdot 280 \cdot (-0.1 - R_x + 1 - 0.6)^2 \rightarrow 1 = 35 \cdot (0.3 - R_x)^2$$

$$\leftrightarrow R_x = 0.1309^{k\Omega}$$

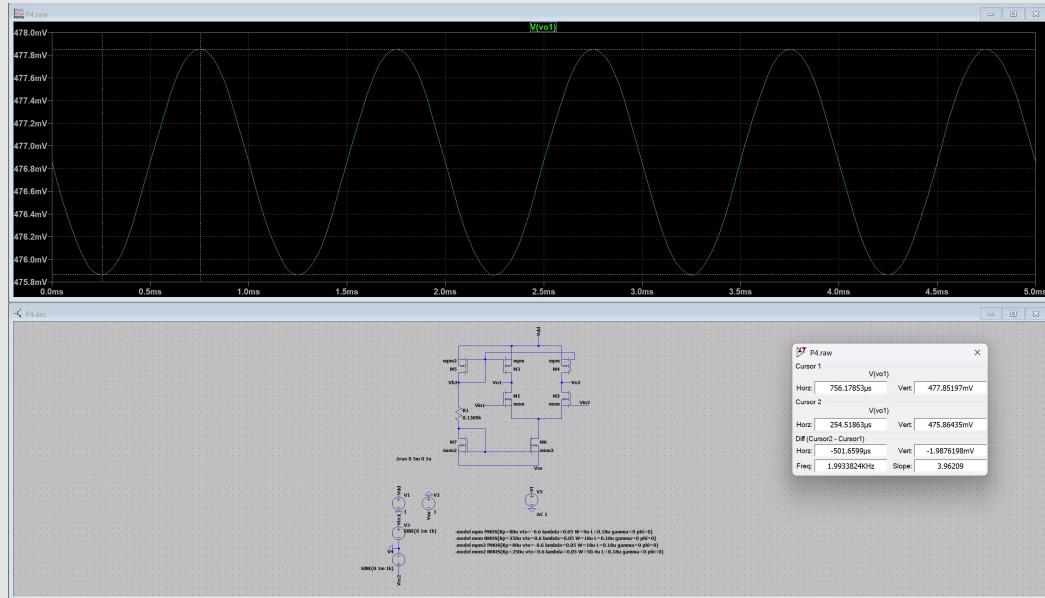
2. Determine the W/L ratio for M7.

$$1 = \frac{1}{2} \times \frac{1}{4} \times \frac{W}{L} \cdot ((-0.1 - 0.1309) - (-1) - 0.6)^2$$
$$\frac{W}{L} \approx 280$$

3. Compute the single-ended Common gain and differential gain.

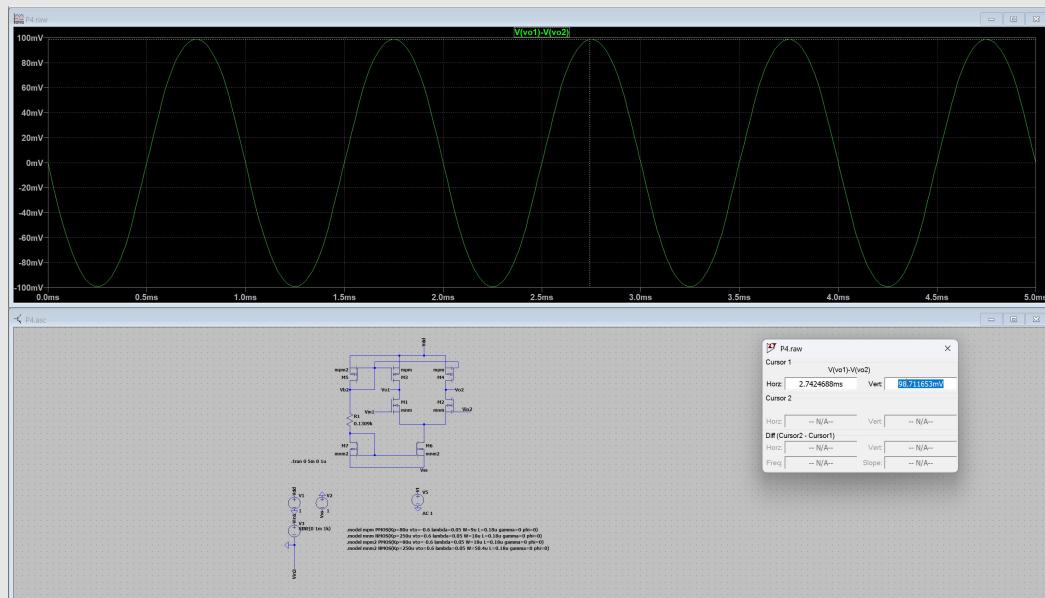
Common Mode :

$$A_v = -\frac{R_D}{\frac{1}{g_{m_1}} + 2.r_{o7}} = -\frac{40}{0.2 + 2 \times 20} = -0.995$$



Differential Mode :

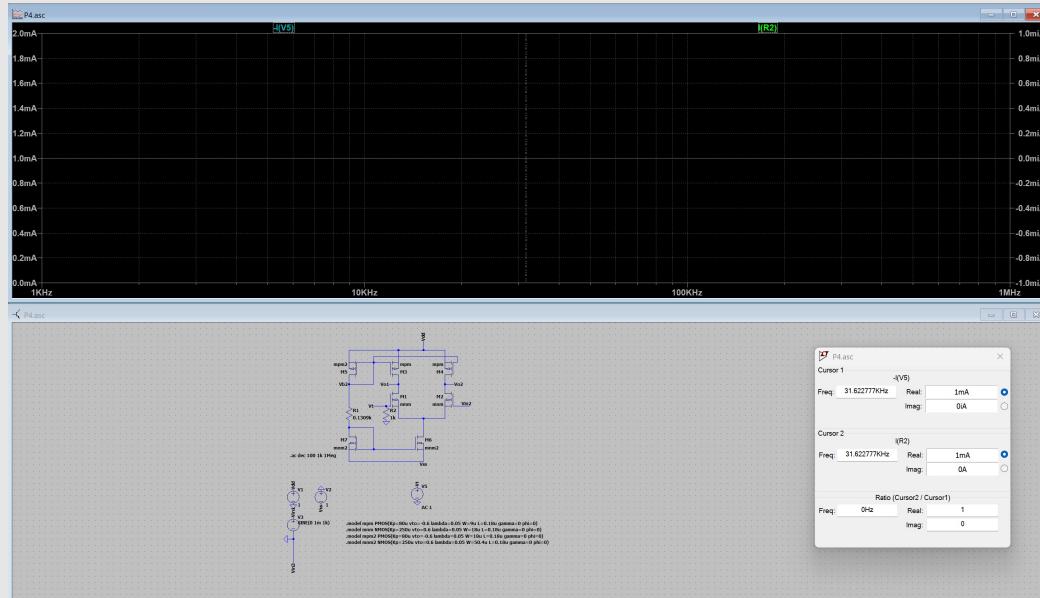
$$A_v = -\frac{R_D || r_{o1}}{\frac{1}{g_m}} = -\frac{20}{0.2} = -100$$



4. Determine the input and output resistance (R_{out} for Both Common and Differential

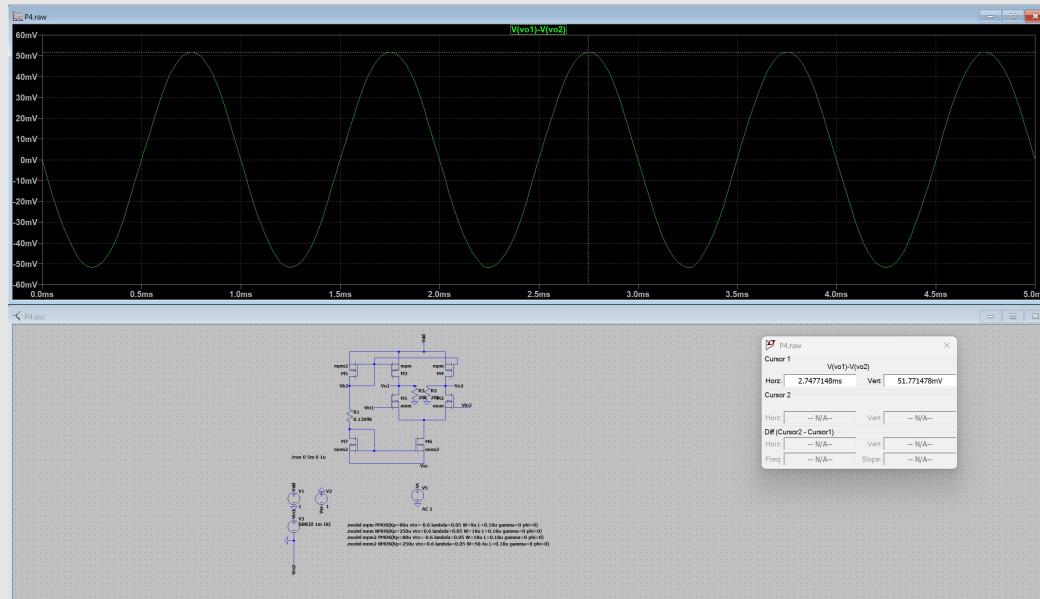
modes).

$$R_{in} = \infty$$



Differential Mode :

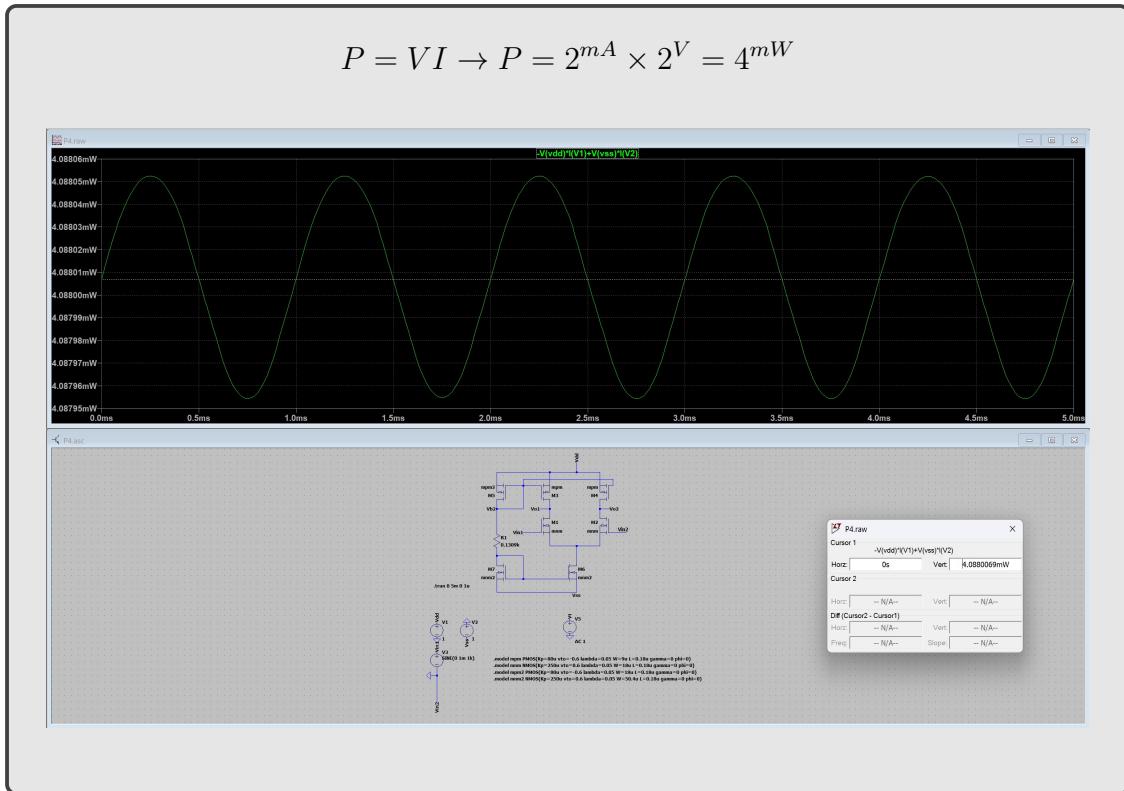
$$R_{out} = r_{o1} || r_{o3} = 20^{k\Omega} \rightarrow \times 2 = 40^{k\Omega}$$



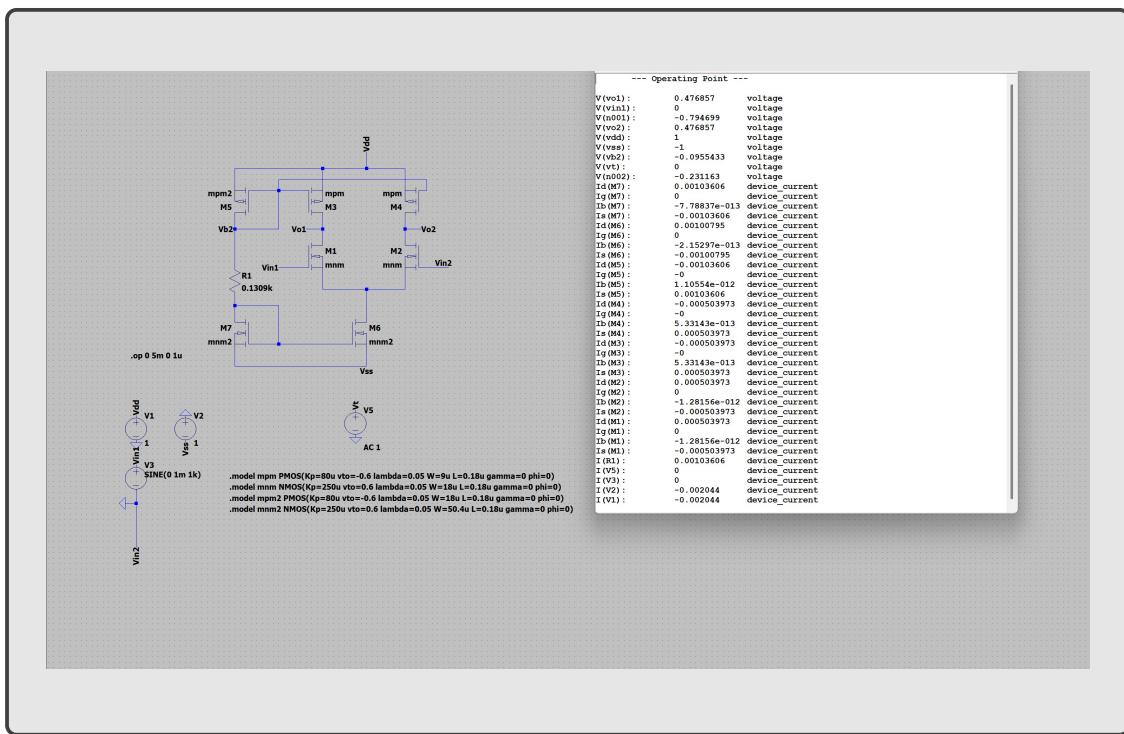
Common Mode :

$$R_{out} = (r_{o1}(1 + g_m 2r_{o7}) + 2r_{o7}) || r_{o3} = (40(1 + 5 \times 40) + 40) || 40 = 39.8^{k\Omega}$$

- Compute the total power consumption.



6. Perform a DC analysis using simulations.



7. Explain why, despite an increase in differential gain, the single-ended gain is not optimal. Provide a way to ensure all transistors remain in saturation while maximizing the gain.

It is better to place a small resistor or MOSFET in the source of M7 and adjust the value of R_x in such a way that the circuit bias remains unchanged. In this case, the common-mode gain can be reduced without altering the differential-mode gain.