ARM Microcontroller Based Programming

Lecture 1

Introduction to ARM Processor

History

1990

ARM was formed in as Advanced RISC Machines Ltd., a joint venture of Apple Computer, Acorn Computer Group, and VLSI Technology.

1991

ARM introduced the ARM6 processor family to meet Apple requirement for its product "Personal Digital Assistant" called Newton.

Unfortunately, the Newton was not a great success and so *Robin Saxby*, ARM's CEO, decided to grow the business by pursuing what we now call intellectual property "IP" business model.

The ARM processor was licensed to many semiconductor companies for an upfront license fee and then royalties on production silicon. This effectively incentivized ARM to help its partner get to high volume shipments as quickly as possible.

History

1993

Nokia approached *TI* to produce a chipset for an upcoming GSM mobile phone and TI proposed an ARM7 based system to meet Nokia's performance and power requirements. Unfortunately Nokia rejected the proposal !

ARM came up with a radical idea to create a subset of the ARM instruction set that required just 16 bits per instruction. This improved the code density by about 35% and brought the memory footprint down to a size comparable with 16 bit microcontrollers.

The first ARM-powered GSM phone was the hugely popular *Nokia6110* and the *ARM7TDMI*.

History

ARMCORTEX®
Processor Technology

1997
ARM had grown to become a £27m business with a net income of £3m !
ARM then decided to build software-based systems on a single chip, the so-called system-on-chip, or SoC.

2001
ARM9 was announced. It was fully synthesizable with a 5 stage pipeline and a proper MMU, as well as hardware support for Java acceleration and some DSP extension.

2002
ARM11 families had extended the capability of the ARM architecture in the direction of higher performance with the introduction of multi-processing, SIMD multimedia instructions, DSP capability, Java acceleration etc

History

ARM CORTEX®
Processor Technology

2005
The ARM Cortex ... !
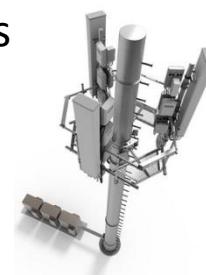
| Cortex - A	Cortex - R	Cortex - M
Application Processors for full OS and Open Application Platforms	Embedded Processors for real time signal processing and control applications	Microcontroller Oriented Processors
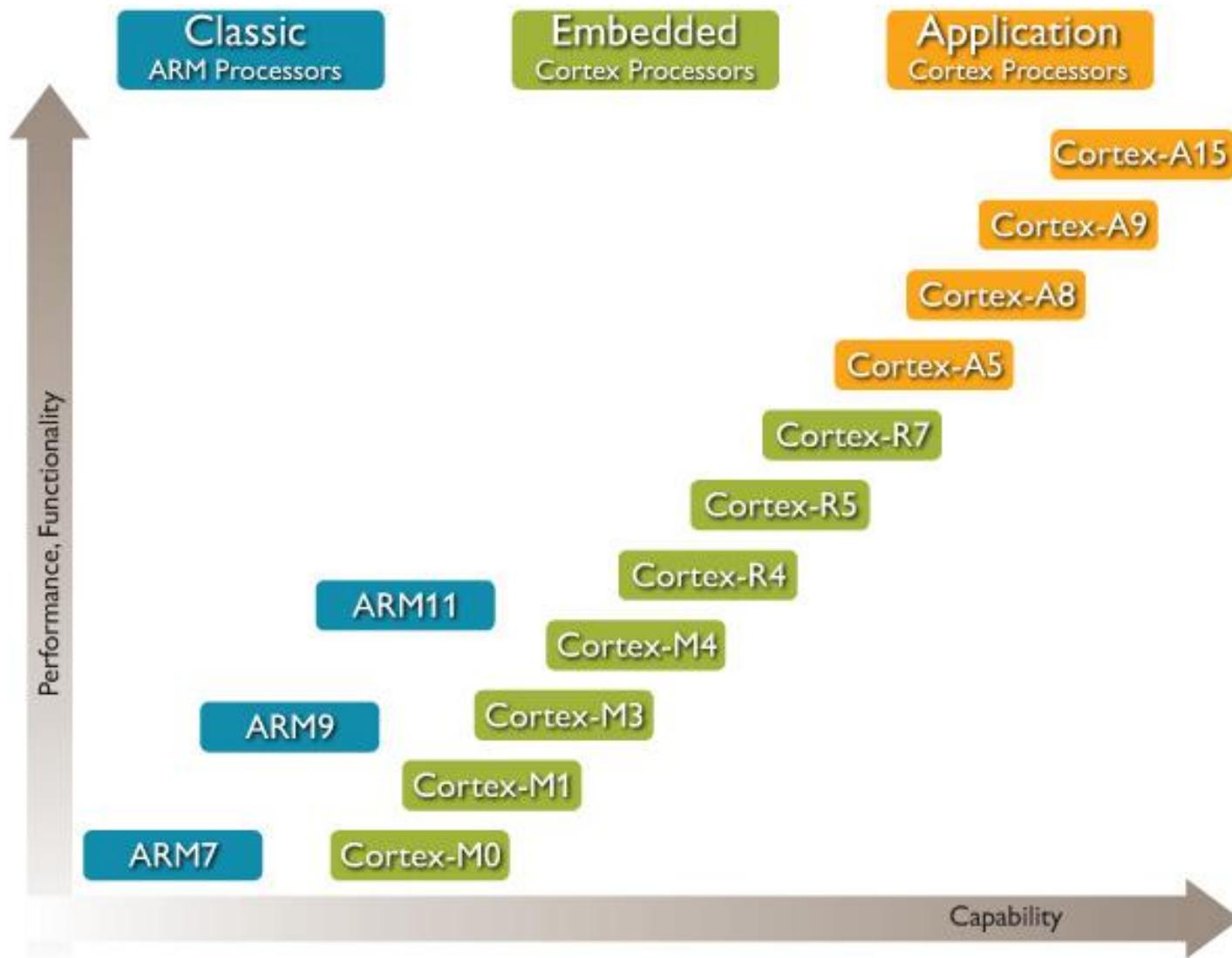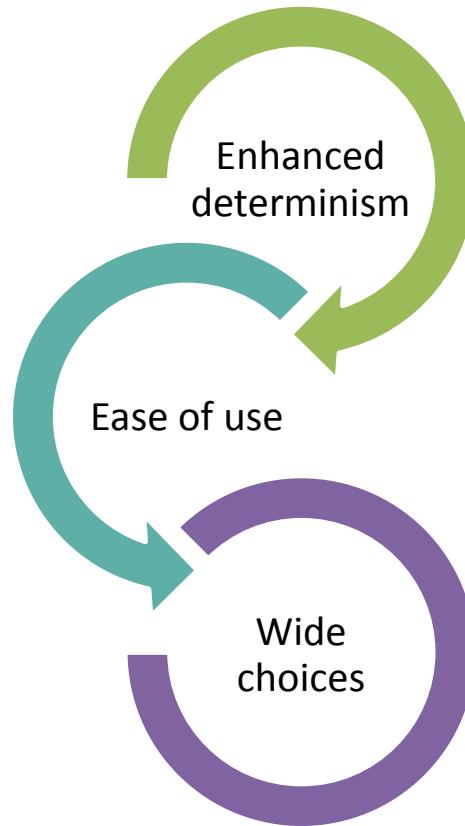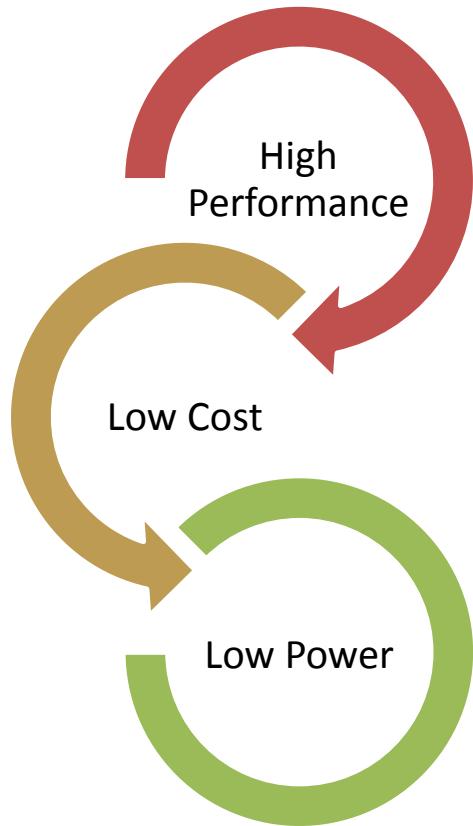
ARM Processor Roadmap
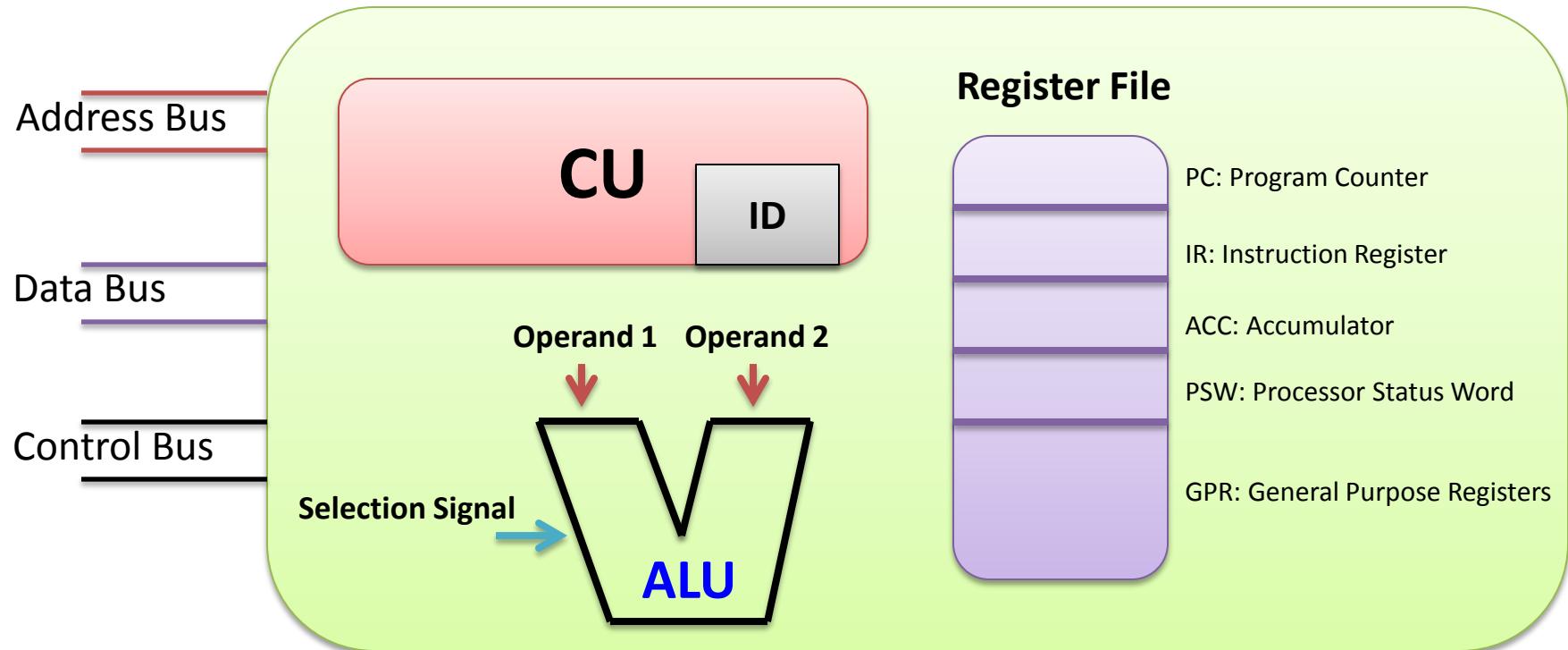
ARM Major Characteristics

High Performance

Low Cost

Low Power

Enhanced determinism

Ease of use

Wide choices

General Processor Architecture

Address Bus

Data Bus

Control Bus

CU

ID

Register File

Operand 1   Operand 2

Selection Signal

ALU

PC: Program Counter

IR: Instruction Register

ACC: Accumulator

PSW: Processor Status Word

GPR: General Purpose Registers
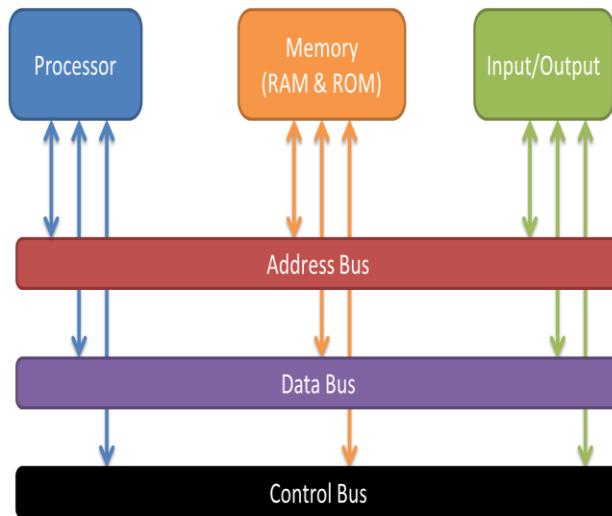
CU : Control Unit
ID   : Instruction Decoder
ALU: Arithmetic Logic Unit
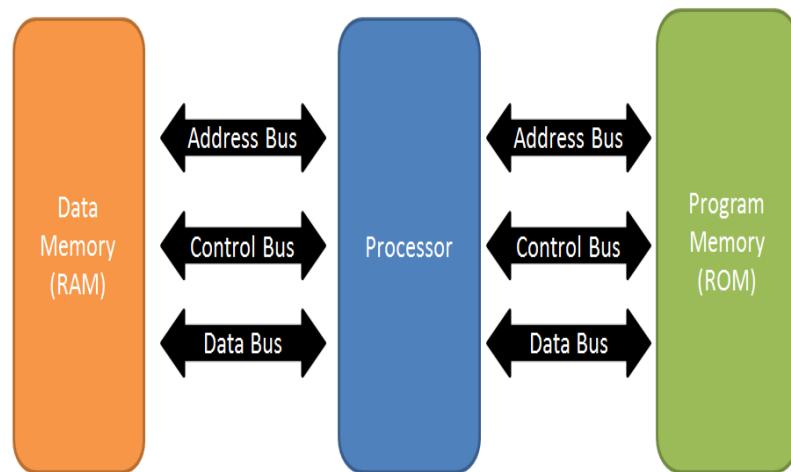
Von Numann Vs Harvard Architecture

1- Von Numann

2- Harvard Architecture

- Simple in Design

- The code is executed serially

- Complex in design

- The code is executed in parallel
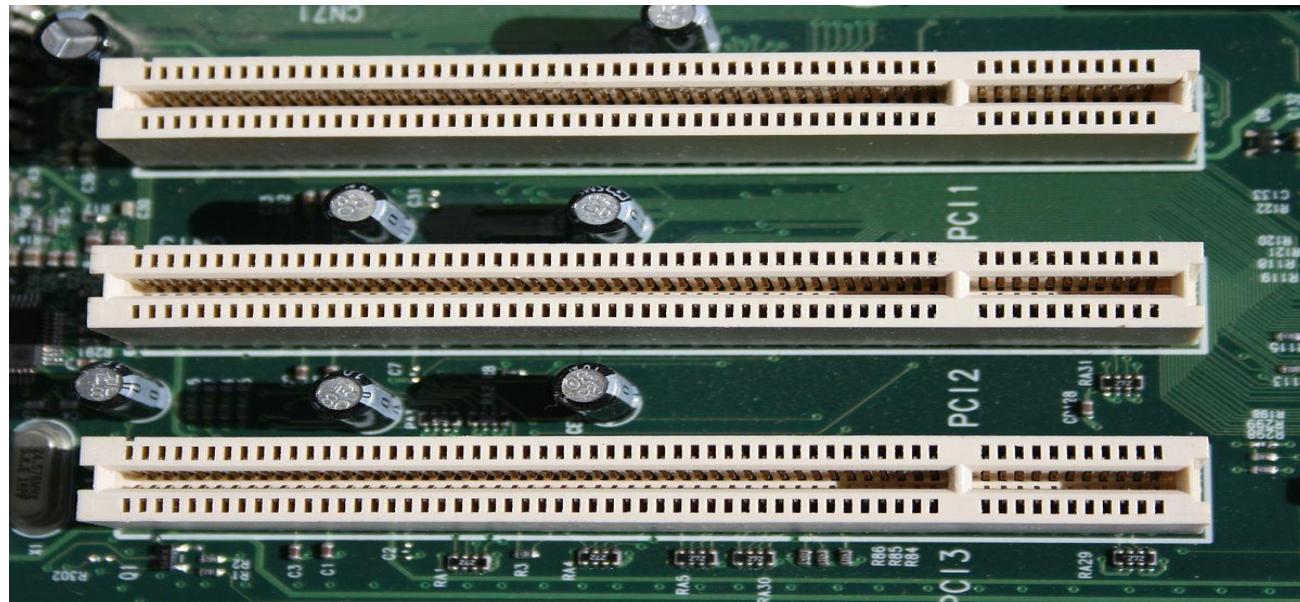
Note: *Bus Definition*

Bus is not just a group of wires, a bus is a communication system that transfers data between components inside the processor, or between processor and peripherals. This expression covers all related *hardware components* (wire, optical fiber, etc.) and *software*, including *communication protocols*.

Example:

PCI Bus

Peripheral Component Interconnect
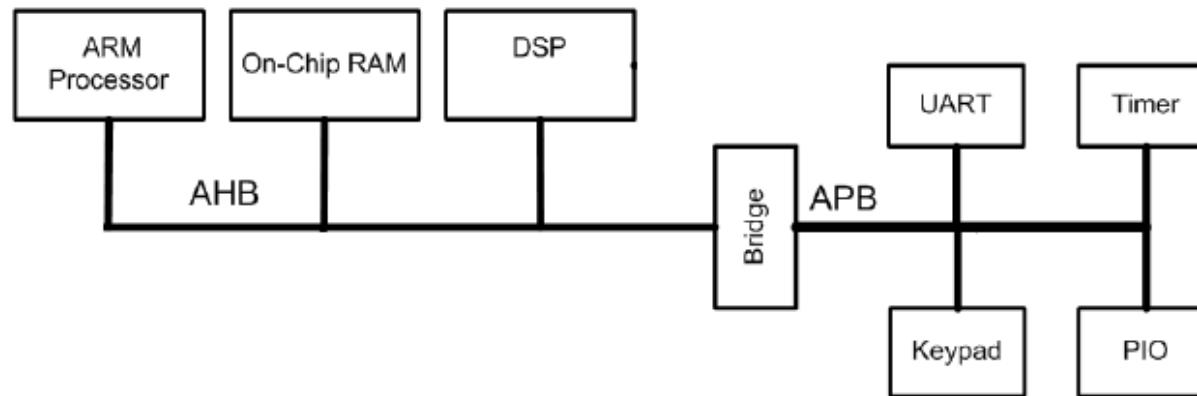
AMBA Bus

Advanced Microcontroller Bus Architecture

Open standard, on-chip interconnect specification for the connection and management of functional blocks in system-on-a-chip (SoC) designs. It was introduced by ARM in 1996 and currently it includes some protocols that considered as *de facto standard* for embedded processors because they are well documented and can be used without royalties.

AHB Vs APB

AHB
stands for *Advanced High Performance Bus*
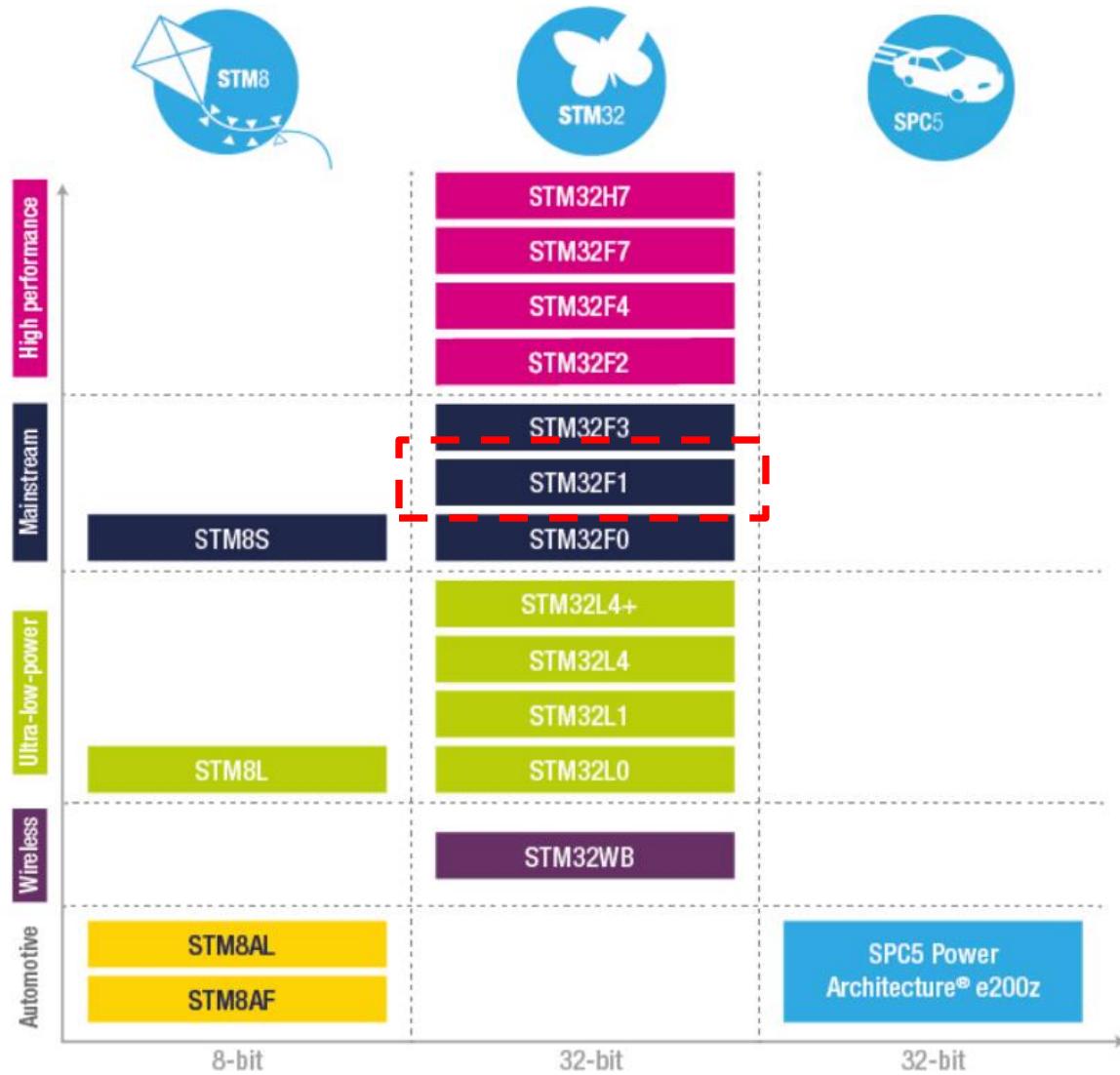
- High Performance

- Full Duplex

- Support Pipelining

- MultiMaster operation

- Complex in design

APB
stands for *Advanced Peripheral Bus*
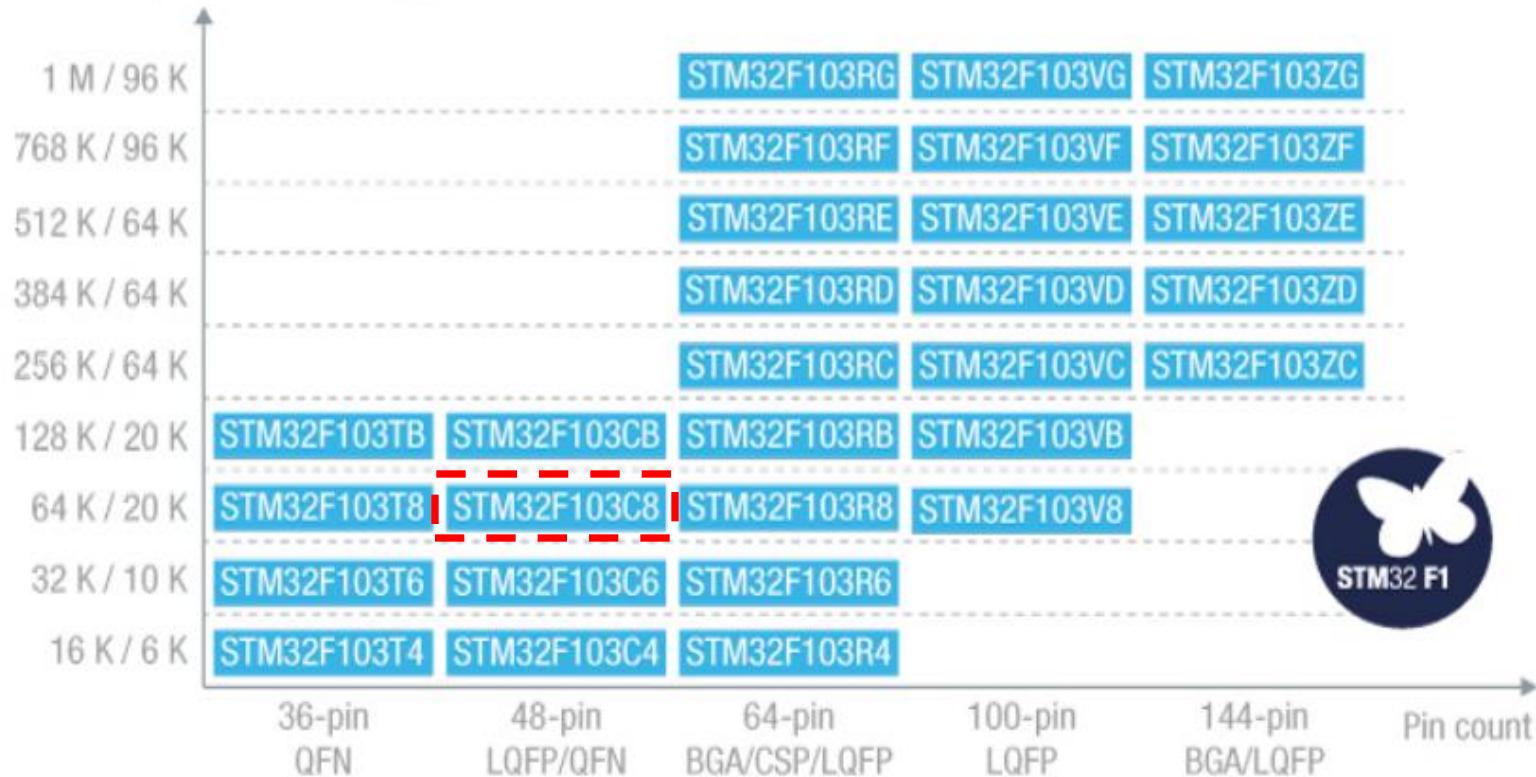
- Low Power

- No Pipelining

- Simple in design

- Used for connecting peripherals

ST Product lines
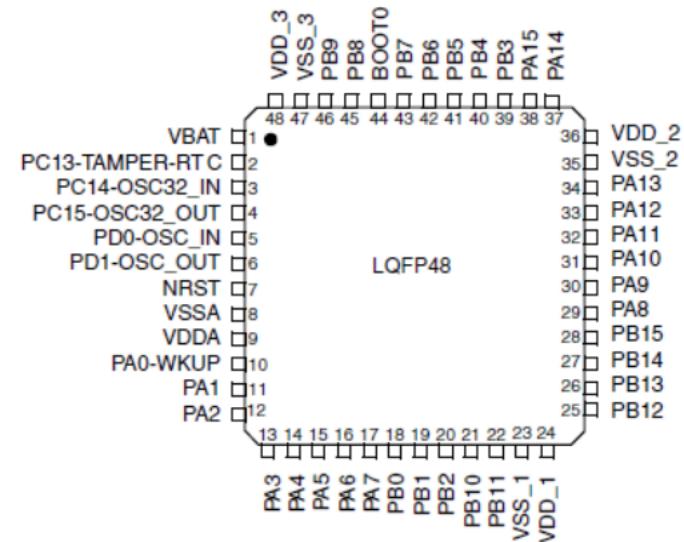
STM32F103 Family
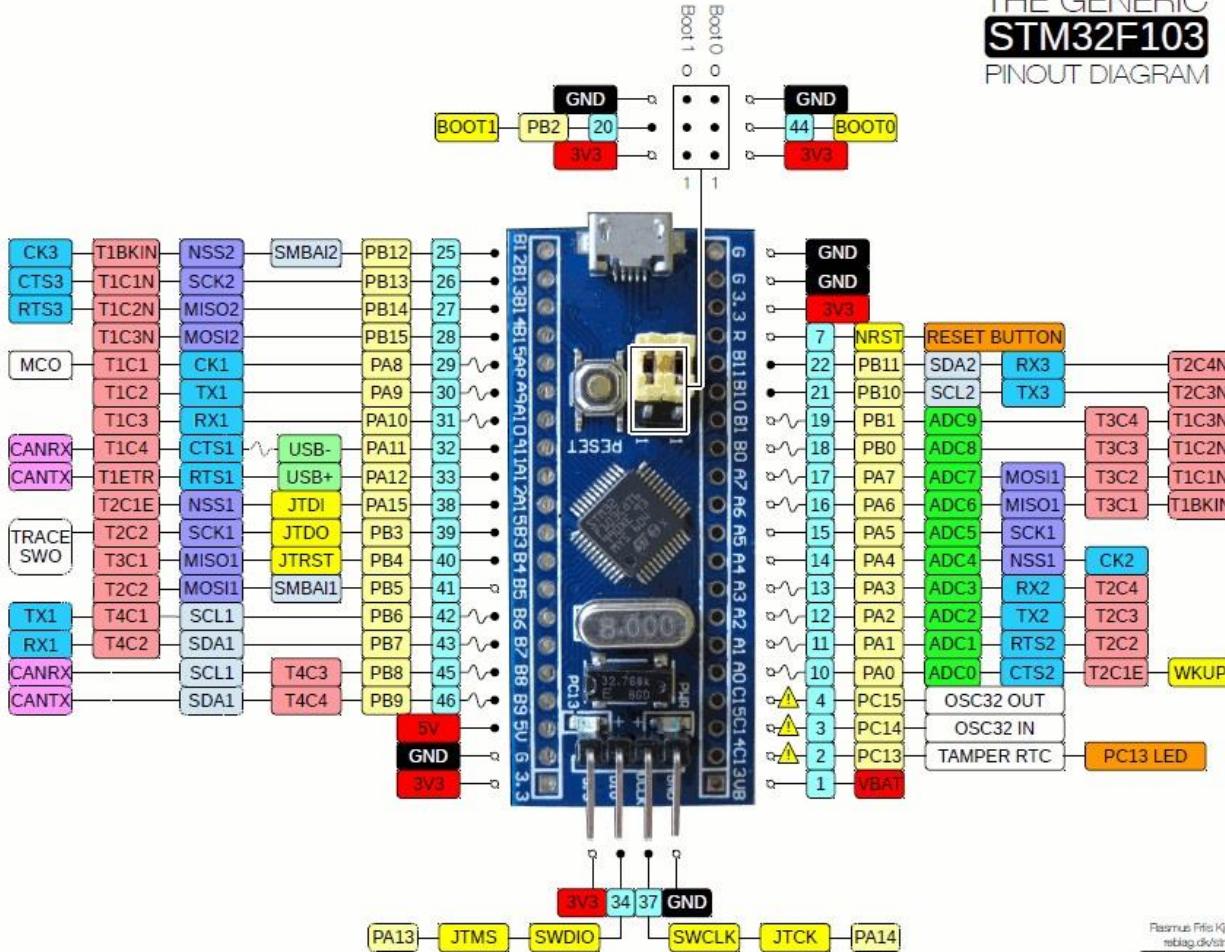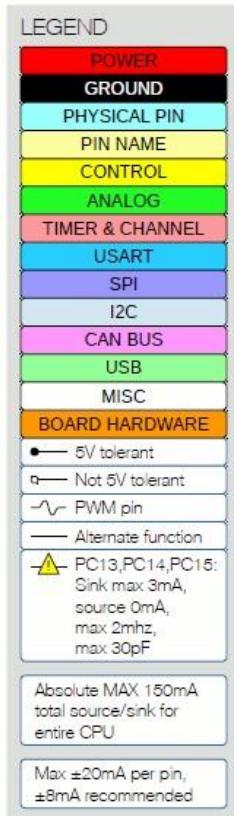
STM32F103C8 Specifications

Core	ARM Cortex-M3
Max Operating Frequency	72 MHz
Flash Memory Size	64 KB
RAM Size	20 KB
Timers	4 x 16 Bit Timers 2 x WDT 24-Bit Down Counter RTC
ADC Converter	10 x 12 Bit Channels
GPIO	32 High Current
I2C Bus	2 Channels
SPI Bus	2 Channels
USART Bus	3 Channels
CAN Bus	1 Channel
Operating Voltage	2 to 3.6 Voltage
Operating Temperature	- 40 to 105 Degree C

Development Kit

THE GENERIC
STM32F103
PINOUT DIAGRAM

LEGEND

POWER	
GROUND	
PHYSICAL PIN	
PIN NAME	
CONTROL	
ANALOG	
TIMER & CHANNEL	
USART	
SPI	
I2C	
CAN BUS	
USB	
MISC	
BOARD HARDWARE	

- ●— 5V tolerant
- ○— Not 5V tolerant
- ∿ PWM pin
- — Alternate function
- ⚠ PC13,PC14,PC15: Sink max 3mA, source 0mA, max 2mhz, max 30pF

Absolute MAX 150mA total source/sink for entire CPU

Max ±20mA per pin, ±8mA recommended

Boot1 0 / Boot0 0

GND · BOOT1 · PB2 · 20 · · 44 · BOOT0 · GND
3V3 · · · 3V3

									GND
CK3	T1BKIN	NSS2	SMBAl2	PB12	25				GND
CTS3	T1C1N	SCK2		PB13	26				3V3
RTS3	T1C2N	MISO2		PB14	27		7	NRST	RESET BUTTON
	T1C3N	MOSI2		PB15	28		22	PB11	SDA2	RX3	T2C4N
MCO	T1C1	CK1		PA8	29		21	PB10	SCL2	TX3	T2C3N
	T1C2	TX1		PA9	30		19	PB1	ADC9		T3C4	T1C3N
	T1C3	RX1		PA10	31		18	PB0	ADC8		T3C3	T1C2N
CANRX	T1C4	CTS1	USB-	PA11	32		17	PA7	ADC7	MOSI1	T3C2	T1C1N
CANTX	T1ETR	RTS1	USB+	PA12	33		16	PA6	ADC6	MISO1	T3C1	T1BKIN
	T2C1E	NSS1	JTDI	PA15	38		15	PA5	ADC5	SCK1	
TRACE SWO	T2C2	SCK1	JTDO	PB3	39		14	PA4	ADC4	NSS1	CK2
	T3C1	MISO1	JTRST	PB4	40		13	PA3	ADC3	RX2	T2C4
	T2C2	MOSI1	SMBAl1	PB5	41		12	PA2	ADC2	TX2	T2C3
TX1	T4C1	SCL1		PB6	42		11	PA1	ADC1	RTS2	T2C2
RX1	T4C2	SDA1		PB7	43		10	PA0	ADC0	CTS2	T2C1E	WKUP
CANRX		SCL1	T4C3	PB8	45		4	PC15	OSC32 OUT
CANTX		SDA1	T4C4	PB9	46		3	PC14	OSC32 IN
				5V			2	PC13	TAMPER RTC	PC13 LED
				GND			1	VBAT	
				3V3					

3V3 · 34 · 37 · GND

PA13 · JTMS · SWDIO · SWCLK · JTCK · PA14

Rasmus Friis Kjeldsen
rasblag.dk/stm32

V1.0

Processor Architecture

Memory Map

0xE00FF000	ROM table
0xE00FEFFF	External private peripheral bus
0xE0042000	
0xE0041000	ETM
0xE0040000	TPIU

0xE003FFFF	Reserved
0xE000F000	
0xE000E000	NVIC
0xE000DFFF	Reserved
0xE0003000	
0xE0002000	FPB
0xE0001000	DWT
0xE0000000	ITM

0x43FFFFFF		Bit-band alias
0x42000000	32 MB	
0x41FFFFFF		
0x40100000	31 MB	
0x40000000	1 MB	Bit-band region

0x23FFFFFF		Bit-band alias
0x22000000	32 MB	
0x21FFFFFF		
0x20100000	31 MB	
0x20000000	1 MB	Bit-band region

Vendor specific		0xFFFFFFFF
		0xE0100000
Private peripheral bus: Debug/external		0xE00FFFFF
		0xE0040000
Private peripheral bus: Internal		0xE003FFFF
		0xE0000000
		0xDFFFFFFF
External device		
	1 GB	0xA0000000
		0x9FFFFFFF
External RAM		
	1 GB	0x60000000
		0x5FFFFFFF
Peripherals		
	0.5 GB	0x40000000
		0x3FFFFFFF
SRAM		
	0.5 GB	0x20000000
		0x1FFFFFFF
Code		
	0.5 GB	0x00000000

Bus Connections

Boundary address	Peripheral	Bus
0x4002 3000 - 0x4002 33FF	CRC	
0x4002 2400 - 0x4002 2FFF	Reserved	
0x4002 2000 - 0x4002 23FF	Flash memory interface	
0x4002 1400 - 0x4002 1FFF	Reserved	AHB
0x4002 1000 - 0x4002 13FF	Reset and clock control RCC	
0x4002 0400 - 0x4002 0FFF	Reserved	
0x4002 0000 - 0x4002 03FF	DMA1	
0x4001 4C00 - 0x4001 FFFF	Reserved	
0x4001 4800 - 0x4001 4BFF	TIM17 timer	
0x4001 4400 - 0x4001 47FF	TIM16 timer	
0x4001 4000 - 0x4001 43FF	TIM15 timer	
0x4001 3C00 - 0x4001 3FFF	Reserved	
0x4001 3800 - 0x4001 3BFF	USART1	
0x4001 3400 - 0x4001 37FF	Reserved	
0x4001 3000 - 0x4001 33FF	SPI1	
0x4001 2C00 - 0x4001 2FFF	TIM1 timer	
0x4001 2800 - 0x4001 2BFF	Reserved	APB2
0x4001 2400 - 0x4001 27FF	ADC1	
0x4001 1C00 - 0x4001 23FF	Reserved	
0x4001 1800 - 0x4001 1BFF	GPIO Port E	
0x4001 1400 - 0x4001 17FF	GPIO Port D	
0x4001 1000 - 0x4001 13FF	GPIO Port C	
0x4001 0C00 - 0x4001 0FFF	GPIO Port B	
0x4001 0800 - 0x4001 0BFF	GPIO Port A	
0x4001 0400 - 0x4001 07FF	EXTI	
0x4001 0000 - 0x4001 03FF	AFIO	

Boundary address	Peripheral	Bus
0x4000 7C00 - 0x4000 FFFF	Reserved	
0x4000 7800 - 0x4000 7BFF	CEC	
0x4000 7400 - 0x4000 77FF	DAC	
0x4000 7000 - 0x4000 73FF	Power control PWR	
0x4000 6C00 - 0x4000 6FFF	Backup registers (BKP)	
0x4000 5C00 - 0x4000 6BFF	Reserved	
0x4000 5800 - 0x4000 5BFF	I2C2	
0x4000 5400 - 0x4000 57FF	I2C1	
0x4000 4C00 - 0x4000 53FF	Reserved	
0x4000 4800 - 0x4000 4BFF	USART3	
0x4000 4400 - 0x4000 47FF	USART2	
0x4000 3C00 - 0x4000 3FFF	Reserved	APB1
0x4000 3800 - 0x4000 3BFF	SPI2	
0x4000 3400 - 0x4000 37FF	Reserved	
0x4000 3000 - 0x4000 33FF	Independent watchdog (IWDG)	
0x4000 2C00 - 0x4000 2FFF	Window watchdog (WWDG)	
0x4000 2800 - 0x4000 2BFF	RTC	
0x4000 1800 - 0x4000 27FF	Reserved	
0x4000 1400 - 0x4000 17FF	TIM7 timer	
0x4000 1000 - 0x4000 13FF	TIM6 timer	
0x4000 0C00 - 0x4000 0FFF	Reserved	
0x4000 0800 - 0x4000 0BFF	TIM4 timer	
0x4000 0400 - 0x4000 07FF	TIM3 timer	
0x4000 0000 - 0x4000 03FF	TIM2 timer	

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