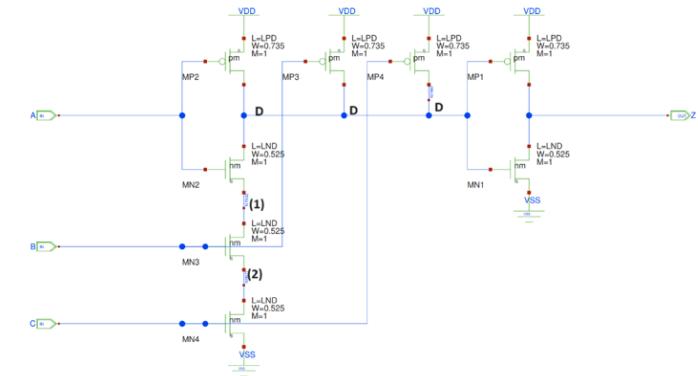
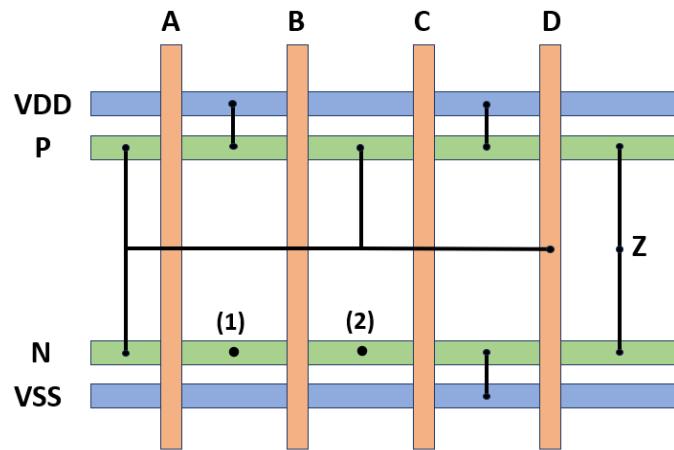


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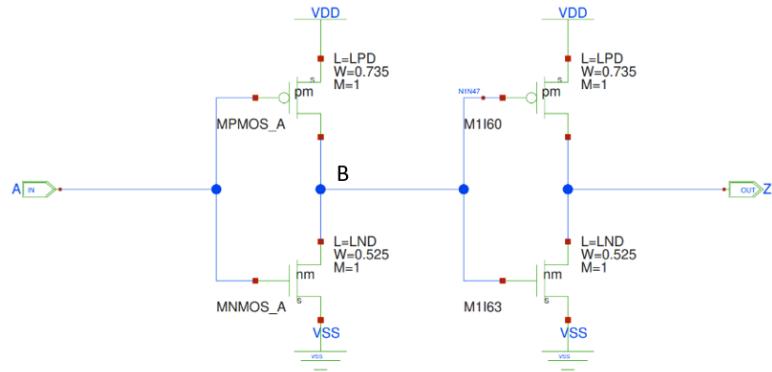


pMOS: $D \rightarrow A \xrightarrow{VDD} B \xrightarrow{D} C \xrightarrow{VDD} D \xrightarrow{Z}$

dti_55g_10t_and3x1.pdf



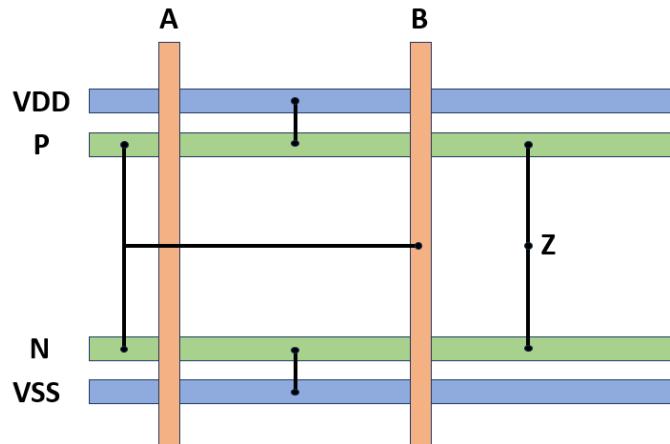
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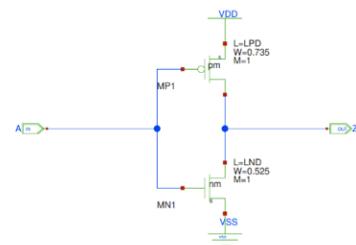
pMOS: B -----> A -----> VDD -----> Z ----->

nMOS: B -----> VSS -----> A -----> B ----->

dti_55g_10t_bufx1.pdf

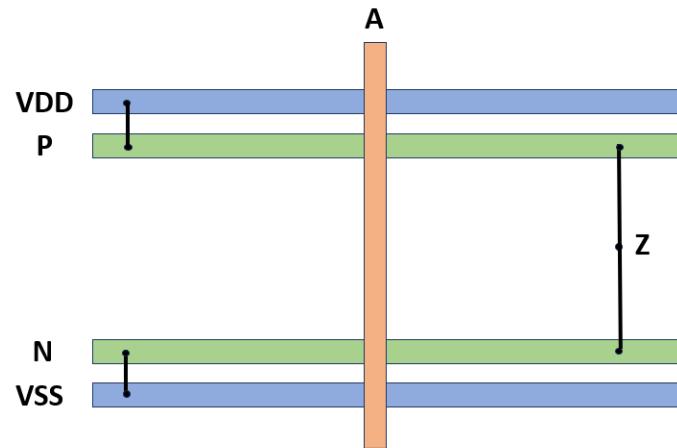


dti_55g_10t_invx1.pdf

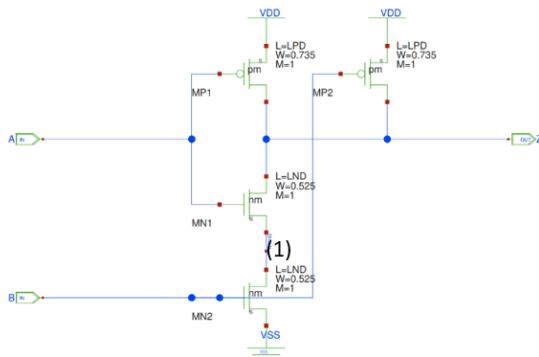


pMOS: VDD -----> A -----> Z
nMOS: VSS -----> A -----> Z

dti_55g_10t_invx1.pdf



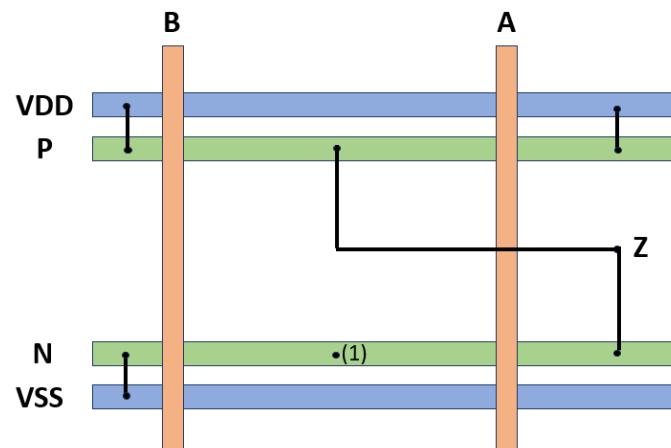
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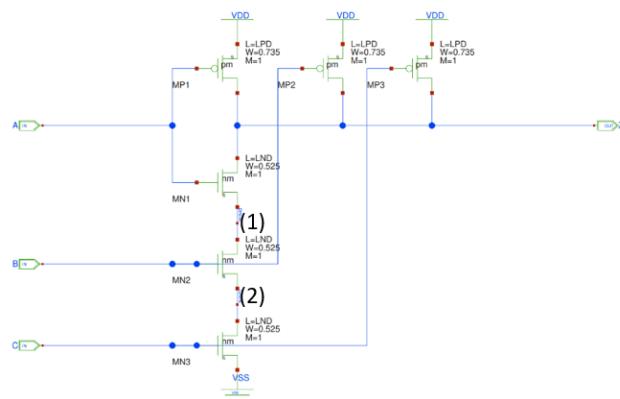
pMOS: $VDD \rightarrow B \rightarrow Z \rightarrow A \rightarrow VDD$

nMOS: $VSS \rightarrow B \rightarrow (1) \rightarrow Z \rightarrow A \rightarrow VSS$

dti_55g_10t_nand2x1.pdf



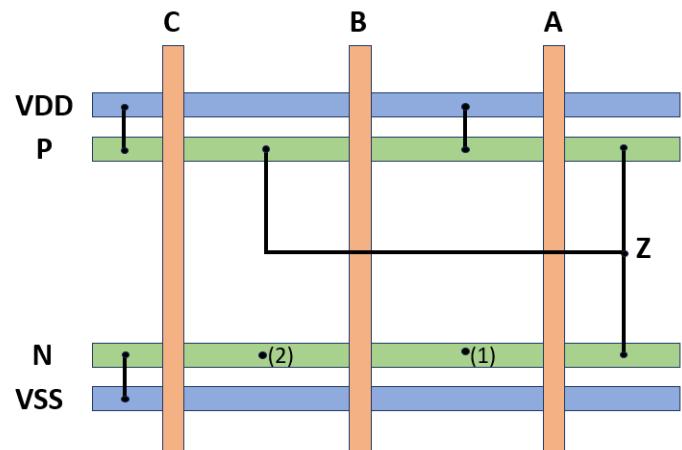
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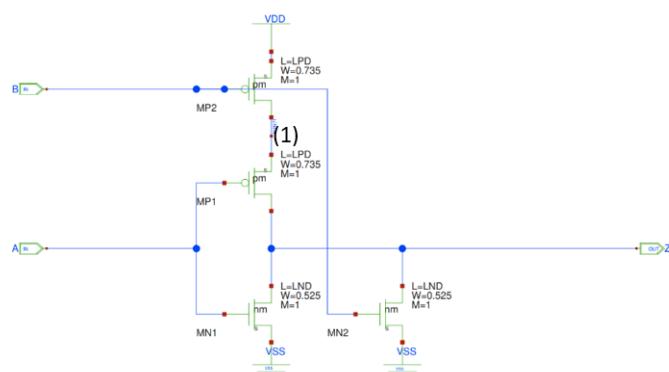
pMOS: $VDD \rightarrow C \rightarrow Z \rightarrow B \rightarrow VDD \rightarrow A \rightarrow Z \rightarrow$

nMOS: $VSS \rightarrow C \rightarrow (2) \rightarrow B \rightarrow (1) \rightarrow A \rightarrow Z \rightarrow$

dti_55g_10t_nand3x1.pdf



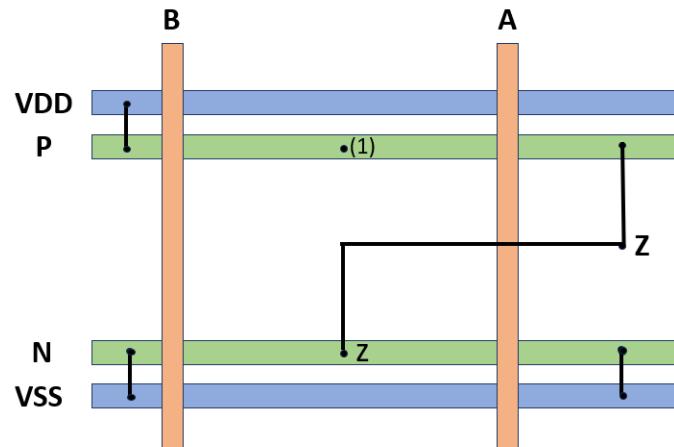
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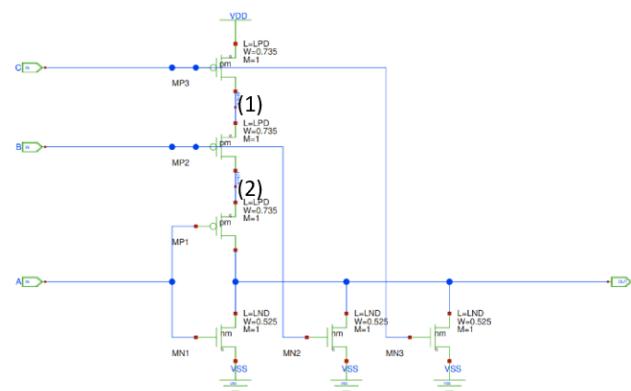
pMOS: $VDD \rightarrow B \xrightarrow{(1)} A \rightarrow Z$

nMOS: $VSS \rightarrow B \xrightarrow{Z} A \rightarrow VSS$

dti_55g_10t_nor2x1.pdf



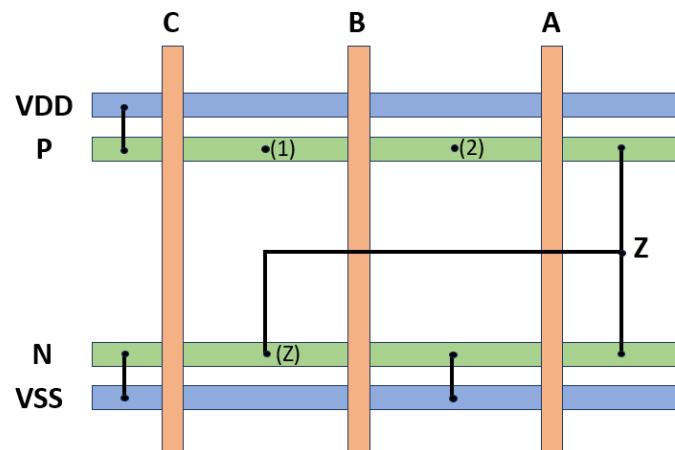
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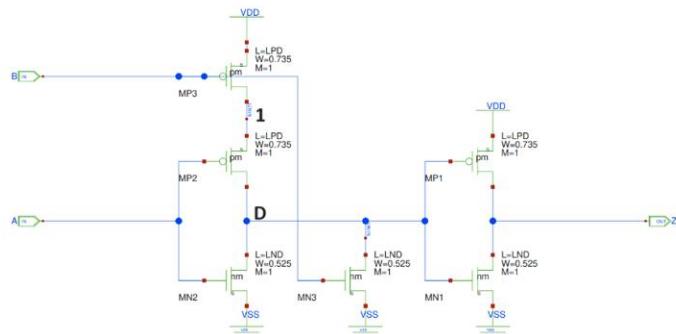
pMOS: $VDD \rightarrow C \xrightarrow{(1)} B \xrightarrow{(2)} A \rightarrow Z$

nMOS: $VSS \rightarrow C \xrightarrow{Z} B \xrightarrow{VSS} A \xrightarrow{Z} VSS$

dti_55g_10t_nor3x1.pdf



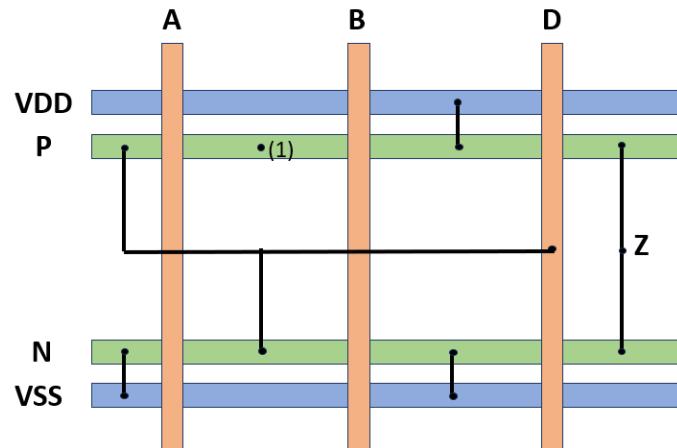
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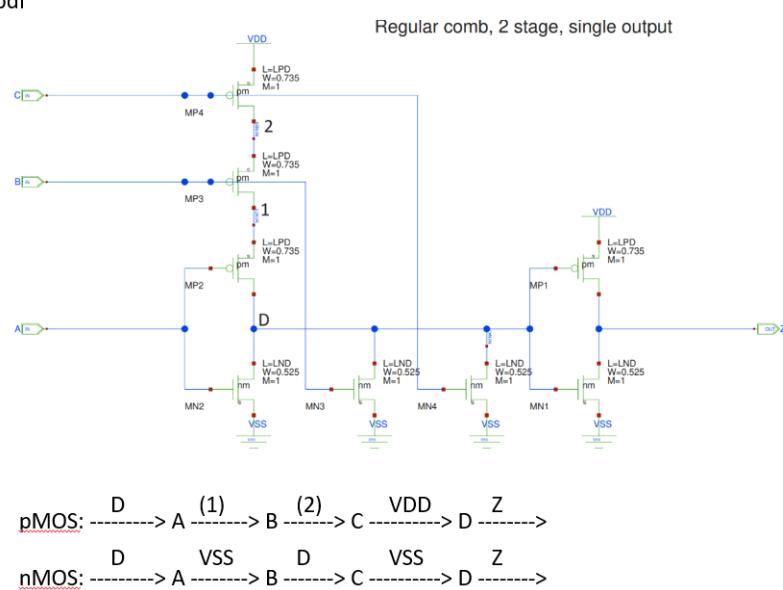
pMOS: $D \xrightarrow{(1)} A \xrightarrow{VDD} B \xrightarrow{D} Z \xrightarrow{\dots}$

nMOS: $VSS \xrightarrow{A} D \xrightarrow{VSS} B \xrightarrow{D} Z \xrightarrow{\dots}$

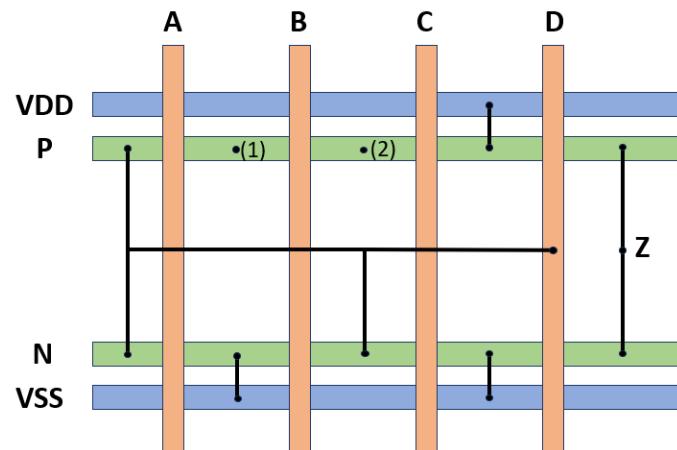
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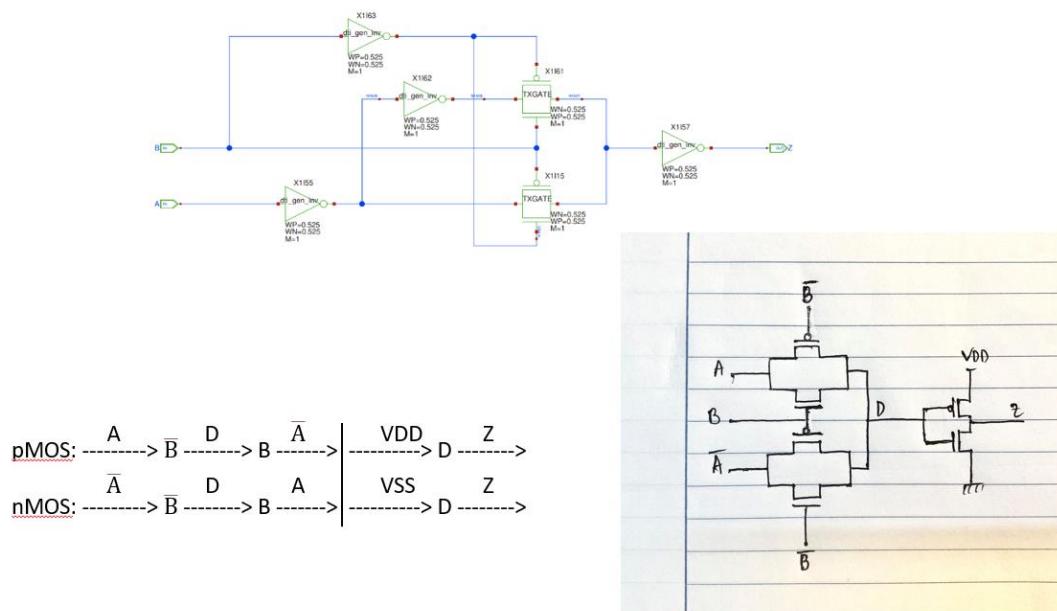
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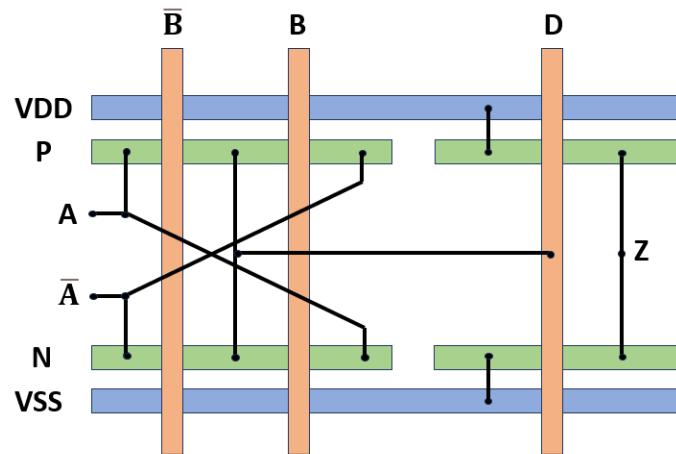
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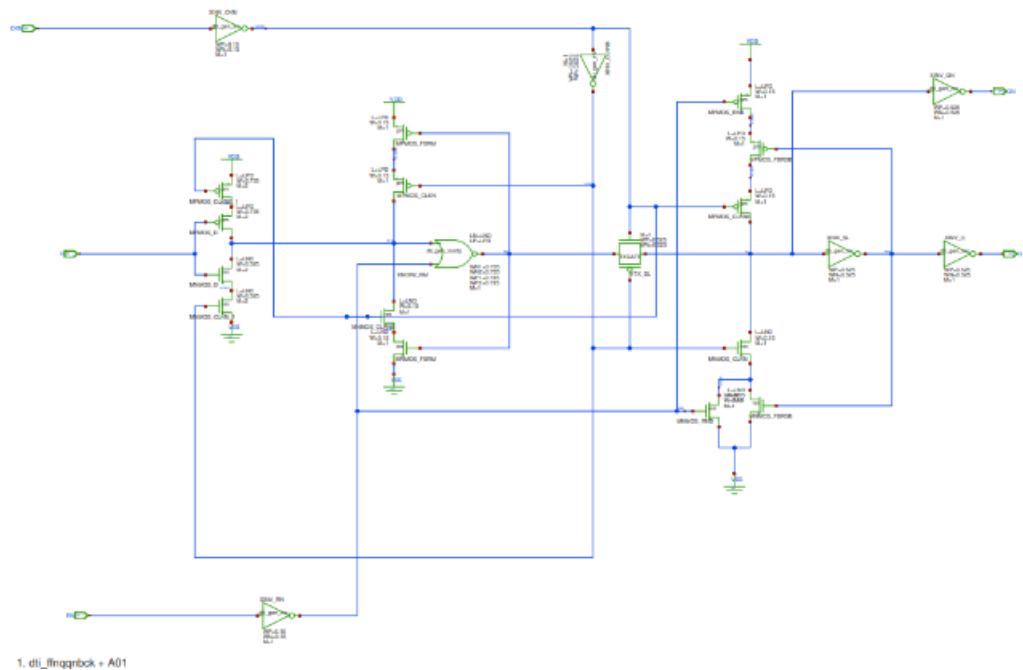


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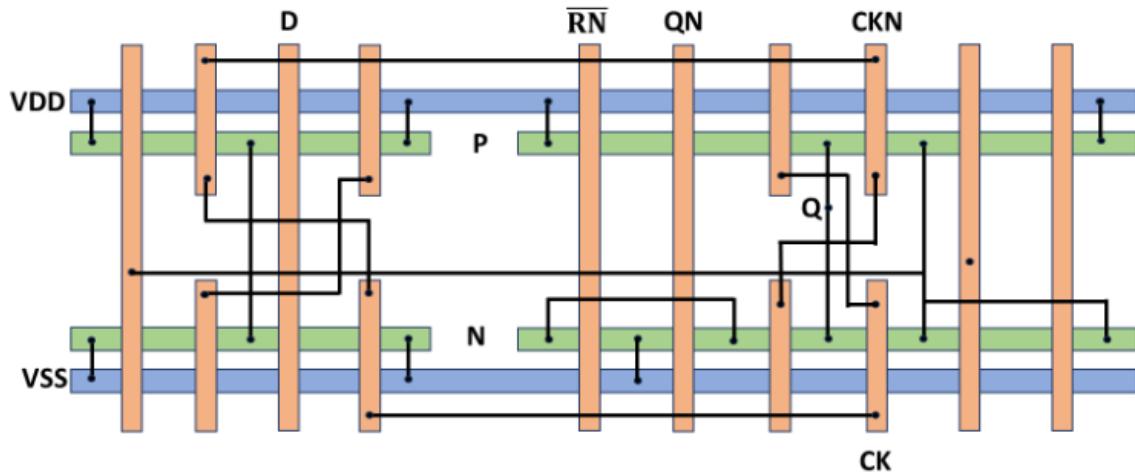
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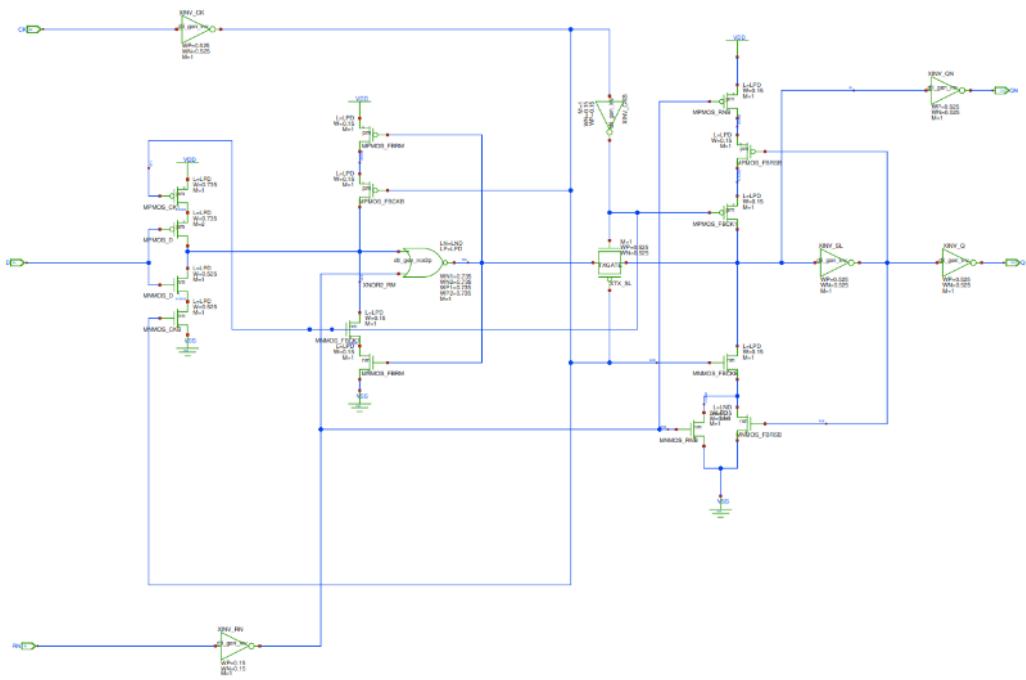




1. dti_ffnqnbck + A01

dti_55g_10t_ffnqqnbcka01x1.pdf





1. See dti_ffqnbck + A01 option

dti_55g_10t_ffqnbcka01x1.pdf

