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Class Group: COMP1DX

Lab 7 – Decoders and Multiplexers

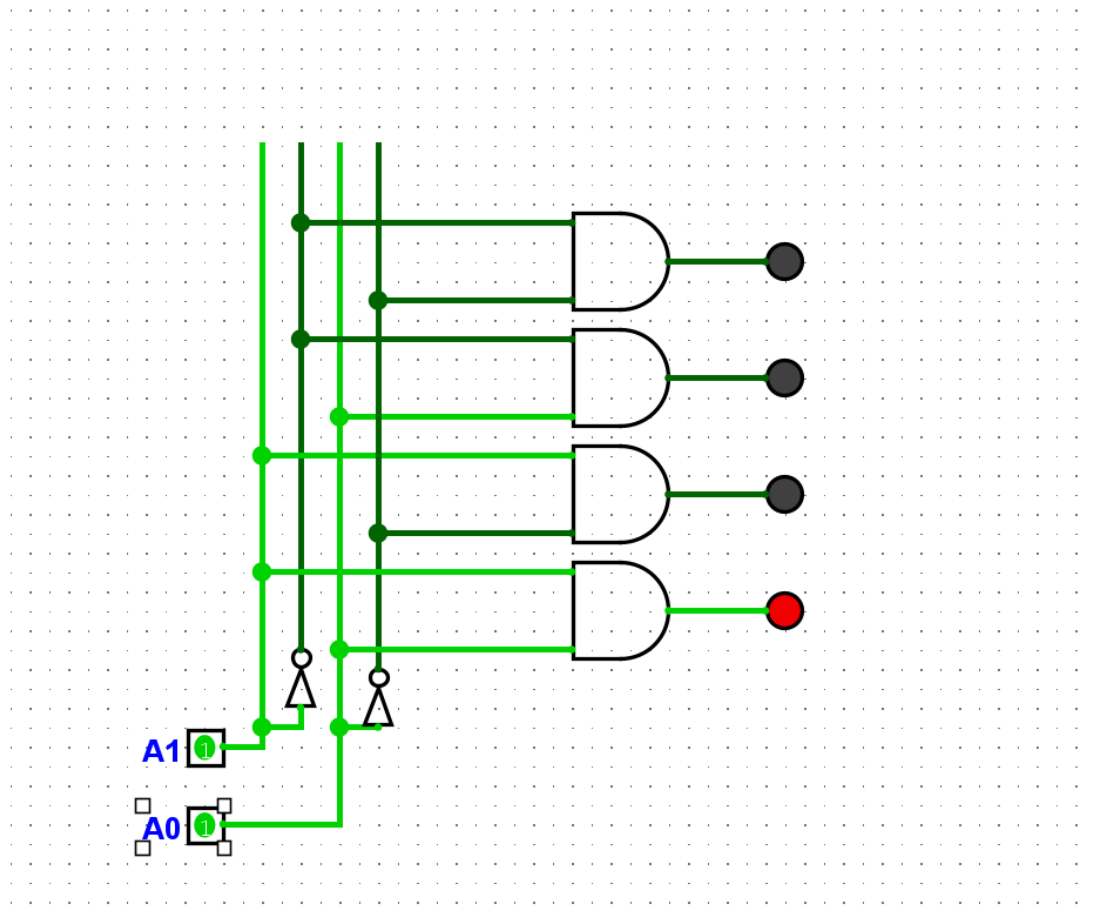
1. Complete the following truth table for a binary decoder:

Truth Table:

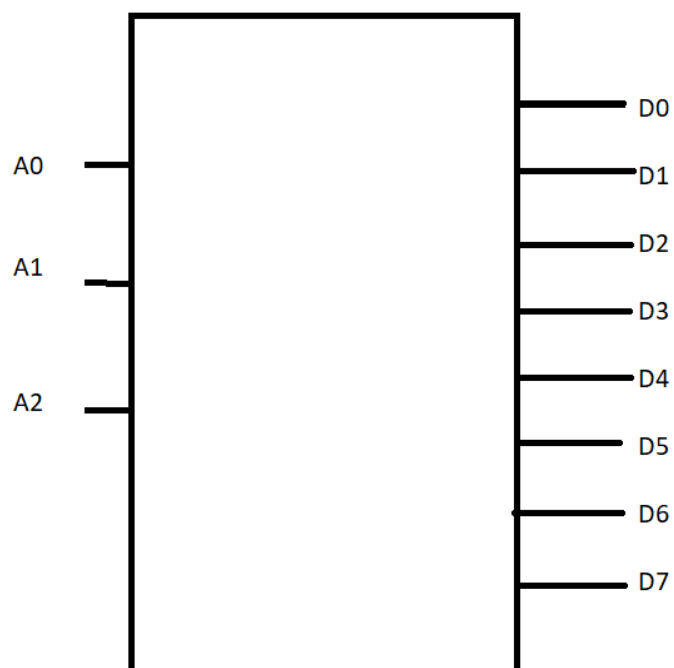
A ₁	A ₀	D ₀	D ₁	D ₂	D ₃	Product of Terms
0	0	1	0	0	0	$D_0 = A_1 'A_0'$
0	1	0	1	0	0	$D_1 = A_1 'A_0'$
1	0	0	0	1	0	$D_2 = A_1 A_0'$
1	1	0	0	0	1	$D_3 = A_1 A_0$

2. Design a circuit which implements the binary decoder outlined in the truth table above. Verify its operation using the simulator and paste a snapshot of your circuit below.

Circuit:



3. Draw the black box representation and complete the truth table for a 3-to-8 binary decoder:

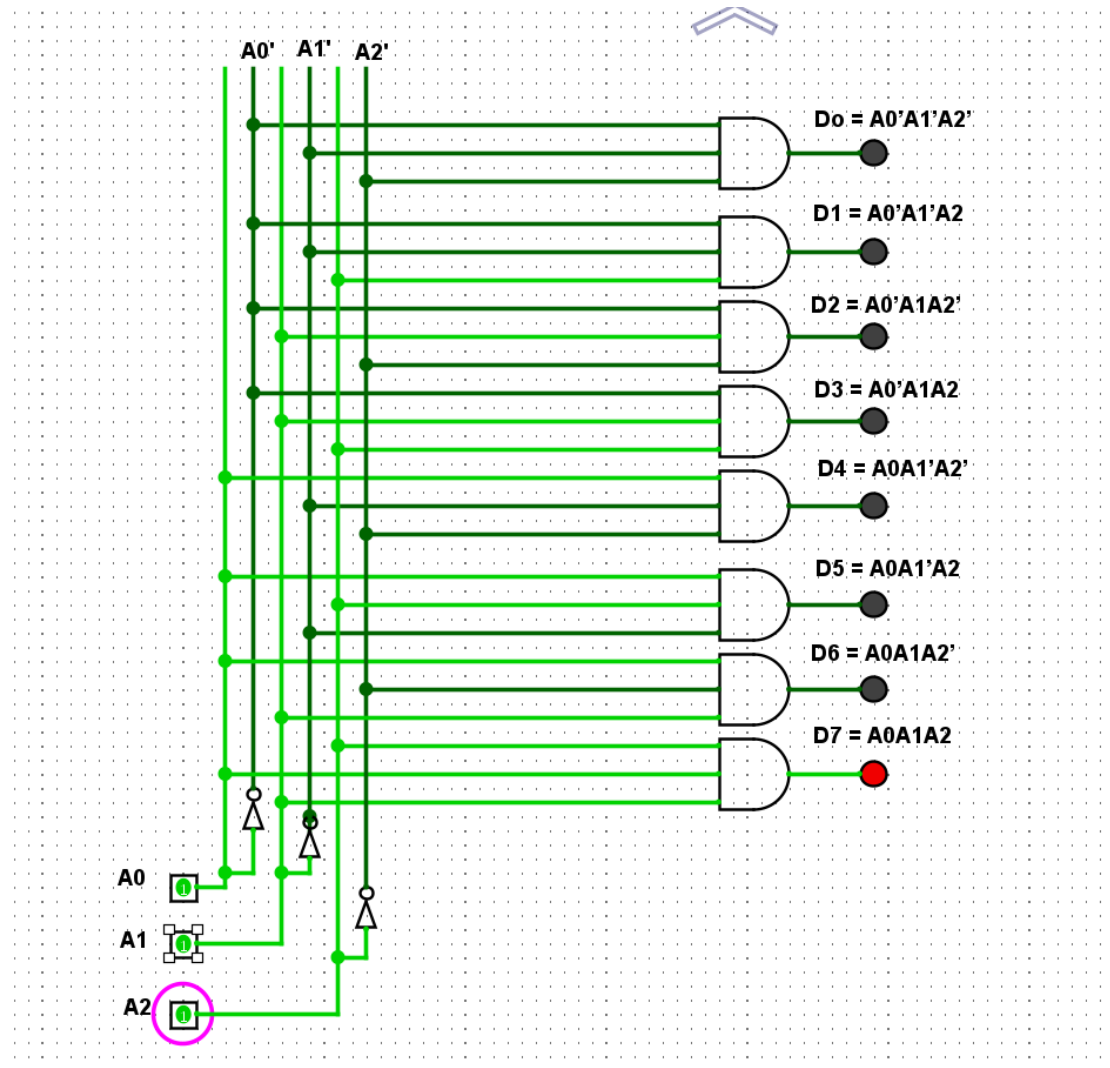


A0	A1	A2	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

4. Design a circuit which implements the 3-to-8 binary decoder outlined in the truth table from Q.3. Verify its operation using the simulator and paste a snapshot of your circuit below.

Circuit:

$$\begin{array}{llll} D_0 = A_0'A_1'A_2' & D_1 = A_0'A_1'A_2 & D_2 = A_0'A_1A_2' & D_3 = A_0'A_1A_2 \\ D_4 = A_0A_1'A_2' & D_5 = A_0A_1'A_2 & D_6 = A_0A_1A_2' & D_7 = A_0A_1A_2 \end{array}$$



5. Complete the following truth table for a multiplexer.

Truth Table:

S_1	S_0	I_0	I_1	I_2	I_3	Output	Product of Terms
0	0	0	x	x	x	M0	
0	1	x	0	x	x	M1	
1	0	x	x	0	x	M2	
1	1	x	x	x	0	M3	
0	0	1	x	x	x	M4	$S_1'S_2'I_0$
0	1	x	1	x	x	M5	$S_1'S_2'I_0$
1	0	x	x	1	x	M6	$S_1S_2'I_0$
1	1	x	x	x	1	M7	$S_1S_2'I_0$

6. Design a circuit which implements the multiplexer outlined in the truth table above. Verify its operation using the simulator and paste a snapshot of your circuit below.

Circuit:

