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Class Group: COMP1D-X

Lab 9 – Latches and Memory

1.

Describe, using your own words, a D Latch. Illustrate how it is implemented below and confirm its operation using the simulator. Draw its truth table.

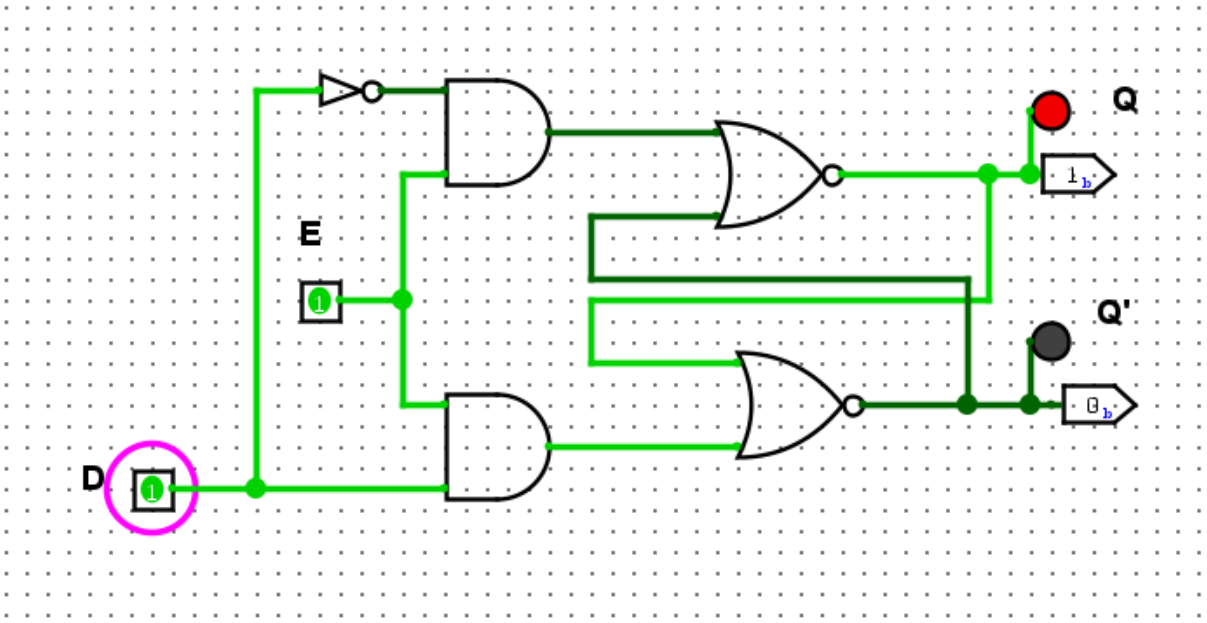
Description:

A D latch, also known as a data latch or transparent latch, is a digital circuit that stores one bit of information. It has a data input (D), a enable input (E), and two outputs: Q and Q' (the complement of Q). When the enable signal is active, the input data is transferred to the output. Here's a basic truth table scenario of how a D latch works:

Truth Table:

E	D	Qt+1
0	0	Qt
0	1	Qt
1	0	0
1	1	1

Circuit:



2.

Show a circuit which can be used to write to a 4x5 memory.

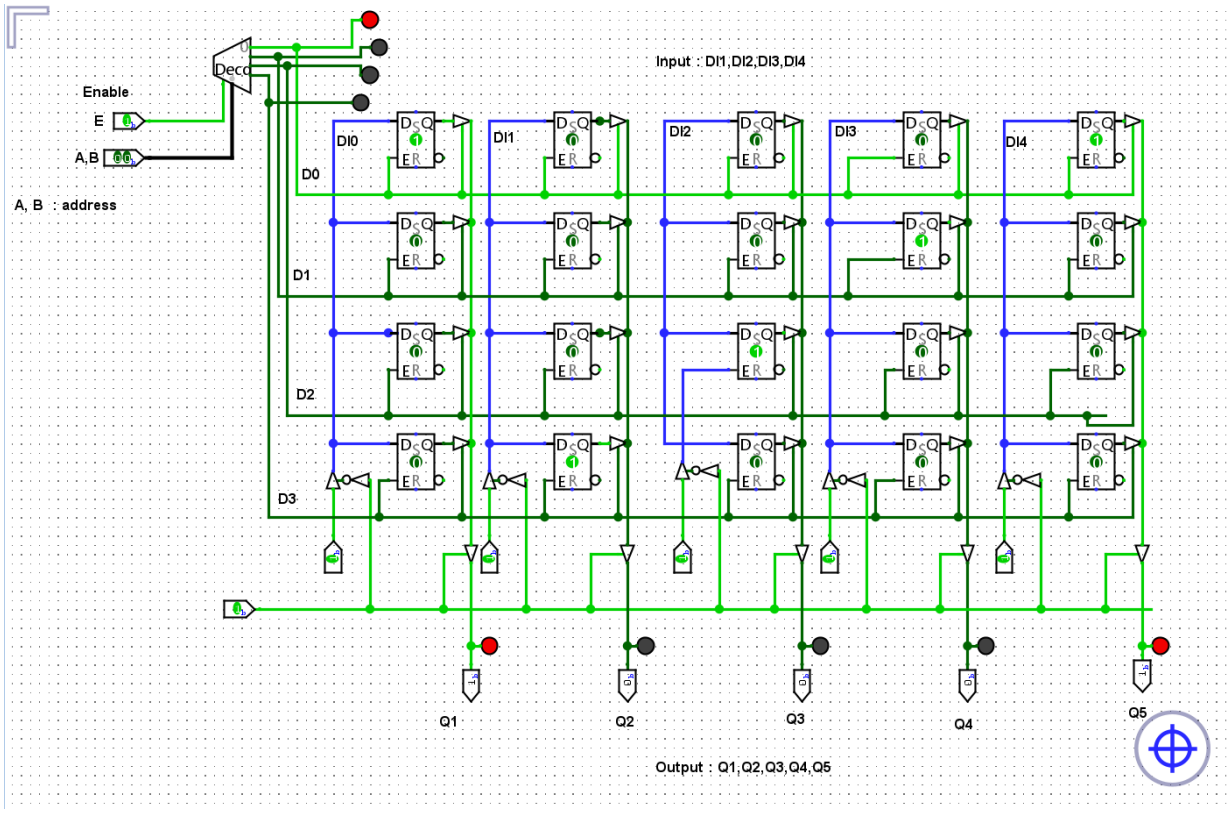
Illustrate how it is implemented below and confirm its operation using the simulator.

(You may use the blackbox decoder in Logisim).

Description:

In Logisim, create a 4x5 memory array and designate individual output pins for each cell. Introduce input pins for the 2-bit address lines (A,B), the 4-bit data lines (D0, D1, D2, D3), and the write enable signal (E). Connect the decoder outputs to the respective row and column select lines of the memory array. Utilize logic gates to generate write signals for each memory cell based on the decoder outputs and the write enable signal. Connect the data lines to the memory array's data inputs, the address lines to the decoders, and the write enable signal to the write logic. Introduce a enable signal to control the memory cells, and simulate the circuit in Logisim, observing the changes in memory cell outputs based on different address, data, and write enable inputs to confirm the correct functionality of the write operation.

Circuit:


Deco
Enable
E
A,B
A, B : address
Input : DI1,DI2,DI3,DI4
DI0
DI1
DI2
DI3
DI4
D0
D1
D2
D3
Q1
Q2
Q3
Q4
Q5
Output : Q1,Q2,Q3,Q4,Q5