Assingnment_1

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Question_1:

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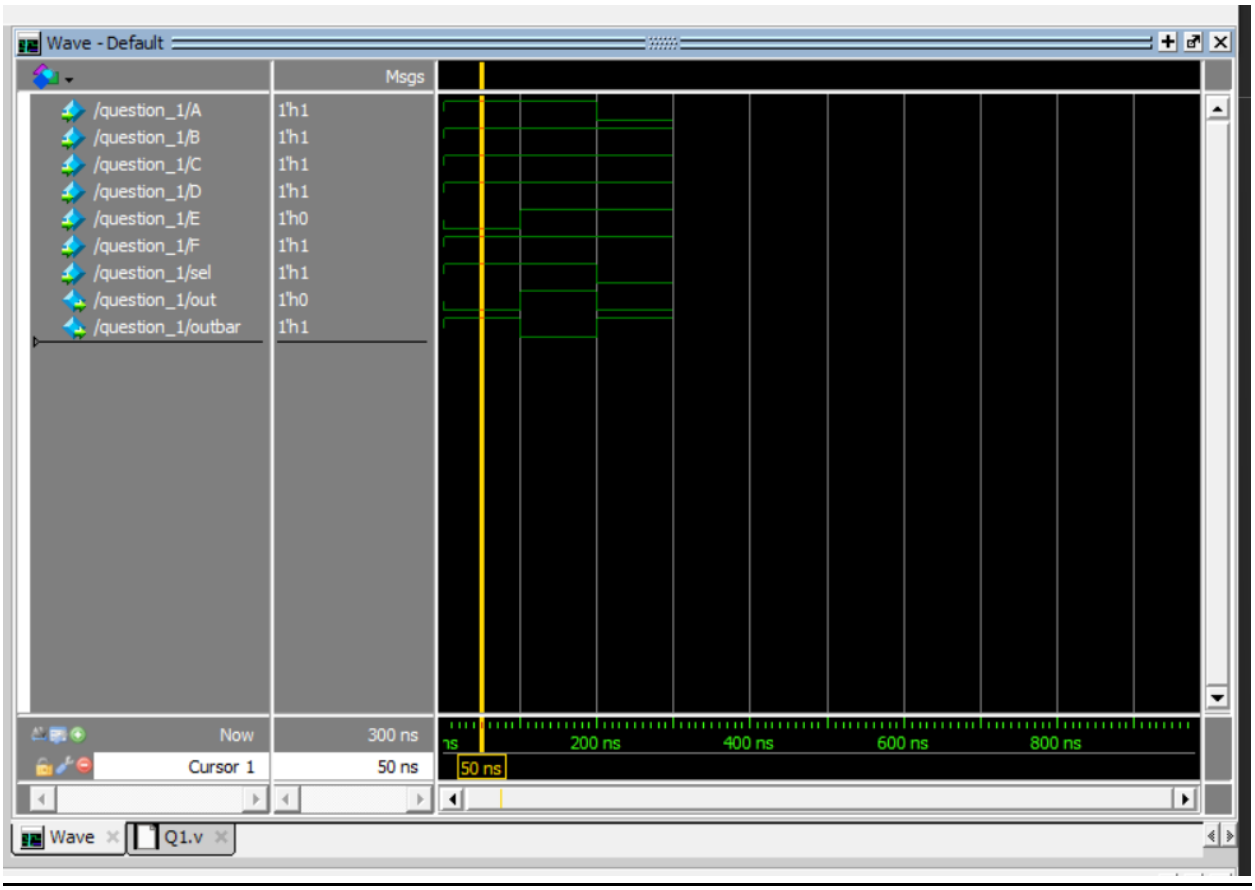
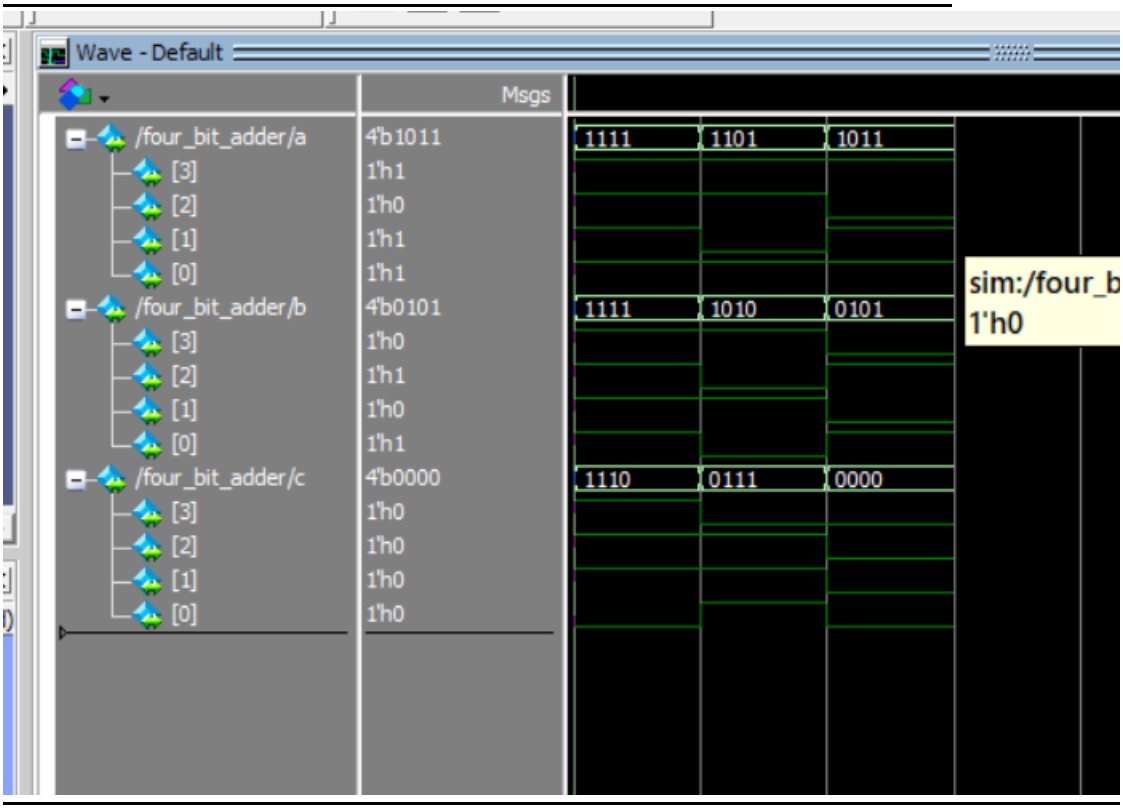
```
Ln#
1  module question_1(A,B,C,D,E,F,sel,out,outbar);
2      input A , B ,C,D,E,F,sel;
3      output out , outbar;
4      wire w1 = A & B & C;
5      wire w2 = D ~^ E ~^ F ;
6      assign out = (sel == 1) ? w2 : w1;
7      assign outbar = ~out ;
8
9  endmodule
```



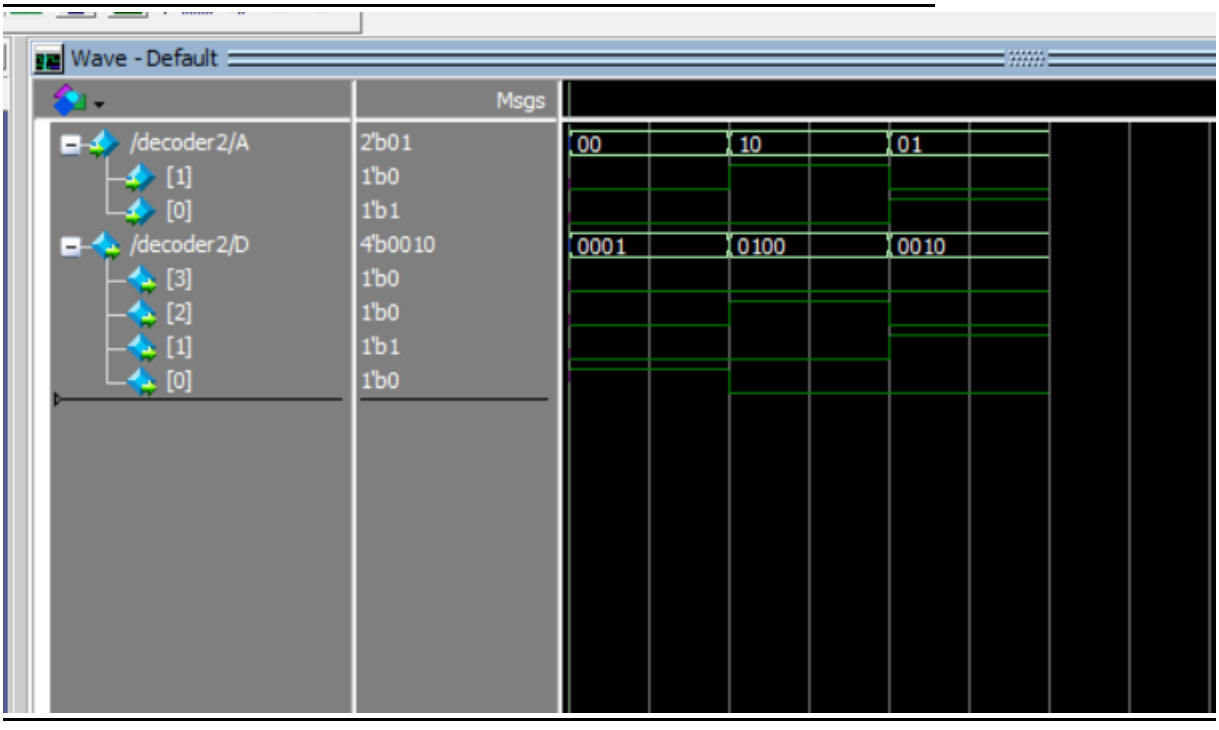
Question_2:

```
Ln#
 1  module four_bit_adder(
 2          [3:0]a,
 3          [3:0]b,
 4          [3:0]c
 5  );
 6  //assign c[0]= a[0] + b[0];
 7  //assign c[1]= a[1] + b[1]+c[0];
 8  //assign c[2]= a[2] + b[2]+c[1];
 9  assign c= a + b;
10
11  endmodule
```



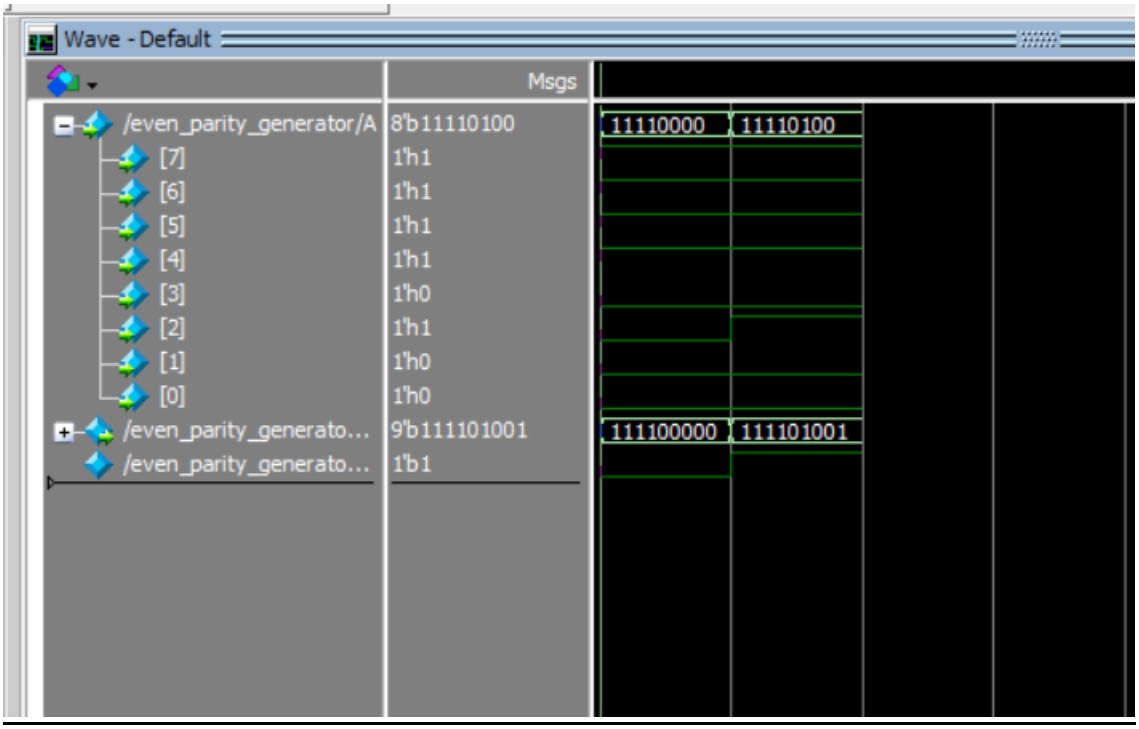
Question_3:

```
Ln#
 1  module decoder2(
 2      input [1:0] A,
 3      output [3:0] D
 4  );
 5
 6  assign D = (A == 2'b00) ? 4'b0001 :
 7             (A == 2'b01) ? 4'b0010 :
 8             (A == 2'b10) ? 4'b0100 :
 9                            4'b1000;
10
11  endmodule
12
```



Question_4:

```
1  module even_parity_generator(
2
3          input [7:0]A,
4          output [8:0]output_with_parity
5
6          );
7
8          wire parity;
9          assign parity = ^A ;
10
11         assign output_with_parity = {A,parity};
12
13
14 endmodule
```



Question_5:

```
Ln#
 7   assign C2 = (A<B) ? 1 : 0 ;
 8   assign C3 = (A==B) ? 1 : 0 ;
 9
10   endmodule*/
11
12   module comparetor(
13       input [3:0] A,
14       input [3:0] B,
15       output C1, C2, C3
16   );
17
18       assign C1 = (A > B) ? 1 : 0;
19       assign C2 = (A < B) ? 1 : 0;
20       assign C3 = (A == B) ? 1 : 0;
21
22   endmodule
```