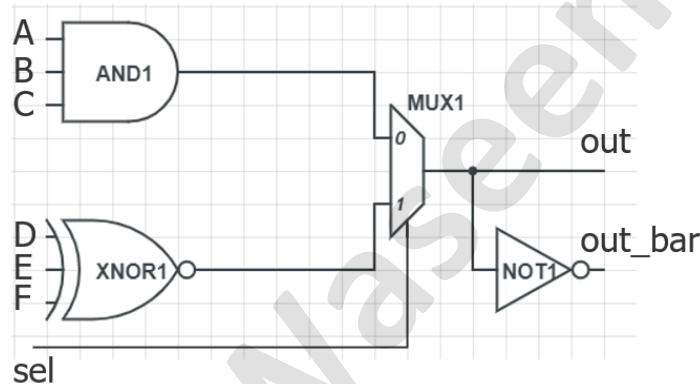


Combinational Circuit Design

Design the following circuits with Verilog using assign statements.

1)

- The design has 7 inputs and 2 outputs
- Use assign statements to design the following



2) Implement 4-bit adder using addition operator

- The design takes 2 inputs (A, B) and the summation is assigned to output (C) ignoring the carry

3) Implement 2-to-4 Decoder using **conditional operator** (A logic decoder has n input lines and 2^n output lines. Each output line corresponds to a unique combination of the input values.)

- The design has input A (2 bits) and output D (4 bits)

A ₁	A ₀	D ₃	D ₂	D ₁	D ₀
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

4) Implement an **even parity generator module**. In case you don't know what a parity bit is, please check this [link](#). The design input is a bus where a reduction operator will be used to generate the even parity bit.

- The design has 1 input A (8 bits) and 1 output **out_with_parity** (9 bit) where the parity bit calculated will be inserted in the least significant bit of the output bus and the remaining bits will be the input A (Hint: use concatenation).

5) Implement a comparator that compares 2 inputs (**A**, **B**) and has 3 outputs using conditional operator.

- The first output **A_greaterthan_B** is high only when A is greater than B
- The second output **A_equals_B** is high only when A equals B
- The third output **A_lessthan_B** is high only when A is less than B



Inputs A and B are 4-bit bus while the 3 outputs are single bits.

Deliverables: The assignment should be submitted as a PDF file with this format <your_name>_Assignment1 for example Kareem_Waseem_Assignment1

Note that your document should be organized as 5 sections corresponding to each design above, and in each section, I am expecting the Verilog code for the design, and waveform snippets forcing different input values to verify the functionality of the design.