CS303 Lab 3 – Lab Report

Part 1) Verifying Correctness

In this part, a set of tests conducted on RippleCarry and CLA circuits to verify their correctness.

Test Cases:

1)

```
//47 + 15 = 62
control = 0;
A = 47;
B = 15;
#10;
```

2)

```
//1031 + 4099 = 5130
control = 0;
A = 1031;
B = 4099;
#10;
```

3)

```
//12321 + 30123 = 42444 OVERFLOW
control = 0;
A = 12321;
B = 30123;
#10;
```

4)

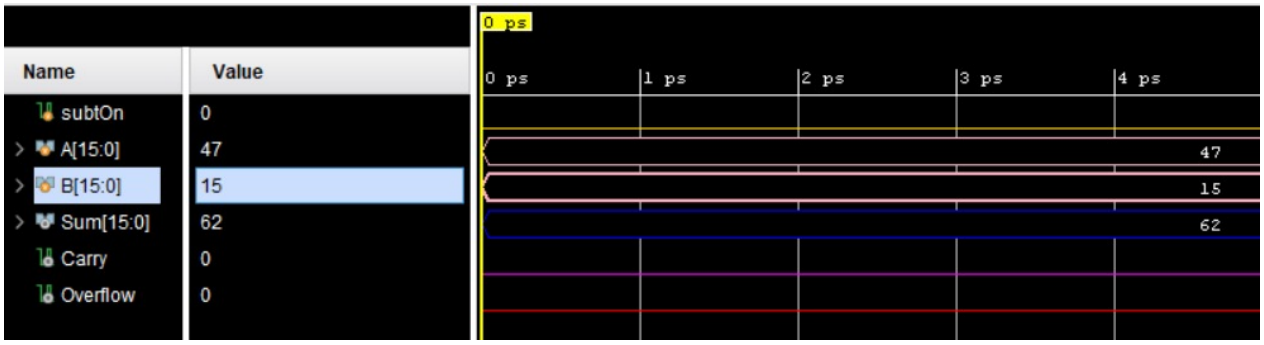
```
//1159 - 4131 = -2972
control = 1;
A = 1159;
B = 4131;
#10;
```

5)

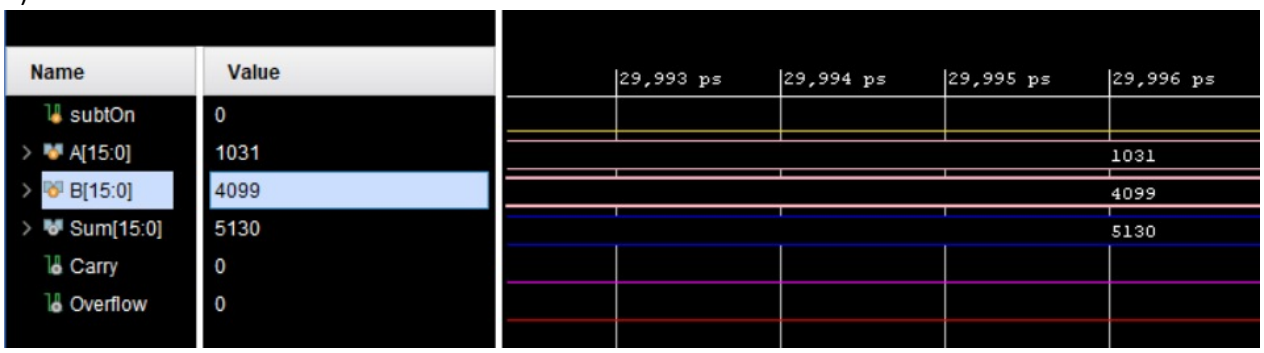
```
//(-30577) - (-28671) = -1906
control = 1;
A = -30577;
B = -28671;
#10;
```

Ripple Carry Adder/Subtractor outputs:

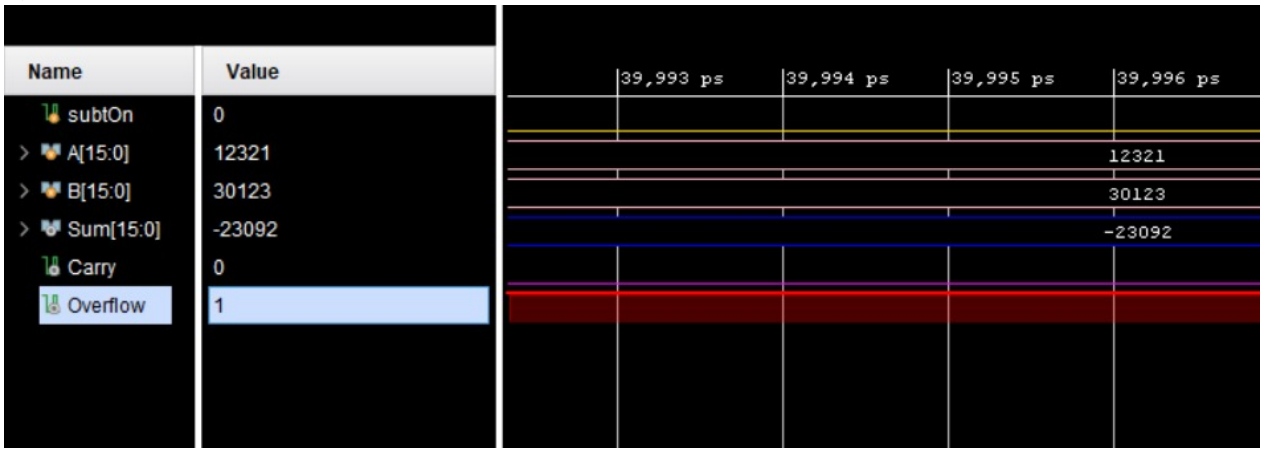
1)



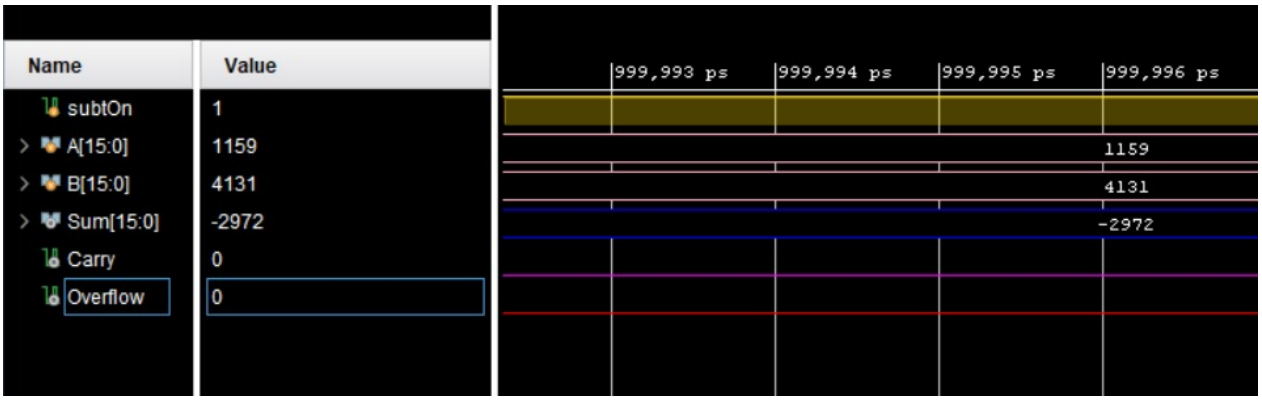
2)



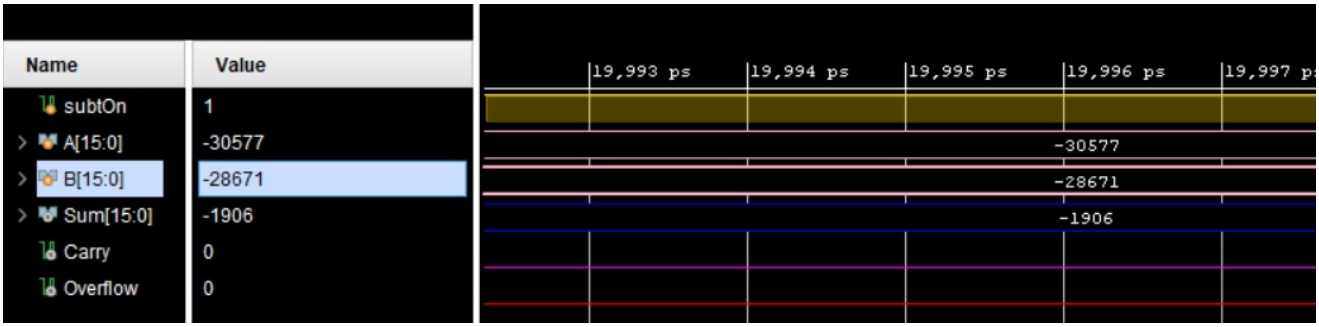
3)



4)

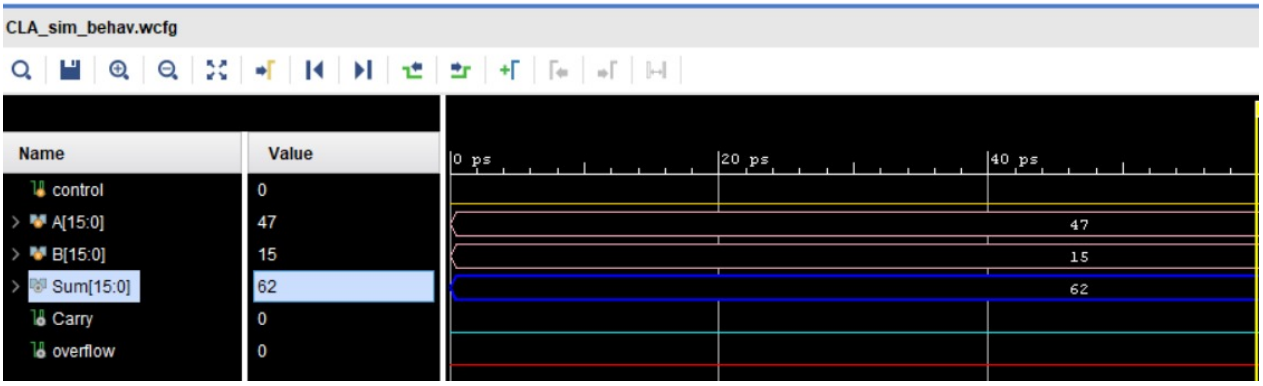


5)

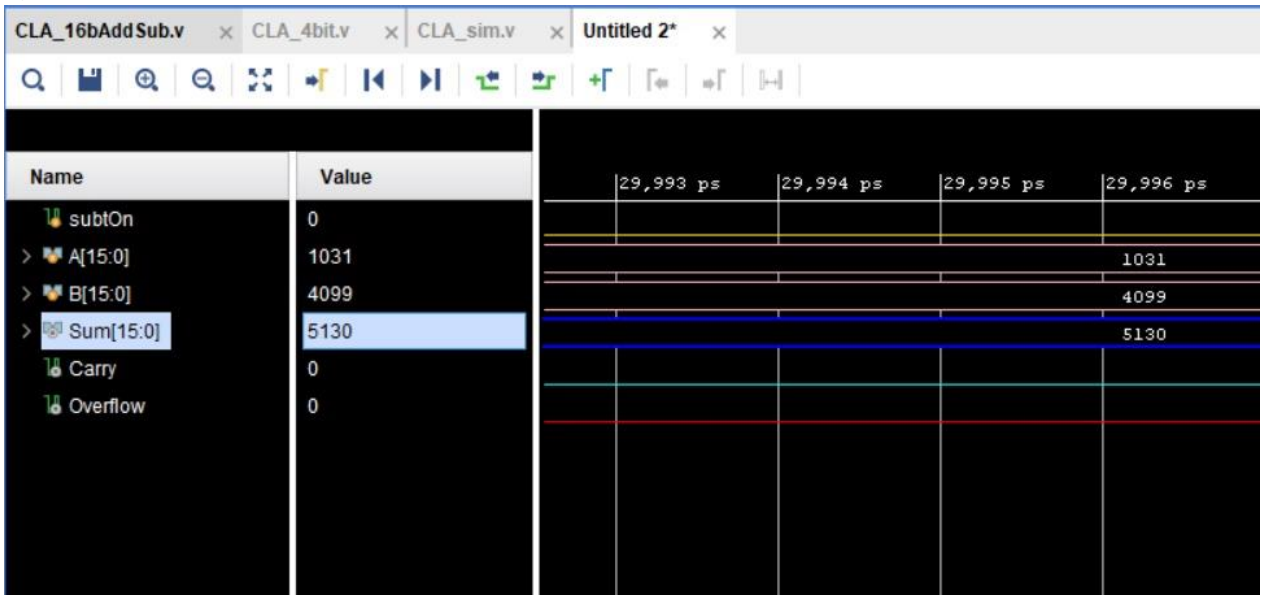


CLA Adder/Subtractor outputs:

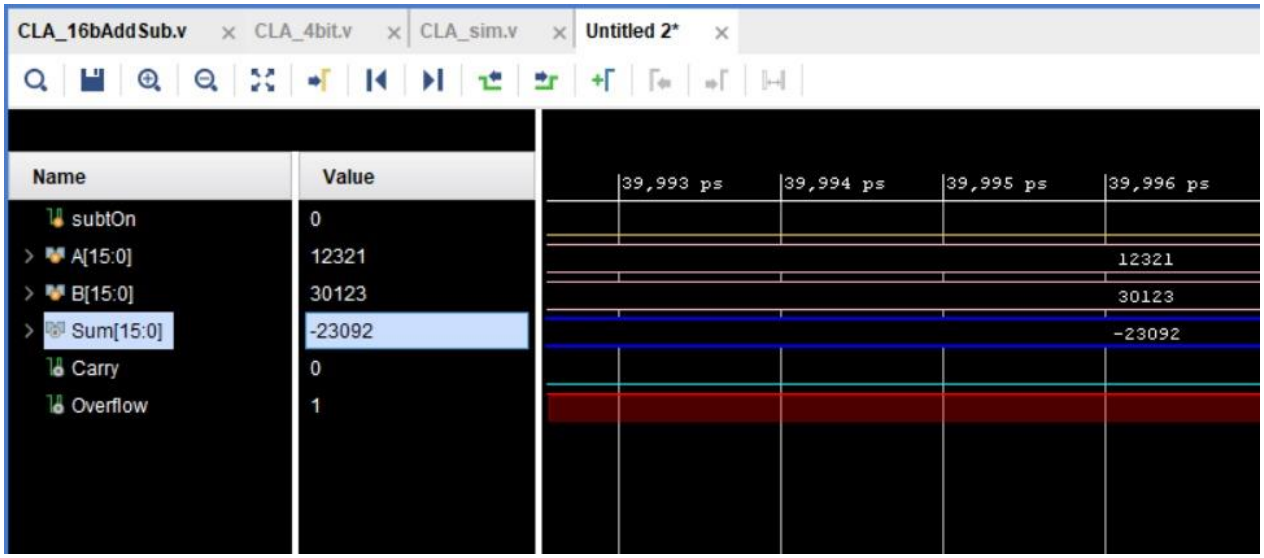
1)



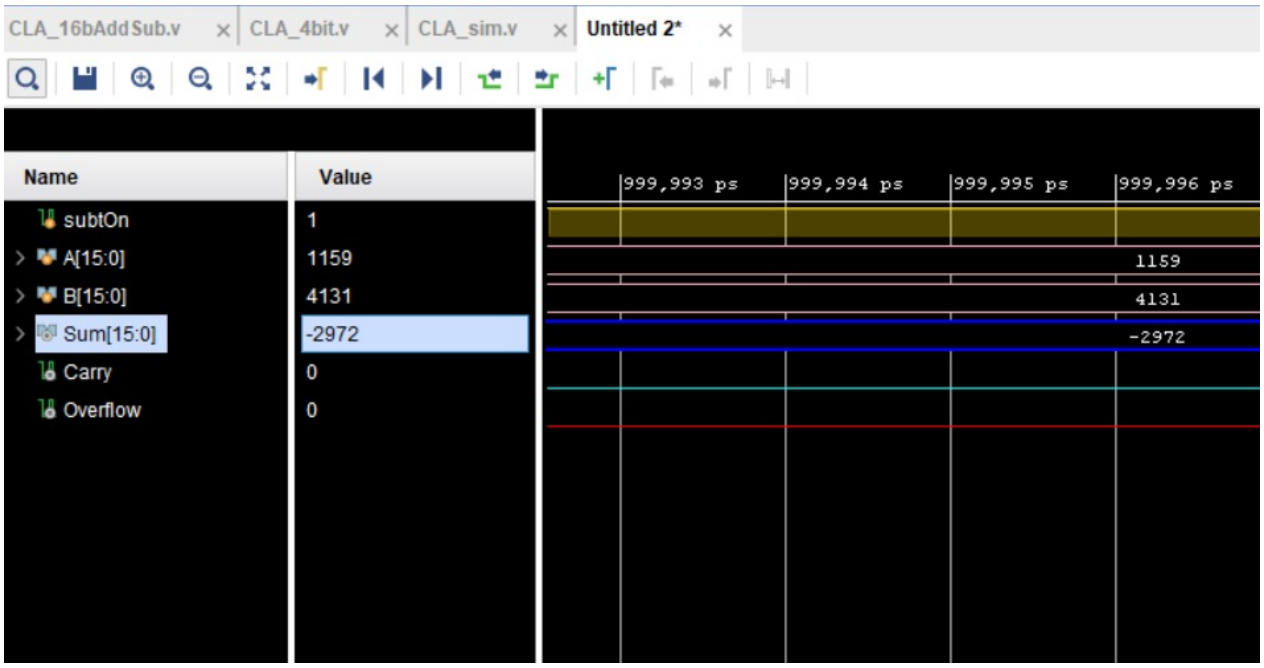
2)


CLA_16bAddSub.v
CLA_4bit.v
CLA_sim.v
Untitled 2*
Name
Value
subtOn
0
A[15:0]
1031
B[15:0]
4099
Sum[15:0]
5130
Carry
0
Overflow
0
29,993 ps
29,994 ps
29,995 ps
29,996 ps
1031
4099
5130

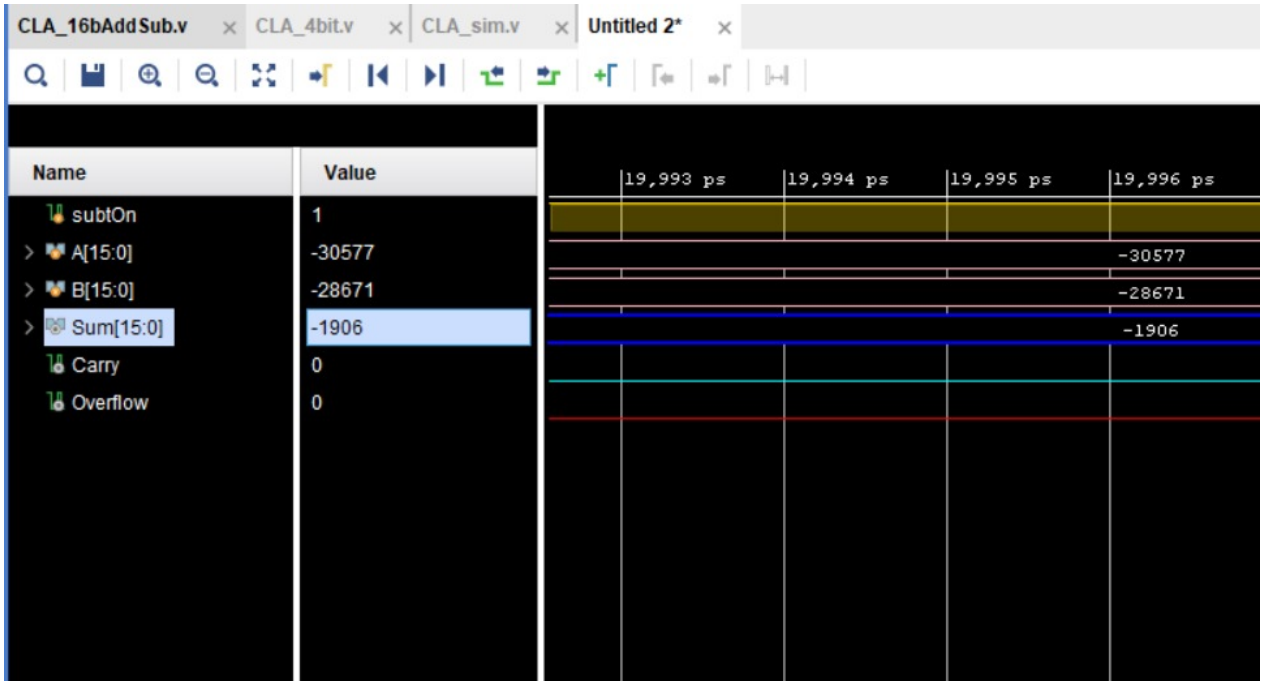
3)


CLA_16bAddSub.v
CLA_4bit.v
CLA_sim.v
Untitled 2*
Name
Value
subtOn
0
A[15:0]
12321
B[15:0]
30123
Sum[15:0]
-23092
Carry
0
Overflow
1
39,993 ps
39,994 ps
39,995 ps
39,996 ps
12321
30123
-23092

4)



5)



As it can be seen, both circuit calculates same answers which are also the correct answers. Also, they are able to detect arithmetic overflows. Therefore, now we can safely compare their performances.

Part 2) Performance Comparison Between Two Design in Terms of Area

In Digital Design, it is a fact that "Area" and "Time" are inversely proportional. Therefore, it is expected that, the Carry Lookahead Adder/Subtractor (CLA) circuit, which is design to reduce carry propagation time, will use more area than the Ripple Carry Adder/Subtractor circuit while CLA outperforms the cascaded Ripple Carry Adder/Subtractor circuit.

Both circuits "post-synthesis and post-implementation" utilization stats and "simulation run" records can be seen as follows:

Ripple Carry Adder/Subtractor:

Resource	Estimation	Available	Utilization %
LUT	24	63400	0.04
IO	51	210	24.29

Fig.1: Ripple Carry Adder/Subtractor's Post-synthesis utilization

Resource	Utilization	Available	Utilization %
LUT	24	63400	0.04
IO	51	210	24.29

Fig.2: Ripple Carry Adder/Subtractor's Post-implementation utilization

```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'ripple_sim_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:08 ; elapsed = 00:00:10 . Memory (MB): peak = 775.668 ; gain = 17.102
```

Fig.3: Ripple Carry Adder/Subtractor's simulation run record

Carry Lookahead Adder/Subtractor:

Resource	Estimation	Available	Utilization %
LUT	33	63400	0.05
IO	51	210	24.29

Fig.4: Carry Lookahead Adder/Subtractor's Post-synthesis utilization

Resource	Utilization	Available	Utilization %
LUT	33	63400	0.05
IO	51	210	24.29

Fig.5: Carry Lookahead Adder/Subtractor's Post-synthesis utilization

```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'CLA_sim_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:03 ; elapsed = 00:00:07 . Memory (MB): peak = 1712.402 ; gain = 0.000
```

Fig.6: Carry Lookahead Adder/Subtractor's simulation run record

As can be observed in figures 1-2 and 3-4, CLA uses ~25% more area than Ripple Carry Adder/Subtractor therefore, Ripple Carry Adder/Subtractor circuit outperforms CLA in terms of "area" utilization. Also, as can be seen in figures 3 and 6, CLA requires much more memory than the Ripple Carry Adder/Subtractor circuit which may be another indicator that Ripple Carry Adder/Subtractor outperforms CLA in terms of area performance.

On the other hand, figures 3 and 6 clearly indicates that CLA runs much faster than the Ripple Carry Adder/Subtractor circuit in CPU time. Therefore, it can be said that CLA outperforms Ripple Carry Adder/Subtractor circuit in terms of the time performance.

Consequently, while in terms of **area** Ripple Carry Adder/Subtractor circuit is better than CLA, in terms of **time** CLA is better than Ripple Carry Adder/Subtractor circuit.