Operating System

Revision 4 - General

Process scheduling

1. Consider the following five processes each having its own unique burst time and arrival time. Apply SJF non-preemptive and preemptive.

Process Queue	Burst time	Arrival time
P1	6	2
P2	2	5
P3	8	1
P4	3	0
P5	4	4

Solution:

Non-Preemptive, Average wait time ➔ 5.2

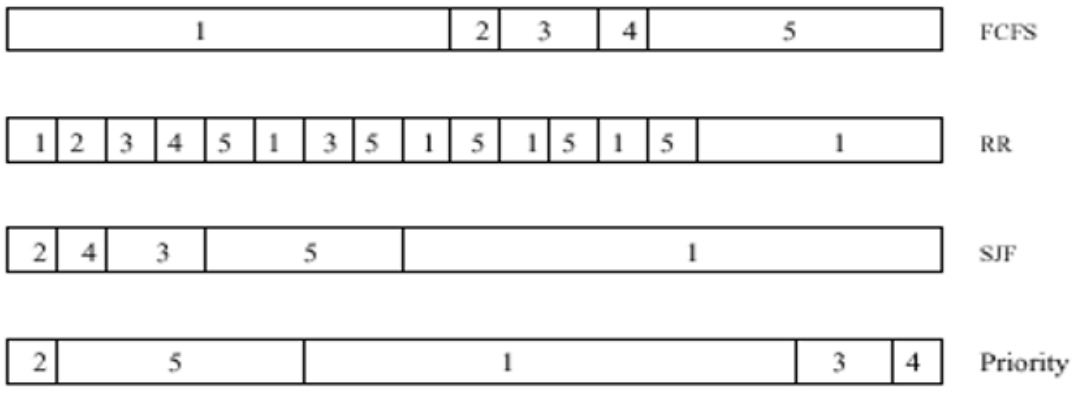
Non-preemptive JF, average wait time ➔ 4.6

2. Consider the following set of processes, with the length of the CPU-burst time given in milliseconds:

Process	Burst Time	Priority
P_1	10	3
P_2	1	1
P_3	2	3
P_4	1	4
P_5	5	2

The processes are assumed to have arrived in the order P1, P2, P3, P4, P5, all at time 0.

a. Draw four Gantt charts illustrating the execution of these processes using FCFS, SJF,a nonpreemptive priority (a smaller priority number implies a higher priority), and RR (quantum = 1) scheduling.



b. What is the turnaround time of each process for each of the scheduling algorithms in part a?

	FCFS	RR	SJF	Priority
P_1	10	19	19	16
P_2	11	2	1	1
P_3	13	7	4	18
P_4	14	4	2	19
P_5	19	14	9	6

c. What is the waiting time of each process for each of the scheduling algorithms in part a?

	FCFS	RR	SJF	Priority
P_1	0	9	9	6
P_2	10	1	0	0
P_3	11	5	2	16
P_4	13	3	1	18
P_5	14	9	4	1

d. Which of the schedules in part a results in the minimal average waiting time (over all processes)?

3. What is the average turnaround time for the following processes using

a) FCFS (10.53)

b) SJF non-preemptive (10.53)

c) Preemptive SJF. (7.6)

Process	Arrival Time	Burst Time
P1	0.0	8
P2	0.4	4
P3	1.0	1

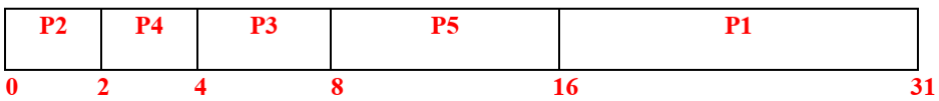
4. Consider five processes P1, P2, P3, P4 and P5 with the following Process Burst Times and Priorities:

	Process Burst	Priority
P_1	15	2
P_2	2	0
P_3	4	2
P_4	2	3
P_5	8	1

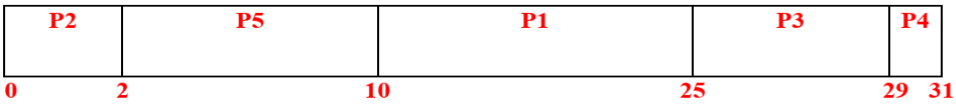
The processes are assumed to have arrived in the order P1, P2, P3, P4, and P5 all at time 0.

FCFS

SJF



Non-preemptive priority (a smaller priority number implies a higher priority)



RR (quantum = 3)

5. Consider the following four processes with arrival times (in milliseconds) and their length of CPU bursts (in milliseconds) as shown below:

Process	P1	P2	P3	P4
Arrival time	0	1	3	4
CPU burst time	3	1	3	Z

These processes are run on a single processor using preemptive Shortest Remaining Time First scheduling algorithm. If the average waiting time of the processes is 1 millisecond, then the value of Z is _____.

A) 2 B) 7 C) 1 D) 4

6. Consider three CPU-intensive processes, which require 10, 20 and 30 time units and arrive at times 0, 2 and 6, respectively. How many context switches are needed if the operating system implements a shortest remaining time first scheduling algorithm? Do not count the context switches at time zero and at the end.

(A) 1 (B) 2 (C) 3 (D) 4

7. Five jobs A, B, C, D and E are waiting in Ready Queue. Their expected runtimes are 9, 6, 3,5 and x respectively. All jobs entered in Ready queue at time zero. They must run in _____order to minimize average response time if 3 < x < 5.

A) B, A, D, E, C B) C, E, D, B, A C) E, D, C, B, A D) C, B, A, E, D

Page replacement algorithms

8. Occurs when a program accesses a page not currently in memory A computer has 16 pages of virtual address space but the size of main memory is only four frames. Initially the memory is empty. A program references the virtual pages in the order 0, 2, 4, 5, 2, 4, 3, 11, 2, 10. How many page faults occur if LRU page replacement algorithm is used?

A) 3 B) 5 C) 7 D) 8

9. A LRU page replacement is used with four page frames and eight pages. How many page faults will occur with the reference string 0172327103 if the four frames are initially empty?

A) 6 B) 7 C) 8 D) 5

10. Given the reference to the following pages by a program0, 9, 0, 1, 8, 1, 8, 7, 8, 7, 1, 2, 8, 2, 7, 8, 2, 3, 8, 3How many page faults will occur if the program has three-page frames available to it and uses an optimal replacement?

A) 7 B) 8 C) 9 D) None

11. The total number of page faults for the reference string 1,2,3,4,5,6,7,8,9,10 using FIFO page replacement policy for a process m if 3 frames are allocated to its are:

A) 9 B) 10 C) 8 D) 11

12. Given the following stream of page references by an application, calculate the number of page faults the application would incur with the following page replacement algorithms. Assume that all pages are initially free. **Reference Stream: A B C D A B E A B C D E B A B**

a. FIFO page replacement with 3 physical pages available

Refrenence stream:	*A*	*B*	*C*	*D*	*A*	*B*	*E*	*A*	*B*	*C*	*D*	*E*	*B*	*A*	*B*
oldest page	*A*	*A*	*A*	*B*	*C*	*D*	*A*	*A*	*A*	*B*	*E*	*E*	*C*	*D*	*D*
		B	*B*	*C*	*D*	*A*	*B*	*B*	*B*	*E*	*C*	*C*	*D*	*B*	*B*
Newest page			*C*	*D*	*A*	*B*	*E*	*E*	*E*	*C*	*D*	*D*	*B*	*A*	*A*
page fault	√	√	√	√	√	√	√			√	√		√	√	

11 page faults

b. LRU page replacement with 3 physical pages available.

Refrenence stream:	*A*	*B*	*C*	*D*	*A*	*B*	*E*	*A*	*B*	*C*	*D*	*E*	*B*	*A*	*B*
least recently used	*A*	*A*	*A*	*B*	*C*	*D*	*A*	*B*	*E*	*A*	*B*	*C*	*D*	*E*	*E*
		B	*B*	*C*	*D*	*A*	*B*	*E*	*A*	*B*	*C*	*D*	*E*	*B*	*A*
most recently page			*C*	*D*	*A*	*B*	*E*	*A*	*B*	*C*	*D*	*E*	*B*	*A*	*B*
page fault	√	√	√	√	√	√	√			√	√	√	√	√	

12 page faults

c. OPT page replacement with 3 physical pages available.

On a page fault, replace the page used furthest in the future.

Refrenence stream:	*A*	*B*	*C*	*D*	*A*	*B*	*E*	*A*	*B*	*C*	*D*	*E*	*B*	*A*	*B*
	A	*B*	*C*	*D*	*D*	*D*	*E*	*E*	*E*	*E*	*E*	*E*	*E*	*E*	*E*
		A	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*	*B*
			A	*A*	*A*	*A*	*A*	*A*	*A*	*C*	*D*	*D*	*D*	*A*	*A*
page fault	√	√	√	√			√			√	√			√	

8 page faults

13. A system that uses FIFO page replacement policy has 4 page frames with no pages loaded initially. 100 distinct pages are accessed by the system in some order and then the same 100 pages are accessed in the reverse order. How many page faults will occur?

a. 193 b. 194 c. 195 d. 196

Contiguous memory allocation algorithms

14. Given the following configuration with jobs arriving in order (Job A, B, C, D) and with blocks shown in order from low order memory to high order memory:

a. Apply best-fit and first-fit algorithms to indicate which memory blocks are allocated to each of the

Job List:	
Job Number	**Memory Requested**
Job A	256K
Job B	900K
Job C	50K
Job D	350K

Memory Block List:	
Memory Block	**Memory Block Size**
Block 1	910K
Block 2	900K
Block 3	200K
Block 4	300K

b. Calculate the total amount of internal fragmentation in all four blocks using the best-fit algorithm.

15. Consider a swapping system in which memory consists of the following hole sizes in memory order: 10K, 4K, 20K, 18K, 7K, 9K, 12K, and 15K. Which hole is taken for successive segment requests of: I) 12K, II) 10K, III) 9K
for (a) First-fit? (b) Best-fit? (c) Worst-fit?

16. Given memory partitions of 100 K, 500 K, 200 K, 300 K and 600 K (in order) and processes of 212 K, 417 K,112 K, and 426 K (in order), using the first-fit algorithm, in which partition would the process requiring 426 K be placed ?

A) 500 K B) 200 K C) 300 K D) 600 K

Paging

17. Consider a logical address space of eight pages of 1024 words each, mapped onto a physical memory of 32 frames.

a. How many bits are there in the logical address?
b. How many bits are there in the physical address?

18. Refer to the following PMT:

Page	0	1	2	3
Frame	5	2	7	3

1. If the frame size of 1024, what is the physical address associated with the logical address <2, 85>?
7253
2. If the frame size of 1024, what is the physical address associated with the logical address <3,555>?
3627
3. If the frame size of 1024, what is the physical address associated with the logical address <3,1555>?
Illegal address. The offset is larger than the page size.

19. If a processor has 32 bit virtual address, 28 bit physical address, 2 KB pages. How many bits are required for the virtual, physical page number?

A) 17,21 B) 21,17 C) 6,10 D) None

20. Consider a logical address space of 8 pages of 1024 words each, mapped onto a physical memory of 32 frames. How many bits are there in the physical address and logical address respectively?

A) 5, 3 B) 10, 10 C) 15, 13 D) 15, 15

21. If there are 64 pages, and the page size is 4096 words, the length of the logical address is _____.

A) 16 bits B) 18 bits C) 20 bits D) 22 bits

22. Consider the following page table, in which "x" means an invalid entry.

Logical	Physical
15	x
14	x
13	x
12	x
11	7
10	x
9	5
8	x
7	x
6	x
5	3
4	4
3	0
2	6
1	1
0	2

Assume a 4 KB page size. Give the physical address corresponding to the following logical addresses. All addresses are decimal values.

a) 20

b) 4100

Give the logical address corresponding to the following physical addresses.

a) 24300

23. For the following page table:

Page Number	*Frame Number*
0	5
1	2
2	7
3	0

Assume that logical memory size is 1024 bytes and the number of frames in the physical memory are 16 frames. **Find:**

- **a) Page size.**
- **b) Physical memory size.**
- **c) The physical address corresponding to the logical address 717.**
- **d) The logical address corresponding to the physical address 764.**

24. Consider a logical address space of 32 pages of 2048 words mapped into memory of 64 frames. Then the number of bits required for logical address are

(A) 16-bits (B) 17-bits (C) 18-bits (D) 20-bits

25. If 8 bits are used in a virtual address to designate an offset within a page, each page must be exactly 256 bytes. T/F
26. If there are 64 frames, and the frame size is 1024 words, the length of physical address is:
(A) 16-bits (B) 17-bits (C) 18-bits (D) 20-bits

EAT using TLB

27. The hit ratio of a Translation Lookaside Buffer (TLB) is 80%. It takes 20 nanoseconds (ns) to search TLB and 100 ns to access main memory. The effective memory access time is _____.

A	36 ns	B	140 ns
C	122 ns	D	40 ns

28. Suppose it takes 100 ns to access page table and 20 ns to access associative memory. If the average access time is 28 ns, the corresponding hit rate is :

A	100 percent	B	90 percent
C	80 percent	D	70 percent

29. Suppose it takes 100 ns to access a page table and 20 ns to access associative memory with a 90% hit rate, the average access time equals :

A	20 ns	B	28 ns
C	90 ns	D	100 ns

30. Calculate the cache Hit Ratio using the formula presented in this chapter assuming that the total number of requests is 2,056 and 647 of those requests are found in the cache.
31. If the hit ratio to a TLB is 80%, and it takes 15 nanoseconds to search the TLB, and 150 nanoseconds to access the main memory, then what must be the effective memory access time in nanoseconds?
A. 185 B. 195 C. 205 D. 175

Consider a paging hardware with a TLB. Assume that the entire page table and all the pages are in the physical memory. It takes 10 milliseconds to search the TLB and 80 milliseconds to access the physical memory. If the TLB hit ratio is 0.6, the effective memory access time (in milliseconds) is _____.

A 120
B **122**
C 124
D 118

EAT in demand paging

32. Suppose the time to service a page fault is on the average 10 milliseconds, while a memory access takes 1 microsecond. Then a 99.99% hit ratio results in average memory access time of

A. 1.9999 milliseconds
B. 1 millisecond
C. 9.999 microseconds
D. 1.9999 microseconds

33. Consider a system with page fault service time(S)=100 ns, main memory access time(M)=20 ns, and page fault rate(P)=65%. Calculate the effective memory access time.
A) 62 ns B) 82 ns C) 80 ns D) 72 ns

34. The time taken to service a page fault is on average 10ms and the memory access time is 20 ms. If the hit ratio is 70%, calculate the average access time.
(A) 3018 ms (B) 4014 ms (C) 3014 ms (D) 4024 ms

35. In a paged memory, the page hit ratio is 0.35, the time required to access a page in secondary memory is equal to 100 ns. The time required to access a page in primary memory is 10ns. The average time required to access a page is _____.
A. 3.0ns. B. 68.0 ns. C. 68.5 ns. D. 78.5 ns.

Segmentation

36. Consider the following segment table:

Segment	Limit	Base
0	1000	1400
1	400	6300
2	400	4300
3	1100	3200
4	1000	4700

37. The physical address for a logical address which is in segment 2 with offset 253 is
(A) 4553 (B) 6353 (C) 6253 (D) 4453

38. Consider the following segment table:

Segment No.	Base	Length
0	1219	700
1	2300	14
2	90	100
3	1327	580
4	1952	96

Which of the following logical address will produce trap addressing error?

A. 0, 430
B. 1, 11
C. 2, 100
D. 3, 425
E. 4, 95

Calculate the physical address if no trap is produced.

Fixed Relocation

39. If, in a fixed partition memory management system, the current value of the base register is 42993 and the current value of the bounds register is 2031, compute the physical addresses that correspond to the following logical addresses:
    a. 104
    b. 1755
    c. 3041
40. If, in a single contiguous memory management system, the program is loaded at address 30215, compute the physical addresses (in decimal) that correspond to the following logical addresses:
    a. 9223
    39438
    b. 2302
    32517
    c. 7044
    37259

Internal fragmentation

41. If the process size is 3.5 KB and frame size= 2 KB, what is the amount of internal fragmentation?

a) 1 b) 0.5 c) 2 d) none

42. If the process size is 2.01 KB and frame size = 2 KB, what is the amount of internal fragmentation?

a) 1.75 b) 1.45 c) 1.99 d) none