Ollscoil Chathair
Bhaile Átha Cliath
Dublin City University

AUGUST/RESIT EXAMINATIONS 2022/2023

MODULE: EE496 - Computer Architecture and HDL

PROGRAMME(S):

ECE	BEng Electronic & Computer Engineering
ECSAO	Study Abroad (Engineering & Computing)
ECEI	BEng Electronic & Computer Engineering

YEAR OF STUDY: 4,O

EXAMINER(S):

Dr. Xiaojun Wang	(Internal)	(Ext:5808)
Prof. Martin Glavin	(External)	External

TIME ALLOWED: 2 Hours

INSTRUCTIONS: **Answer 4 questions. All questions carry equal marks.**

PLEASE DO NOT TURN OVER THIS PAGE UNTIL YOU ARE INSTRUCTED TO DO SO.
The use of programmable or text storing calculators is expressly forbidden.
Please note that where a candidate answers more than the required number of questions, the examiner will mark all questions attempted and then select the highest scoring ones.

There are no additional requirements for this paper.

QUESTION 1 ***[TOTAL MARKS: 25]***

Q 1(a) **[10 Marks]**

Write a VHDL model that infers a simple single port 16x32 RAM block with 16 32-bit words. The RAM *write is synchronous* to a clock rising edge, and when RAM write is enabled (we). The RAM *read is asynchronous*. The figure below shows the RAM input and output ports.

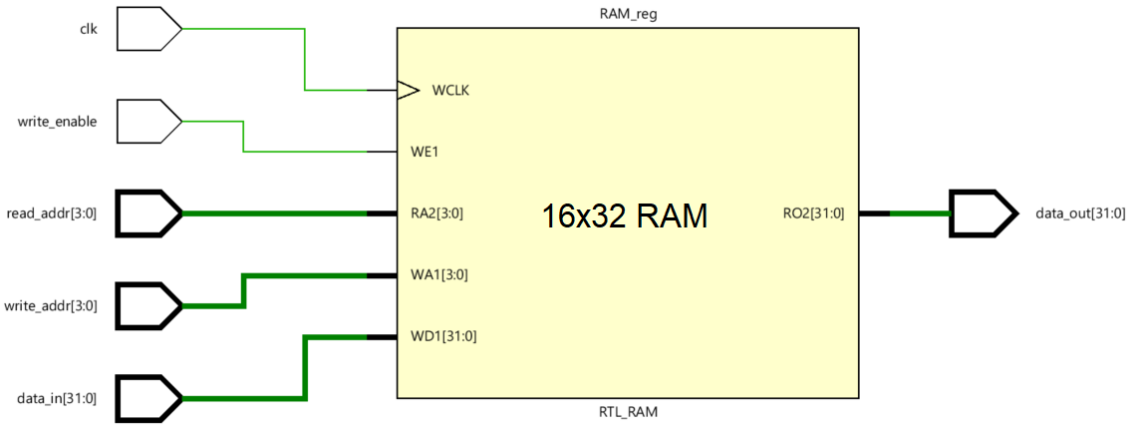


Figure Q 2(a)

Q 1(b) **[5 Marks]**

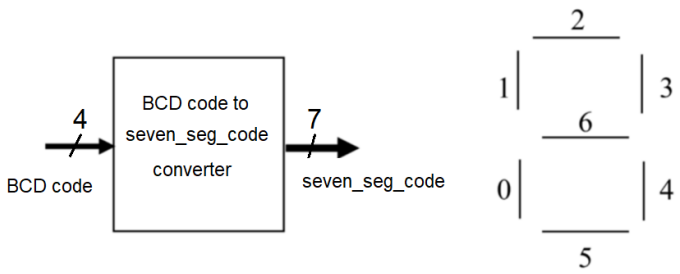
Briefly discuss the differences between Distributed and Block RAM in the context of a Xilinx FPGA?

Q 1(c) **[5 Marks]**

Write a VHDL fragment extending a 32-bit *signed* type signal `a(31 downto 0)` to 64 bits and assigns it to a 64-bit *signed* type signal `y(63 downto 0)`, maintaining the original decimal value of `a`.

Q1(d) **[5 Marks]**

A BCD (binary coded decimal) code to a 7-segment display code converter converts a BCD digit to an appropriate code to drive a 7-segment display shown below. A segment *illuminates when its corresponding bit is at logic level* `'0'`; otherwise, it is off. Write an RTL VHDL model for the decoder shown below.



[End of Question 1]

QUESTION 2 ***[TOTAL MARKS: 25]***

Q 2(a) **[5 Marks]**

What problem can *shared variables* introduce into a VHDL model? Explain the problem with an example.

Q 2(b) **[5 Marks]**

Briefly describe the *memory hierarchy* of a modern computer system.

Q 2(c) **[7 Marks]**

What is a *subtype* in VHDL? Briefly explain the usefulness of subtypes.

Q 2(d) **[8 Marks]**

Suppose `s1` is a 4-bit `std_logic_vector` subtype signal with a value of "1101". When comparing `s1` with "11-1" using the standard comparison operator =, will the result be *true* or *false*? How to appropriately compare `std_logic_vector` values containing don't care elements?

[End of Question 2]

QUESTION 3 ***[TOTAL MARKS: 25]***

Q 3(a) **[5 Marks]**

Briefly explain the difference between a Mealy FSM and a Moore FSM. Which type of FSM would you choose if you want synchronous outputs?

Q 3(b) **[7 Marks]**

Describe the *one-hot encoding* scheme and briefly explain the advantages of its use in an FSM design for an FPGA implementation.

Q 3(c) **[5 Marks]**

When a VHDL simulator starts, what is the initial default value of a signal not explicitly initialised at declaration? For example, what is the initial default value for a signal of subtype `std_logic`?

Q 3(d) **[8 Marks]**

Write a *synthesisable* VHDL model for a pulse divider that divides the input pulse frequency by 6. That is to say, for three periods of the input pulse, the divided pulse output is at logic '0', then for the following three periods of the input pulse, the divided pulse output is at logic '1', and then the process repeats. So, for example, if the input pulse period is 20 ns, then the output pulse period will be 120 ns.

[End of Question 3]

QUESTION 4 ***[TOTAL MARKS: 25]***

Q 4(a) **[15 Marks]**

(i) Draw the logic circuit synthesised from the following VHDL code.
[3 marks]

(ii) Explain why the circuit synthesised from the VHDL code is *not recommended* for FPGA designs.
[4 marks]

(iii) Rewrite the architecture body, so the synthesised circuit is *suitable* for FPGA designs.
[4 marks]

(iv) Draw the logic circuit synthesised from your architecture written in (iii) above.
[4 marks]

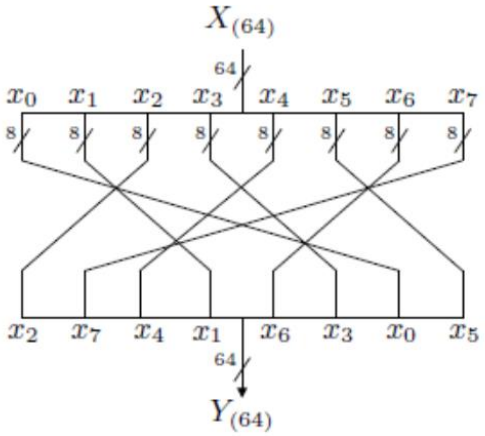
```
library ieee; use ieee.std_logic_1164.all;
entity exam is
 port (d, ctrl1, ctrl2, clk: in std_ulogic;
       q: out std_ulogic);
end entity exam;
architecture arch1 of exam is
   signal clk_sig: std_ulogic;
begin
  clk_sig <= clk and ctrl1 and ctrl2;
  q <= d when rising_edge(clk_sig);
end architecture arch1;
```

Q 4(b) **[5 Marks]**

Explain the difference between attribute `'event` and attribute `'stable`. If `clk` is a `std_logic` subtype signal, write two expressions to determine the rising edge of clk, each using one of the attributes.

Q 4(c) **[5 Marks]**

The following diagram shows the Round Permutation function of the ultra-lightweight block cypher Piccolo. The input is 64 bits (8 bytes), and the output is also 64 bits which are the permutated 8 bytes of the 64-bit input. Write a VHDL code fragment that implements the permutation function.



[End of Question 4]

Q 5(a) **[5 Marks]**

Assuming a multi-cycle computer datapath has five pipeline stages:

1. Hardware to support an instruction *fetch*
2. Hardware to support an instruction *decode*
3. Hardware to support instruction *execution* (i.e. the ALU)
4. Hardware to support a *memory* read or write
5. Hardware to support the *write-back* of the ALU result to the register-file

Assume that each of the above stages takes the amount of time specified in the table below.

Fetch Instruction from Memory	**Decode** & read operands from reg files	Instruction **Execution** ALU	**Memory** Read/Write	Results **write-back** to Reg files
180 ps	100 ps	150 ps	180 ps	80 ps

Given the times for the *datapath* stages listed above, what would the *clock period* be for the entire *datapath*?

Q 5(b) **[5 Marks]**

For the pipelined *datapath* in Q5(a), assuming no hazards or stalls, how long does it take to execute *one* instruction, or what is the instruction *latency?*

Q 5(c) **[5 Marks]**

What is the *throughput* of the pipelined datapath in Q5(a)?

5(d) **[10 Marks]**

For *a single-cycle processor* with the same data path time specification as in the table of Q5(a), What would be the clock period, the instruction latency and the throughput of the single-cycle processor?

[End of Question 5]

[END OF EXAM]