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SEMESTER 1 EXAMINATIONS 2020/2021

MODULE: EE496 - Computer Architecture and HDL

PROGRAMME(S):
ECE BEng Electronic & Computer Engineering

YEAR OF STUDY: 4

EXAMINER(S):

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Dr. Josep R. Casas	(External)	External

TIME ALLOWED: 2 hours (and 30 minutes additional time)

INSTRUCTIONS: **Answer 4 questions. All questions carry equal marks.**

PLEASE DO NOT TURN OVER THIS PAGE UNTIL YOU ARE INSTRUCTED TO DO SO.
The use of programmable or text storing calculators is expressly forbidden.
Please note that where a candidate answers more than the required number of questions, the examiner will mark all questions attempted and then select the highest scoring ones.

There are no additional requirements for this paper.

QUESTION 1 ***[TOTAL MARKS: 25]***

Q 1(a) **[5 Marks]**

Draw the State Diagram for a "sequence detector" that can detect the occurrence of a particular digital signature on an incoming bit-stream from input `Y`. When successfully detected, the output `Match` indicator should go high. The signature to be detected is '1001'.

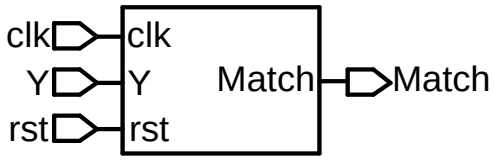

Figure Q1

Q 1(b) **[10 Marks]**

Write a synthesisable VHDL model for the "sequence detector" FSM, assuming it has an active high asynchronous reset signal `rst`, that will reset the sequence detector. The clock signal is `clk`. The external view of the state machine is shown in Figure Q1.

Q 1(c) **[5 Marks]**

Explain the difference between a Mealy FSM and a Moore FSM. Is the above sequence detector a Moore FSM or a Mealy FSM?

Q 1(d) **[5 Marks]**

Describe the one-hot encoding scheme and briefly explain the advantages of its use in an FSM design for an FPGA implementation.

[End of Question 1]

QUESTION 2 ***[TOTAL MARKS: 25]***

Q 2(a) **[5 Marks]**

Write a VHDL description of the one-bit comparator shown in Figure Q 2(A) using VHDL.

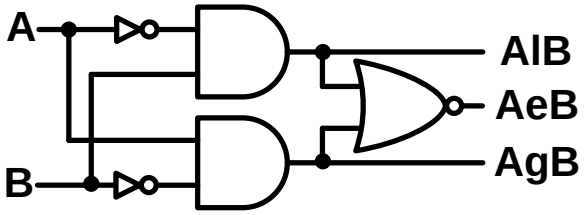

Figure Q 2(A)

Q 2(b) **[10 Marks]**

Implement a 2-bit comparator using VHDL by instantiating three one-bit comparators implemented in part (a) according to the connections shown in Figure Q 2(B).

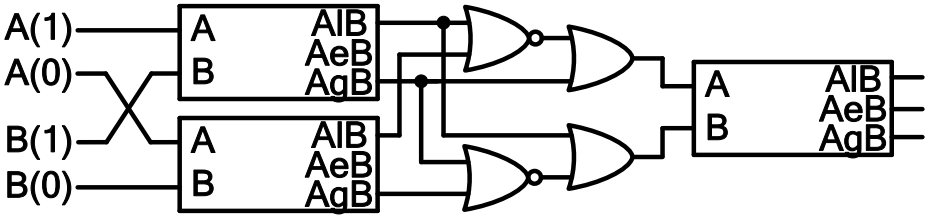

Figure Q 2(B)

Q 2(c) **[10 Marks]**

Write a testbench that will generate all possible test inputs and automatically check that the 2-bit comparator returns the expected results, reporting if each test has passed or failed. *Note: You can code the test inputs directly within the testbench, no need to read the test inputs from a file nor write the test results to a file.*

[End of Question 2]

QUESTION 3 ***[TOTAL MARKS: 25]***

Q 3(a) **[9 Marks]**

Manually synthesize and draw the logic circuit implied by the following VHDL code. Explain why each of the logic components inferred from the code.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Q3A is
    Port(Clk     : in  std_logic;
         Sig     : in  std_logic;
         Deb_Sig : out std_logic);
end Q3A;
architecture rtl of Q3A is
  signal Q0,Q1,Q2 : std_logic := '0';
begin
 process
  begin
    wait on Clk until Clk = '1';
    Q0 <= Sig;
    Q1 <= Q0;
    Q2 <= Q1;
 end process;

 Deb_Sig <= Q0 and Q1 and (not Q2);
end rtl;
```

Q 3(b) **[8 Marks]**

Manually synthesize and draw the logic circuit implied by the following VHDL code. Explain why each of the logic components is inferred from the code.

```
library ieee;
use ieee.std_logic_1164.all;
entity Q3B is
 port(A, B, C, D, E, F : in std_logic;
      out1             : out std_logic);
end Q3B;
architecture rtl of Q3B is
 signal s: std_logic;
begin
 p1: process(A, B, C, D) begin
   s <= A and B;
   s <= s or (C and D);
   s <= s or (E and F);
   out1 <= s;
 end process p1;

end rtl;
```

Q 3(c) **[8 Marks]**

Manually synthesize and draw the logic circuit implied by the following VHDL code. Explain why each of the logic components is inferred from the code.

```
library ieee;
use ieee.std_logic_1164.all;

entity Q3C is
 port(A, B, C, D, E, F: in std_logic;
      out2            : out std_logic);
end Q3C;

architecture rtl of Q3C is
 signal s: std_logic;
begin

 p2: process(A, B, C, D)
       variable v : std_logic;
     begin
       v := A and B;
       v := v or (C and D);
       v := v or (E and F);
     out2 <= v;
     end process p2;

end rtl;
```

[End of Question 3]

QUESTION 4 ***[TOTAL MARKS: 25]***

Q 4(a) **[5 Marks]**

Suppose `clk` and `enable` are bit type signals. Explain the differences between the following two `wait` statements.

```
wait on clk until (clk='1' and enable='1');

wait until (clk='1' and enable='1');
```

Q 4(b) **[8 Marks]**

The truth table of a priority circuit is shown below. Write a synthesisable VHDL model for the priority circuit. A0 to A3 are the inputs, Y0 to Y3 are the outputs.

A_3	A_2	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	**1**
0	0	1	X	0	0	**1**	0
0	1	X	X	0	**1**	0	0
1	X	X	X	**1**	0	0	0

Q 4(c) **[4 Marks]**

Draw a logic circuit implied by your VHDL code written in part Q4(b).

Q 4(d) **[4 Marks]**

An 8-bit **signed** number `N` has a value with hexadecimal representation `X"83"`. What is the equivalent decimal value of `N`? Write out the hexadecimal representation of `N` when it is extended to 16-bit while maintaining the same equivalent decimal value.

Q 4(e) **[4 Marks]**

A 16-bit **signed** number `M` has a vaue with hexadecimal representation `X"FE0C"`.

i) If `K` is an 8-bit **signed** variable after the following statement is executed

```
K := resize(N, K'length);
```

What is the hexadecimal representation of `K`?

ii) What is the equivalent decimal value of K? Has K maintained the same value as that of M?

[End of Question 4]

QUESTION 5 ***[TOTAL MARKS: 25]***

Q 5(a) **[5 Marks]**

When a VHDL simulator starts, what determines the initial value of all signals of an enumeration type? What is the default initial value for a signal of subtype `std_logic`?

Q 5(b) **[5 Marks]**

In the Vivado design suite picoseconds (ps) are used as the minimum simulation resolution because testing equipment can measure timing only to the nearest picosecond resolution. Can you speed up simulation through the use of coarser simulation resolution? In other words, would simulation run faster at resolution 1 ns than at 1 ps? Explain why?

Q 5(c) **[5 Marks]**

Assuming a multi-cycle and pipelined computer datapath is broken down into 5 stages

1. Hardware to support an instruction *fetch*
2. Hardware to support an instruction *decode*
3. Hardware to support instruction *execution* (i.e. the ALU)
4. Hardware to support a *memory* read or write
5. Hardware to support the *write back* of the ALU result to the register file

Assume that each of the above stages takes the amount of time specified in the table below.

Fetch	Decode	Execute	Memory	Write Back
200 ps	120 ps	150 ps	200 ps	50 ps

Given the times for the datapath stages listed above, what would the *clock period* be for the entire datapath?

Q 5(d) **[5 Marks]**

For the pipelined datapath **in** Q5(c), assuming no hazards or stalls, how long does it take to execute *one* instruction, or what is the instruction latency?

Q 5(e) **[5 Marks]**

What is the throughput of the pipelined datapath in Q5(c)?

[End of Question 5]

[END OF EXAM]