An-Najah National University
Faculty of Engineering and IT

جامعة النجاح الوطنية
كلية الهندسة وتكنولوجيا المعلومات

Computer Engineering Department
Course Name: Digital Circuits Design 1 Lab Number: 10636291
Lab Report Grading Sheet

Instructor: Dr. Amjad Abu Hassan	Experiment #: 2
Academic Year: 2021/2022	Experiment Name: TTL & CMOS Logic Levels
Semester:2	

Students	
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Performed on:	Submitted on:

Report's Outcomes

ILO __ =( ) %	ILO __ =( ) %	ILO __ =( ) %	ILO __ =( ) %	ILO __ =( ) %

Evaluation Criterion	Grade	Points
Abstract answers of the questions: "What did you do? How did you do it? What did you find?"	0.5	
Introduction and Theory Sufficient, clear and complete statement of objectives. In addition to Presents sufficiently the theoretical basis.	1.5	
Apparatus/ Procedure Apparatus sufficiently described to enable another experimenter to identify the equipment needed to conduct the experiment. Procedure sufficiently described.	2	
Experimental Results and Discussion Crisp explanation of experimental results. Comparison of theoretical predictions to experimental results, including discussion of accuracy and error analysis in some cases.	4	
Conclusions and Recommendations Conclusions summarize the major findings from the experimental results with adequate specificity. Recommendations appropriate in light of conclusions. Correct grammar.	1	
Appearance Title page is complete, page numbers applied, content is well organized, correct spelling, fonts are consistent, good visual appeal.	1	
Total	10	

Introduction :

In this experiment we will study CMOS and TTL families, and learn the difference between them , understand the differences between logic levels(low level , high level) for CMOS and TTL gates and to obtain the voltage transfer characteristic (VTC) for TTL and CMOS invertors , we will learn how to compute the noise margin for these two types of IC'S.

Objectives:

• To understand the meaning of Logic 0 and Logic 1

• To understand the significance of VOH, VOL, VIH, and VIL.

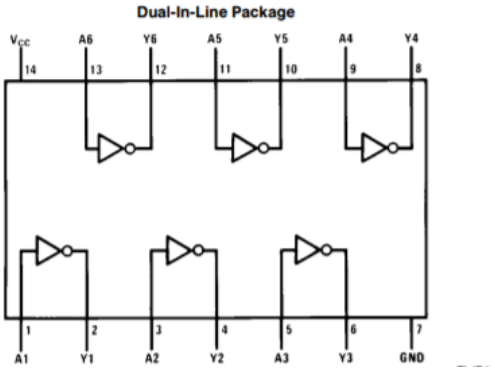
• To determine the noise margins for TTL and CMOS Inverter.

• To understand the differences between logic levels for CMOS and TTL gates.

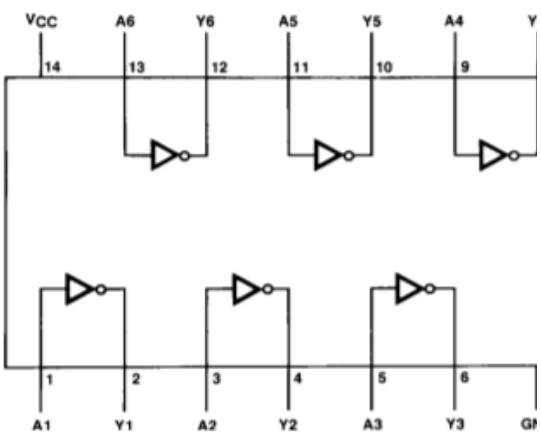
• To obtain the voltage transfer characteristic (VTC) for TTL and CMOS invertors.

Tools:

- 74LS04 TTL IC Inverter



- 74HC04 CMOS IC Inverter



Other tools:

- Wires
- Breadboard
- Power supply
- Multimeter

Procedure:

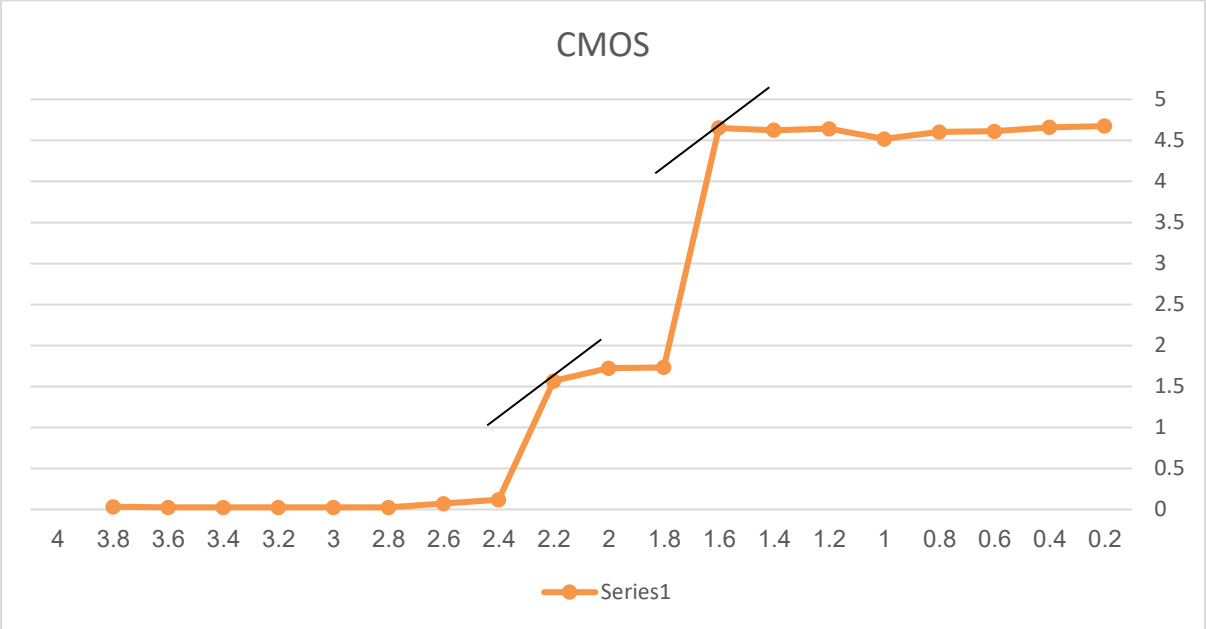
- We connected the IC to the middle of the breadboard and connected it with staple voltage (VCC=5 volt)
- We connected the input of the inverter with variable voltage (from 0-5 increasing it by 0.2 every step) and made common ground with the ground of the IC
- We connected the output of the invertor to the multimeter to measure the voltage of the output and recorded it
- We repeated the steps for each invertor and recorded the results

Practical results:-

For CMOS:

V Inp	V out
.2	4.675
.4	4.66
.6	4.612
.8	4.604
1	4.517
1.2	4.642
1.4	4.625
1.6	4.653
1.8	1.7334
2	1.7229
2.2	1.5664
2.4	0.1191
2.6	0.0725
2.8	0.0256

3	0.0256
3.2	0.0255
3.4	0.0246
3.6	0.0246
3.8	0.0334
4	0.0193



From the graph the slope is nearly -1 at (1.6, 4.653) ,(2.4, 0.1191)

So VOH =4.653 VIH =2.4 (larger input which it's slope =-1)

VOL=0.1191 VIL=1.6 (smaller input which it's slope =-1)

Noise margin low (NML) = VIL– VOLL = 1.6 – 0.1191 = 1.4809

(This means that the difference in signal by this value will accepted as 0)

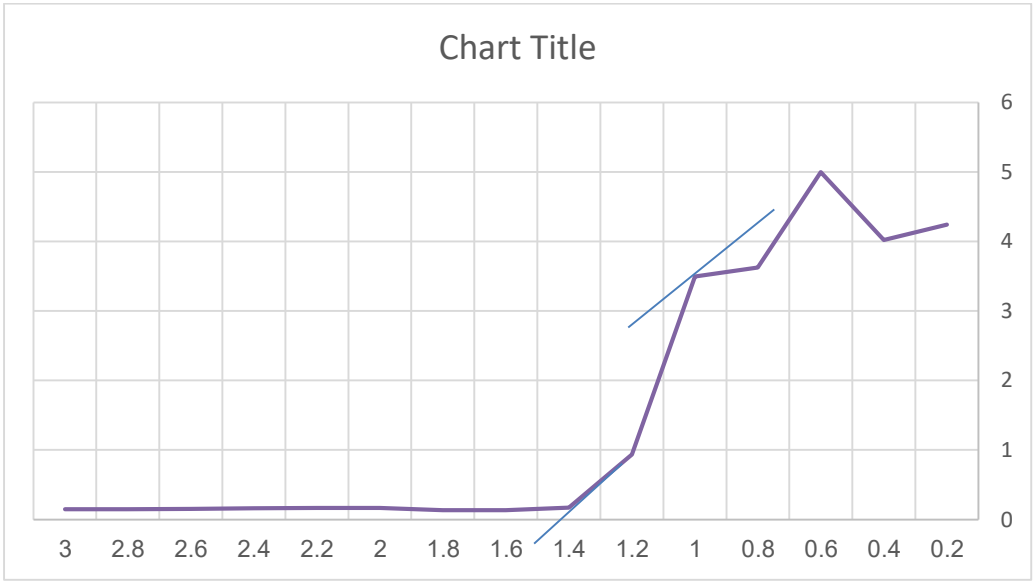
Noise margin high (NMH) = VOH-VIH =4.653 – 2.4 = 2.253

(This means that the difference in signal by this value will accepted as 1)

Forbidden margin between 1.6 and 2.4 (between VIL and VIH)

For TTL:

VINP	VOUT
.2	4.244
.4	4.023
.6	4.995
.8	3.625
1	3.496
1.2	0.9334
1.4	0.1711
1.6	0.1347
1.8	0.1342
2	0.1672
2.2	0.1651
2.4	0.1599
2.6	0.1508
2.8	0.1470
3	0.1465



From the graph the slope is nearly -1 at (1, 3.496) ,(1.4, 0.1711)

So VOH =3.496 VIH =1.4 (larger input which it's slope =-1)

VOL=0.1711 VIL=1 (smaller input which it's slope =-1)

Noise margin low (NML) = VIL– VOLL = 1 - 0.1711 = 0. 8289

(This means that the difference in signal by this value will accepted as 0)

Noise margin high (NMH) = VOH-VIH =3.496 - 1.4 = 2.096

(This means that the difference in signal by this value will accepted as 1)

Forbidden margin between 1 and 1.4 (between VIL and VIH)

Discussion & Question :

Based on this experiment what do we mean by Logic 0 and Logic 1for TTL gates & CMOS gates ?

They represent binary digits we use 0 to represents low voltages and 1 to represents high voltages (in range of 5)

VIH < VOH and VIL> VOL, why?

To avoid forbidden regions and this make the NMH NML both positive value that make the forbidden region smaller.

Conclusion :

We know the difference between the logic “1” and logic “0”

We also calculate the Noise Margin which mean the difference between the acceptable output and input ranges and

We know that the forbidden region in TTL is tighter than forbidden region in CMOS

We noticed that CMOS IC values' are more accurate than TTL because of industrial reasons

The results have some error when we compare results to data sheet for each ICs because the ICs is uses for along time in lab , and main reason is human error .