

ASSIGNMENT Title:

Digital Dice

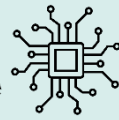


Table of Contents (click to go directly)

- 1- Project Aim**
- 2- Inputs & Outputs**
- 3- Problem solution**
- 4- K-maps & Design**
- 5- Implementation**
- 6- Test**

-Project Aim:

The aim of this project is to design and implement a Digital Dice using basic logic components. The Digital Dice will generate random numbers between 1 and 6, simulating a dice roll for games or educational purposes. This system will utilize basic digital logic design principles to produce a reliable and accurate output on a 7-segment display.

-Problem Statement:

In traditional dice games, the randomness of dice rolls can sometimes be influenced by human factors. This project aims to eliminate such biases by creating a digital system that simulates the roll of a dice. Using D-flip flops to store random values, IC 555 timers to generate timing signals, and BCD to 7-segment decoder to display the results, the system will generate numbers between 1 and 6 and display them on a 7-segment display. The problem being addressed is the need for a simple, low-cost, and accurate digital dice system that can be used in various applications without the need for physical dice

-Inputs:

- **Clock Signal (CLK):**

A periodic signal generated by the IC 555 timer that drives the operation of the D-flip flops and controls the timing for generating random numbers.

- **Manual Dice Roll Button:**

A physical button that the user presses to simulate the rolling action, which could trigger the clock signal or reset the system.

-Outputs:

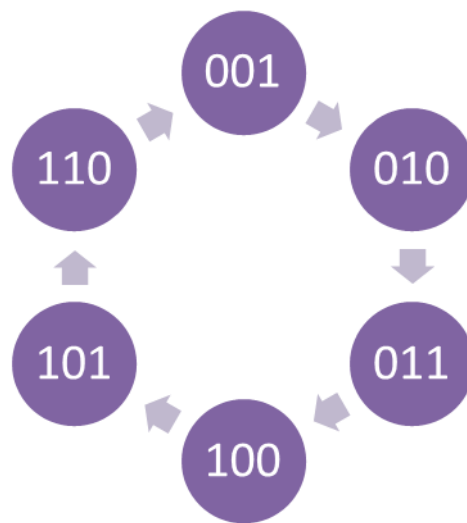
- **BCD to 7-Segment Decoder Output:**

A BCD (Binary Coded Decimal) output connected to the 7-segment display. This converts the 4-bit binary number stored in the D-flip flops into the appropriate 7-segment display code to represent numbers between 1 and 6.

- **7-Segment Display:**

The main output of the system, which will display the generated random number (1 to 6) on a 7-segment display. Each number corresponds to a specific pattern on the display, generated by the BCD to 7-segment decoder.

-Now we need to design a D-flip flop circuit to generate a binary digits from 1 to 6:



-PS NS & excitation table:

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	D_2	D_1	D_0
0	0	0	d	d	d	d	d	d
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	0	0	1	0	0	1
1	1	1	d	d	d	d	d	d

-K-maps:

For D_2 :

	Q_2'	Q_2	
Q_1'	d	1	Q_0'
	0	1	Q_0
Q_1	1	d	
	0	0	Q_0'

$$D_2 = Q_1Q_0 + Q_2Q_1'$$

For D_1 :

	Q_2'	Q_2	
Q_1'	d	0	Q_0'
	1	1	Q_0
Q_1	0	d	
	1	0	Q_0'

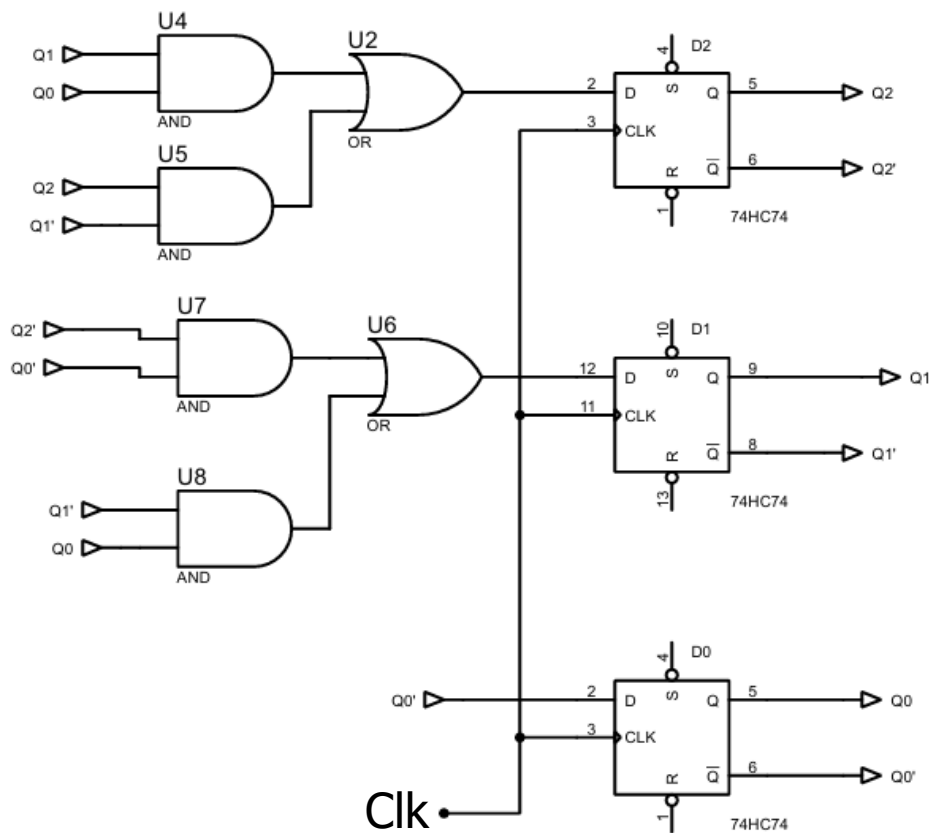
$$D_1 = Q_2'Q_0' + Q_1'Q_0$$

For D_0 :

	Q_2'	Q_2	
Q_1'	d	1	Q_0'
	0	0	Q_0
Q_1	0	d	
	1	1	Q_0'

$$D_0 = Q_0'$$

D-flip flop Design:



-Implementation:

Components: -

- IC 555
- Push button
- 4013 (D-flf)
- 7404 (NOT Gate)
- 7432 (2-input OR Gate)
- 7481 (2-input AND Gate)
- 7447 (BCD to 7-segment)
- FJS5101B (7-segment)
- Resistors
- Capacitors
- Jumper wires

1-IC 555 Circuit (Clock Signal Generator)

- The IC 555 is configured in astable mode to generate a continuous clock signal.
- This clock signal drives the D-flip flops, providing the timing for state transitions, which result in the generation of random numbers.
- The speed of the clock determines how fast the numbers change before the dice "settles" on a final value when the clock stops.

$$T_H = 0.693 \times (R_1 + R_2) \times C_1$$

$$T_H = 0.693 \times (1K\Omega + 10K\Omega) \times 10\mu F$$

$$T_H \approx 0.07623 \text{ seconds}$$

$$T_L = 0.693 \times R_2 \times C_1$$

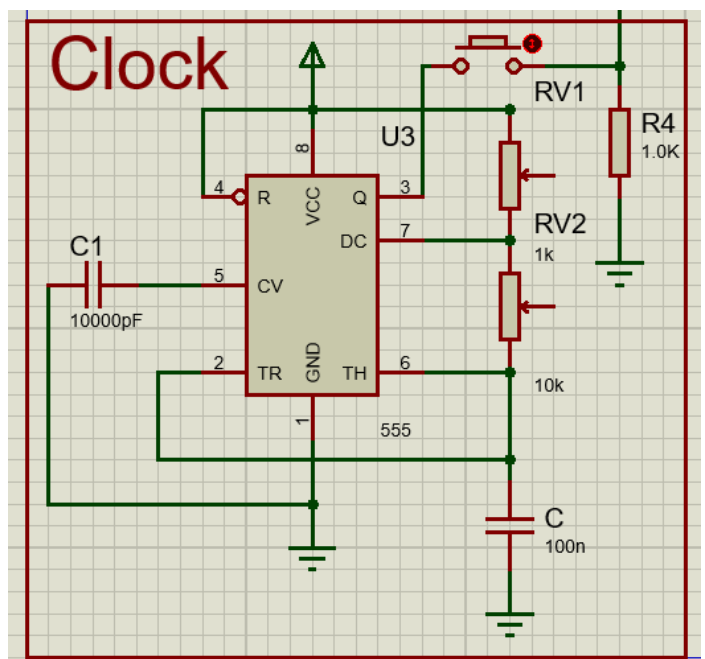
$$T_L = 0.693 \times 10K\Omega \times 100\mu F$$

$$T_L \approx 0.0693 \text{ seconds}$$

$$T_{\text{tot}} = T_H + T_L$$

$$= 0.07623 \text{ seconds} + 0.0693 \text{ seconds}$$

$$\approx 0.14553 \text{ seconds}$$



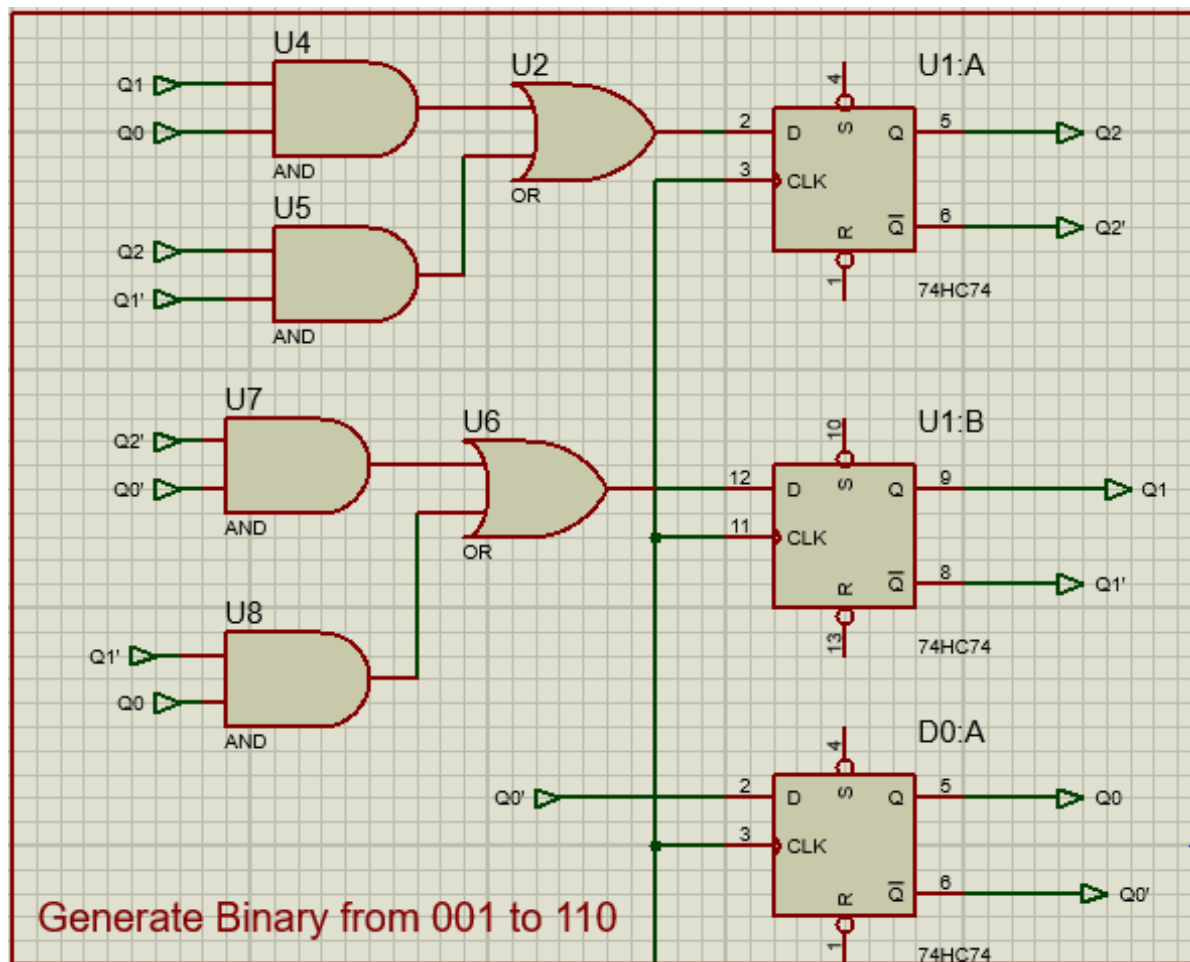
2-D-Flip Flops (Random Number Generator):

- A series of D-flip flops store the binary values that represent the dice numbers.
- The flip-flops are triggered by the clock signal and toggle their states based on the logic design.
- Their outputs collectively form a 3-bit binary number, which corresponds to the dice values (1 to 6).

3-Basic Logic Gates (Logic Control):

Additional logic gates used to:

- Limit the output to the valid dice range (1 to 6).

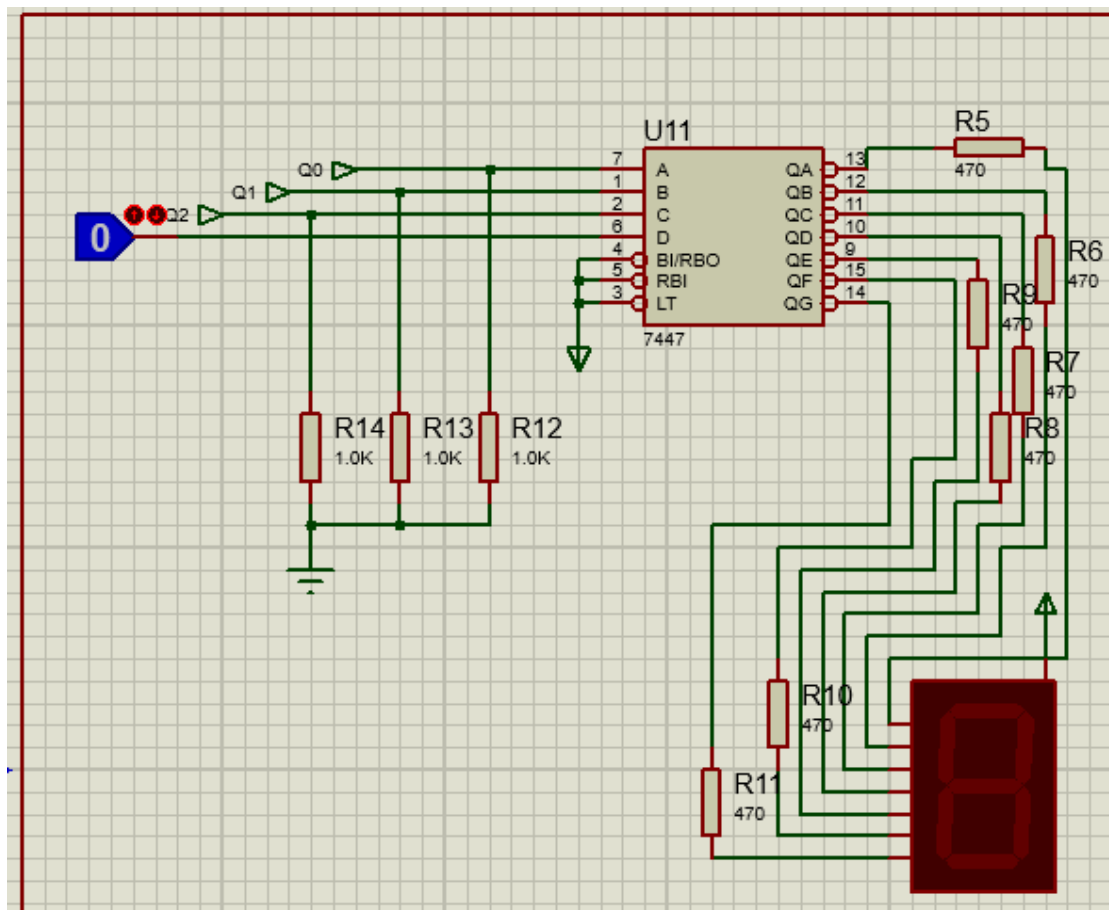


4-BCD to 7-Segment Decoder (IC 7447):

- This IC takes the 3-bit binary output from the flip-flops and converts it into signals that can drive the 7-segment display.
- It maps the binary values to the correct patterns on the 7-segment display to show numbers 1 through 6.

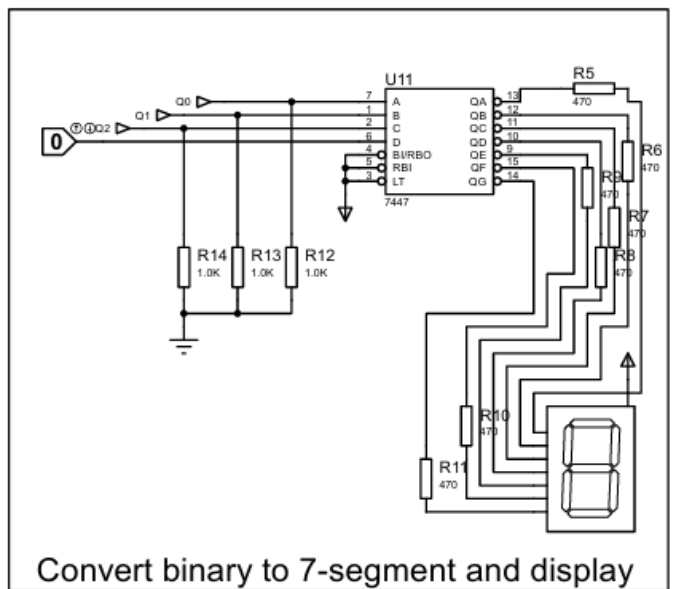
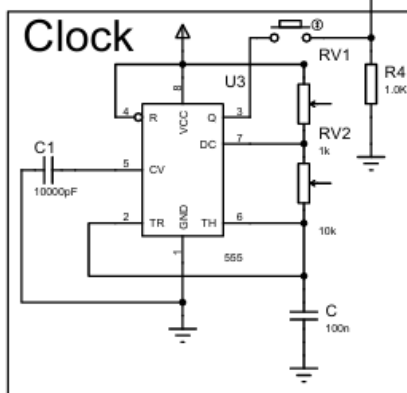
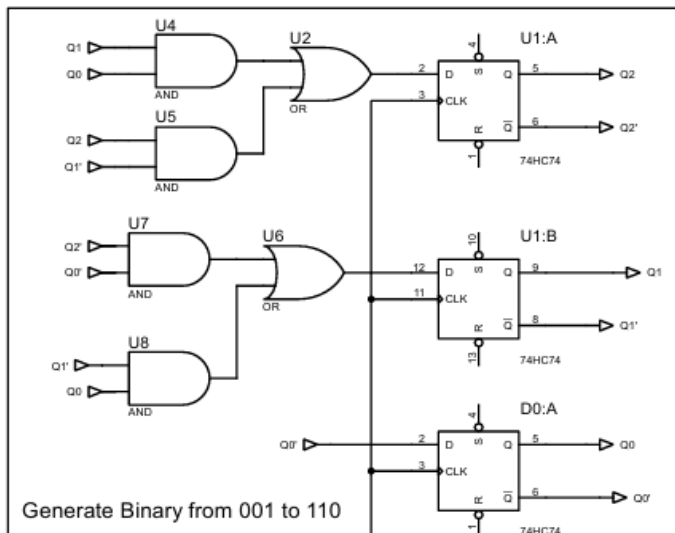
5-7-Segment Display (Output Display):

- It uses the signals from the BCD decoder to visually display the generated dice number.



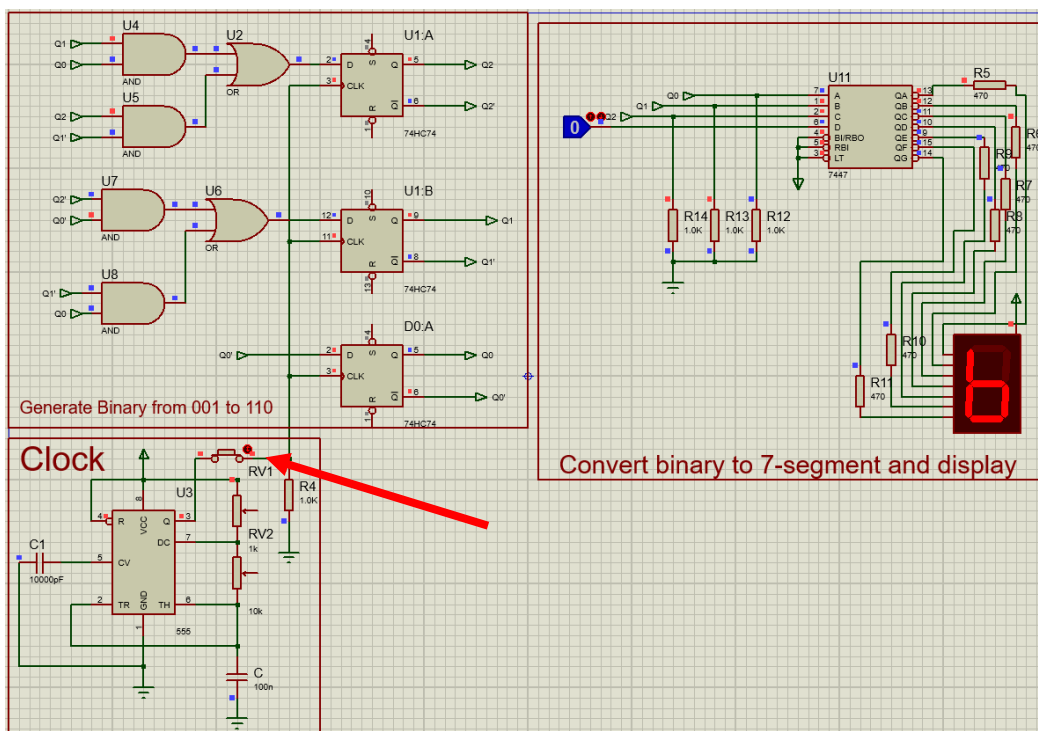
-Summary

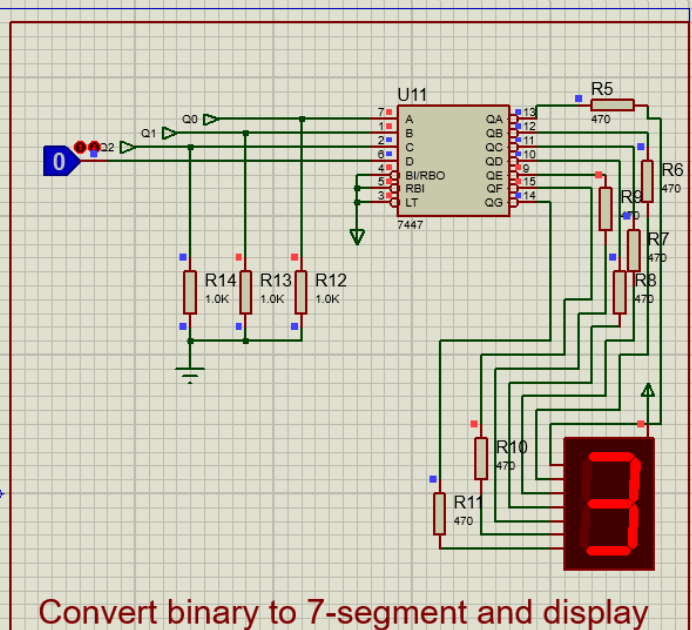
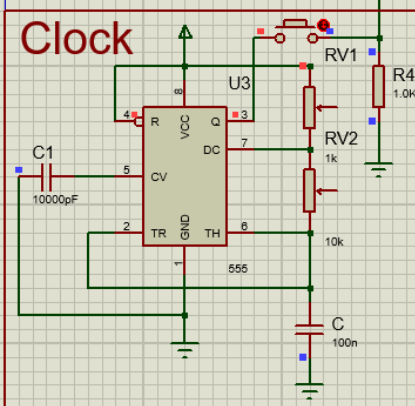
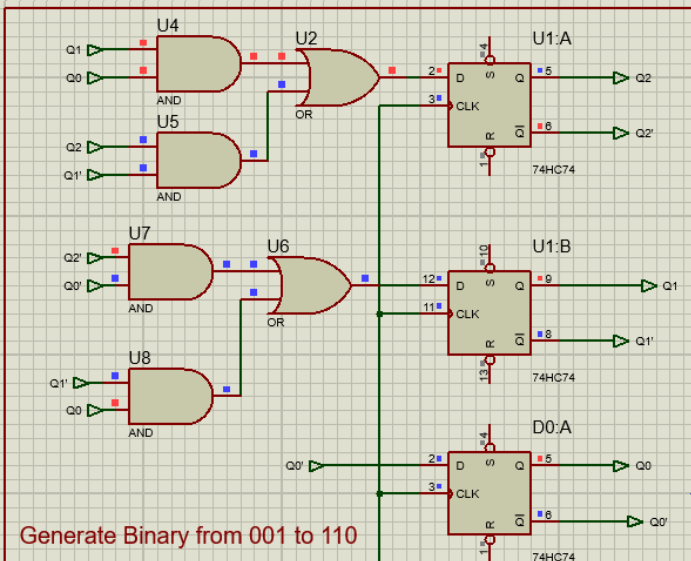
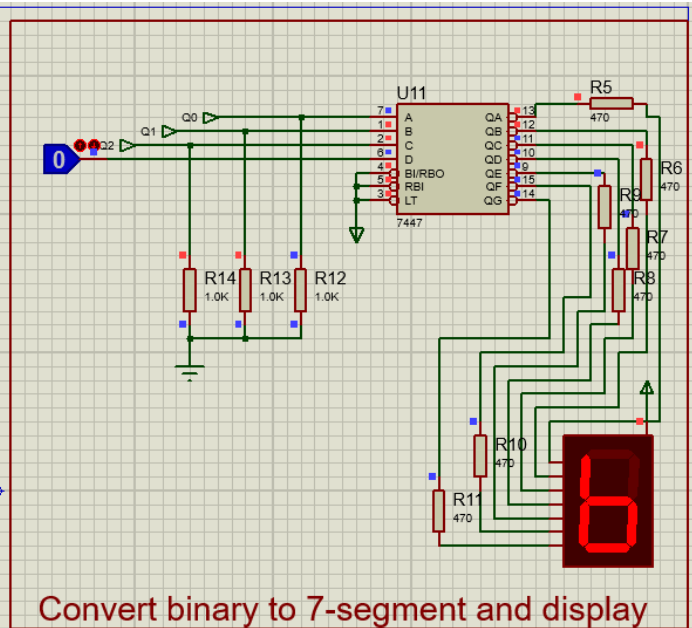
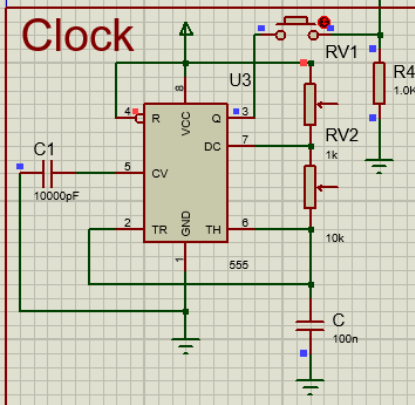
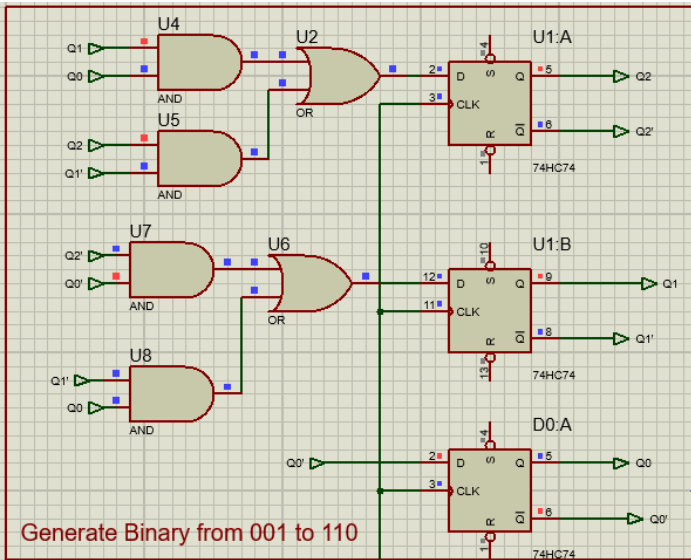
- **IC 555 Timer:** Generates the clock signal for timing.
- **D-Flip Flops:** Store and update binary numbers based on the clock.
- **Logic Gates:** Provide range limiting, control, and auxiliary features.
- **BCD to 7-Segment Decoder:** Converts binary numbers to 7-segment display signals.
- **7-Segment Display:** Shows the dice number (1-6) to the user.

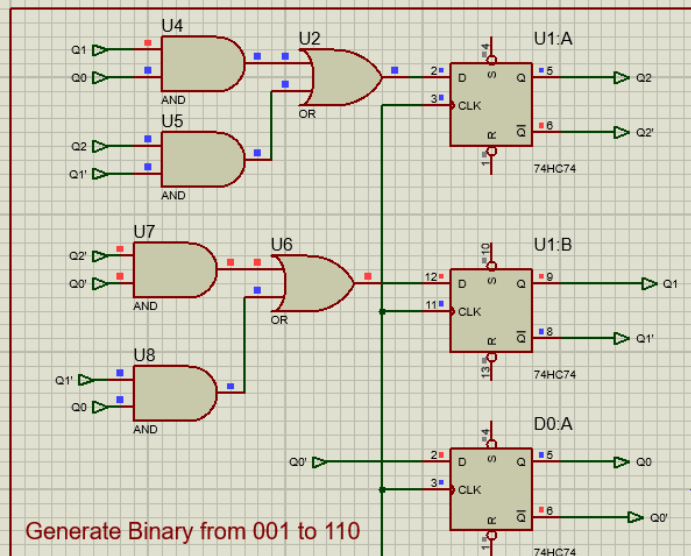


-Test

-first stay pushing the push button the 7-segment will display a numbers from 1 to 6 at a high speed once you release push button a random number from 1 to 6 will be displayed

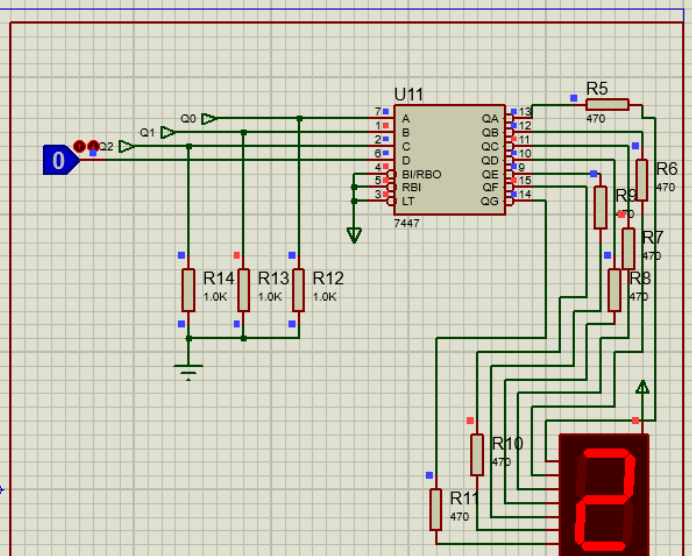
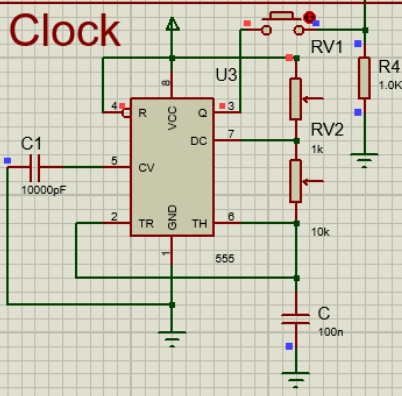




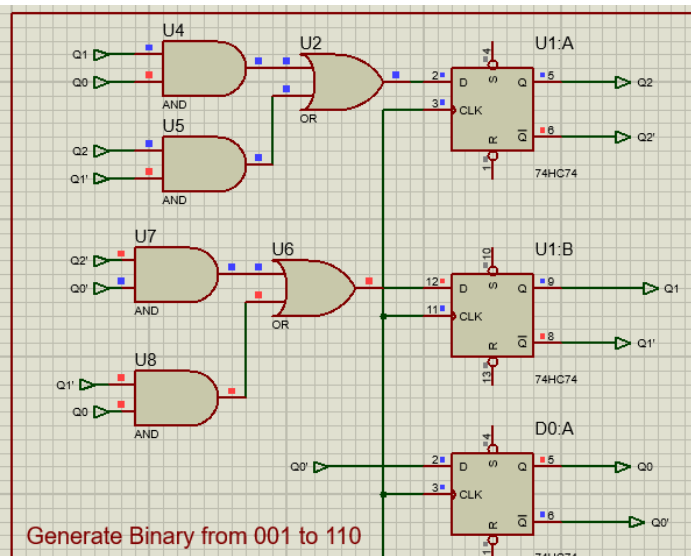


Generate Binary from 001 to 110

Clock

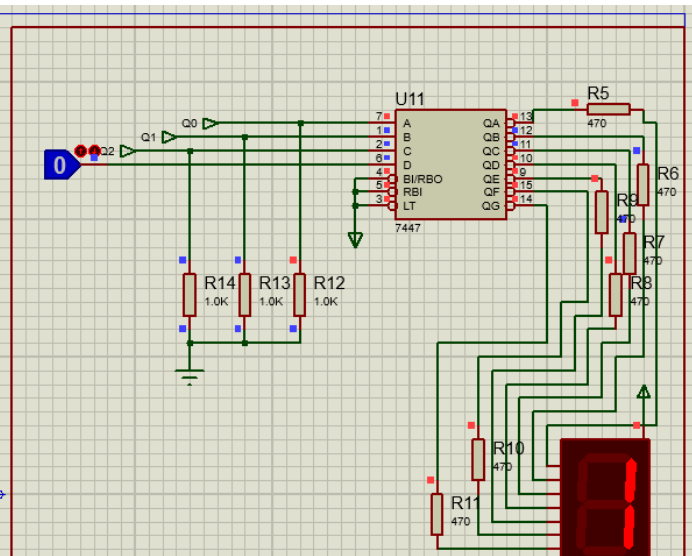
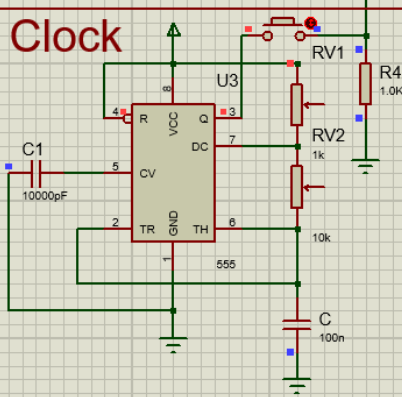


Convert binary to 7-segment and display

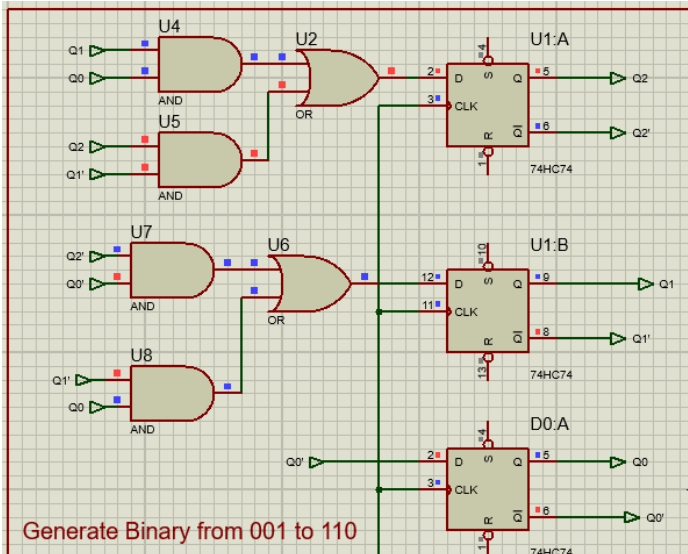


Generate Binary from 001 to 110

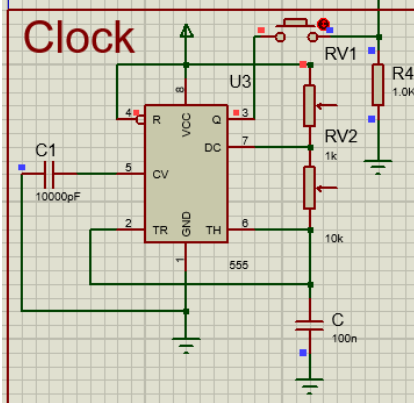
Clock



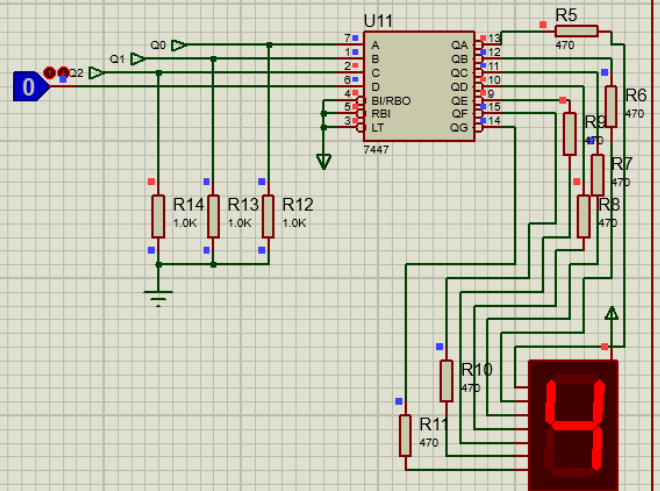
Convert binary to 7-segment and display



Generate Binary from 001 to 110



Clock



Convert binary to 7-segment and display