Ministry of Communications and Information Technology







Embedded Systems Advanced Nanodegree Program

Automotive Door Control System Design (Static Design)

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Tasks	Periodicity	Deadline	Execution time	Occurrence in hyperperiod
BUT1	50ms	50ms	12us	2
BUT2	50 ms	50 ms	13 us	2
Periodic Transmitter	100ms	100ms	140us	1
Uart	20 ms	20ms	150 us	5
Load1	10 ms	10ms	5ms	10
Load2	100ms	100ms	12ms	1

- Hyper period is 100ms
- CPU Load:

Utilization = total execution time/hyper-period

Utilization = 62.9%

System SchedulableRate Monotonic

Utilization"U" = 63.16%

number of tasks"N" = 6

If (U < N(2^(1/N)-1)) then system is schedulable 0.629 < 0.734 thus system is schedulable

Time Demand

$$w_i(t) = e_i + \sum_{k=1}^{i-1} \left\lceil \frac{t}{p_k} \right\rceil e_k$$

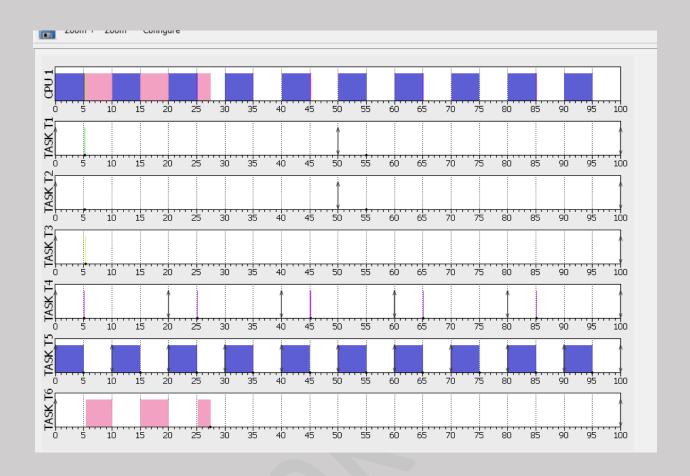
Worst cases >> 100ms

hyperperiod	Tasks	test	periodicity	Schedulable?
10	Load1	W1(10) =5ms+0=5ms	10ms	Yes
5	Uart	W2(20)=150us+(20/10)*5ms=10.15ms	20ms	Yes
2	BUT1	W3(50)=12us+(50/20)*150us+(50/10)*5=25.38	50ms	yes
2	BUT2	25.4	50ms	Yes
1	Periodic Transmitter	51	100ms	Yes
1	Load2	63.6	100ms	yes

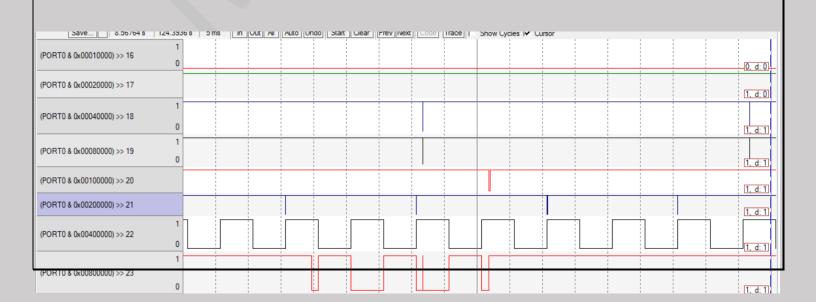
Simso

Qt M	Model data □ □ ※							
General Scheduler Processors Tasks								
id	Name	Task type	bort on mi	Date (Period (ms)	ct. da	dline	WCET (ms)
1	TASK T1	Periodic •	□No	0	50	-	50	0.012
2	TASK T2	Periodic •	□ No	0	50	-	50	.013
3	TASK T3	Periodic •	□ No	0	100	-	100	.14
4	TASK T4	Periodic •	□ No	0	20	-	20	.15
5	TASK T5	Periodic •	□ No	0	10	-	10	5
6	TASK T6	Periodic •	□No	0	100	-	100	12

	Total load	Payload	System load
CPU 1	0.6294	0.6294	0.0000
Average	0.6294	0.6294	0.0000



Kiel implementation



Save 8.56/64 s 1/24 	.3936 s 50 ms In Out All Auto Undo Start Clear Prev Next Lode I Show Cycles Cursor
(PORT0 & 0x00020000) >> 17	0. d: 01
(PORT0 & 0x00040000) >> 18	1 1 0 1 1 d.0 1 d.
(PORT0 & 0x00080000) >> 19	
(PORT0 & 0x00100000) >> 20	0 1 1 1 1 1 1 1 1 1
(PORT0 & 0x00200000) >> 21	
(PORT0 & 0x00400000) >> 22	
(PORT0 & 0x00800000) >> 23	