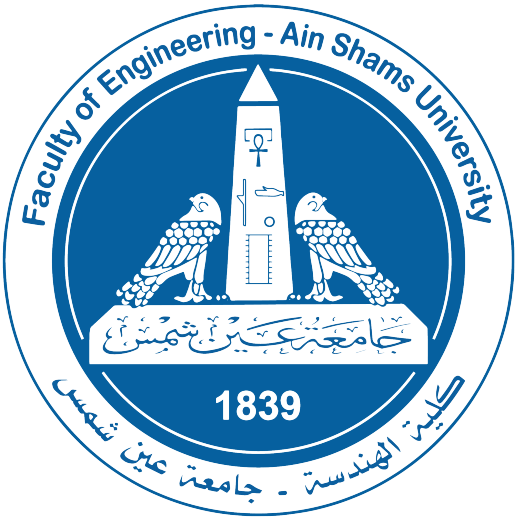

RDMA over Converged Ethernet

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0.1 Purpose of the controller

A passive component designed to resist changes in current. Inductors are often referred to as "AC resistors". The ability to resist changes in current and store energy in its magnetic field account for the bulk of the useful properties of inductors. Current passing through an inductor will produce a magnetic field. A changing magnetic field induces a voltage which opposes the field-producing current. This property of impeding changes of current is known as inductance. The voltage induced across an inductor by a change of current is defined as:

$$V = L\frac{di}{dt}$$

0.2 Features

- 33-bit address for 8 GB of address space.
- 16/32/64-bit data bus width support.
- CAS latencies: 5, 6, 7, 8, 9, 10, and 11.
- 1, 2, 4, and 8 internal banks.
- Burst Length: 8.
- Burst Type: sequential.
- 8GB address space available over one or two chip selects.
- Page sizes: 256, 512, 1024, and 2048-word.
- SDRAM auto initialization from reset or configuration change.
- Self-refresh mode.
- Prioritized refresh scheduling.
- Programmable SDRAM refresh rate and backlog counter.
- Programmable SDRAM timing parameters.
- Big and little endian modes.
- ECC on SDRAM data bus.
- 8-bit ECC per 64-bit data quanta without additional cycle latency.
- Two latency classes supported.
- UDIMM Address mirroring is not supported.

0.3 The DDR5 technology

1. Every command between the controller and the request must be in bursts (16 (columns or normal requests)).
2. There is small timing constrains between the commands in different bank groups.
3. The timing constrains between the two commands in the same bank is the largest then the two banks in the same bank group then the different bank groups.
4. There is timing constrains between writing to the memory and reading from it.

Chapter 1

Block Diagram

1.1 An overview of the basic structure

A passive component designed to resist changes in current. Inductors are often referred to as "AC resistors". The ability to resist changes in current and store energy in its magnetic field account for the bulk of the useful properties of inductors. Current passing through an inductor will produce a magnetic field. A changing magnetic field induces a voltage which opposes the field-producing current. This property of impeding changes of current is known as inductance. The voltage induced across an inductor by a change of current is defined as:

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Chapter 2

Architecture

2.1 Address Mapper

A Input: the full req.
dfdf

desicion: The main diff is that thread fair algo has higher priority to read requests while RLDP always focus on row hits,thus, it has too much transitions between reads and writes, so it leaves out the read queue and stall the system

1- The algo continues to write always if there is a row hit 2- if there is a row hit, then we switch to read queue. 3- Its the problem that we leave read queue if there is a row hit on write queue, so we decided to insert a new condition to delay this switching in future cycles and priotirzes the read queue higher than write drain.

we can switch to thread-fair algo later. we can jsut edit our flowchart in the lower branches and turn it into thread-fair!

2.2 The memory controller structure:

2.2.1 Mapper block:

Applies mapping scheme and gives every request special index

2.2.2 Returner block:

Waits for specific request index to return then it send it out of the controller if other requests come it saves it in it until its turn to be sent out comes

2.2.3 Over flow stopper block:

Make shore that there are no two requests in the controller have the same index

2.2.4 Request saver block:

Stores the request that came out from the mapper when the Modified FIFO block is full then send it as soon as there is place at the FIFO

2.2.5 Modified FIFO block:

It has two FIFO buffers inside one for the write request data (has low entries number) and another for the request type, address and index (with high entries number). It saves and assign the data if it's write request only

2.3 Refresh Management

A Buck converter takes the voltage from a DC source and converts the voltage of supply into lower DC voltage level. Some devices need a certain amount of voltage to run the device. Too much of power can destroy the device or less power may not be able to run the device.This output voltage is achieved by chopping the input voltage with a series of connected switches that apply pulses to an averaging inductor and capacitor circuit.

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