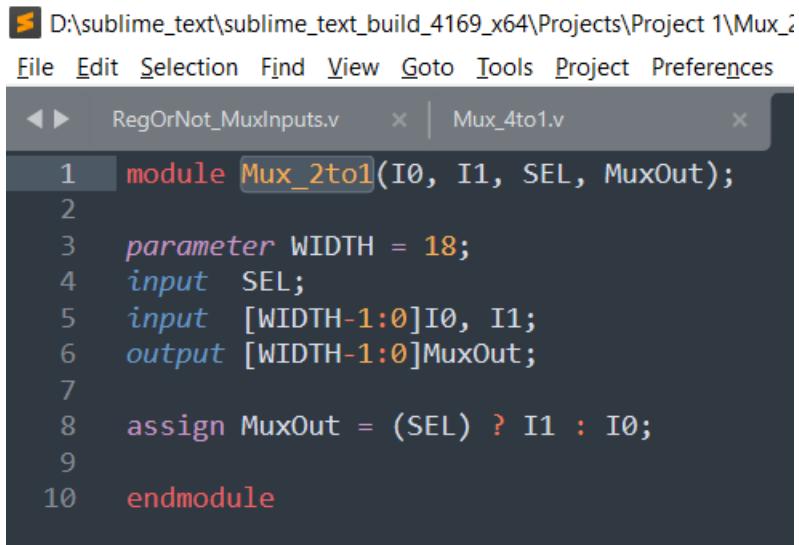


# Project 1

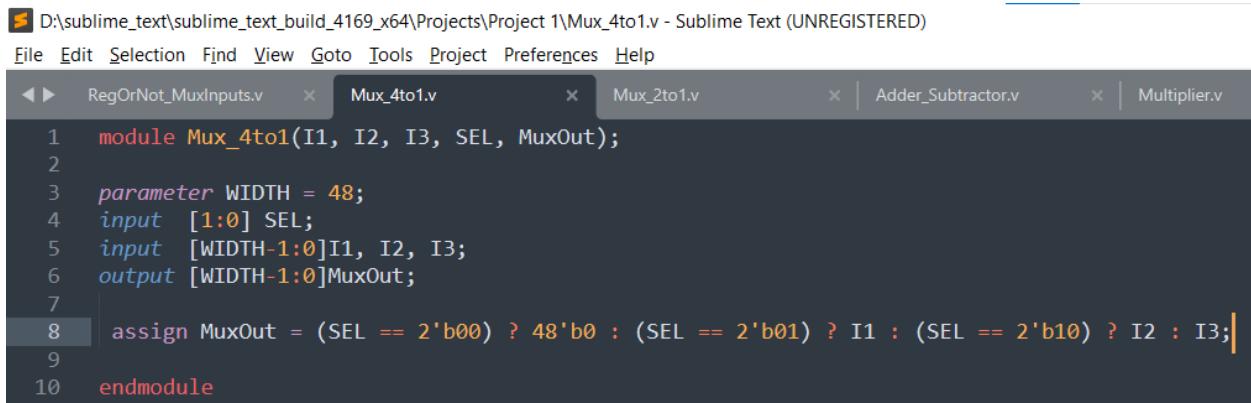
## RTL Code:

Instantiated Modules:



D:\sublime\_text\sublime\_text\_build\_4169\_x64\Projects\Project 1\Mux\_2to1.v

```
File Edit Selection Find View Goto Tools Project Preferences
◀ ▶ RegOrNot_MuxInputs.v × | Mux_4to1.v ×
1 module Mux_2to1(I0, I1, SEL, MuxOut);
2
3 parameter WIDTH = 18;
4 input SEL;
5 input [WIDTH-1:0]I0, I1;
6 output [WIDTH-1:0]MuxOut;
7
8 assign MuxOut = (SEL) ? I1 : I0;
9
10 endmodule
```



D:\sublime\_text\sublime\_text\_build\_4169\_x64\Projects\Project 1\Mux\_4to1.v - Sublime Text (UNREGISTERED)

```
File Edit Selection Find View Goto Tools Project Preferences Help
◀ ▶ RegOrNot_MuxInputs.v × Mux_4to1.v × Mux_2to1.v × | Adder_Subtractor.v × | Multiplier.v ×
1 module Mux_4to1(I1, I2, I3, SEL, MuxOut);
2
3 parameter WIDTH = 48;
4 input [1:0] SEL;
5 input [WIDTH-1:0]I1, I2, I3;
6 output [WIDTH-1:0]MuxOut;
7
8 assign MuxOut = (SEL == 2'b00) ? 48'b0 : (SEL == 2'b01) ? I1 : (SEL == 2'b10) ? I2 : I3;
9
10 endmodule
```

D:\sublime\_text\sublime\_text\_build\_4169\_x64\Projects\Project 1\Adder\_Subtractor.v - Sublir

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```
< > RegOrNot_MuxInputs.v x | Mux_4to1.v x | Mux_2to1.v
```

```
1 module Adder_Subtractor(A, B, CIN, OP, RESULT, COUT);
2
3 parameter WIDTH = 18;
4 input CIN, OP;
5 input [WIDTH-1:0]A, B;
6 output [WIDTH-1:0]RESULT;
7 output COUT;
8
9 assign {COUT, RESULT} = (OP) ? A-(B+CIN) : A+B+CIN;
10
11 endmodule
```

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```
< > RegOrNot_MuxInputs.v x | Mux_4to1.v
```

```
1 module Multiplier(A, B, OUT);
2
3 input [17:0]A, B;
4 output [35:0] OUT;
5
6 assign OUT = A*B;
7
8 endmodule
```

D:\sublime\_text\sublime\_text\_build\_4169\_x64\Projects\Project 1\RegOrNot\_MuxInputs.v - Sublime

File Edit Selection Find View Goto Tools Project Preferences Help

```
< > RegOrNot_MuxInputs.v x Mux_4to1.v x | Mux_2to1.v >
1 module RegOrNot_MuxInputs(D, EN, CLK, RST, SEL, MuxOut);
2
3 parameter WIDTH = 18;
4 parameter RSTTYPE = "SYNC";
5
6 input [WIDTH-1:0] D;
7 input CLK, EN, RST, SEL;
8 output [WIDTH-1:0] MuxOut;
9 reg [WIDTH-1:0] Q;
10
11 generate
12
13 if(RSTTYPE == "SYNC") begin
14     always @(posedge CLK) begin
15         if(RST) begin
16             Q <= 0;
17         end
18         else if(EN) begin
19             Q <= D;
20         end
21     end
22 end
23 else begin
24     always @(posedge CLK or posedge RST) begin
25         if(RST) begin
26             Q <= 0;
27         end
28         else if(EN) begin
29             Q <= D;
30         end
31     end
32 end
33
34 assign MuxOut = (SEL) ? Q : D;
35
36 endgenerate
37
38 endmodule
```

## Design Code:

D:\sublime\_text\sublime\_text\_build\_4169\_x64\Projects\Project 1\Spartan6\_DSP48A1.v - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

RegOrNot\_MuxInputs.v | Mux\_4to1.v | Mux\_2to1.v | Adder\_Subtractor.v | Multiplier.v | Spartan6\_DSP48A1.v

```

1 module Spartan6_DSP48A1(A, B, D, C, CLK, CARRYIN, OPMODE, BCIN, RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE,
2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
4 parameter A0REG = 0; parameter A1REG = 1; parameter B0REG = 0; parameter B1REG = 1;
5 parameter CREG = 1; parameter DREG = 1; parameter MREG = 1; parameter PREG = 1;
6 parameter CARRYINREG = 1; parameter CARRYOUTREG = 1; parameter OPMODEREG = 1;
7 parameter CARRYINSEL = "OPMODES"; parameter B_INPUT = "DIRECT"; parameter RSTTYPE = "SYNC";
8
9 input CLK, CARRYIN, RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE,
10 input [7:0]OPMODE;
11 input [17:0]A, B, BCIN;
12 input [47:0]C, PCIN;
13
14 output CARRYOUT, CARRYOUTF;
15 output [17:0]BCOUT;
16 output [35:0]M;
17 output [47:0]P, PCOUT;
18
19 wire [17:0]D_MuxOut, B0_MuxOut, A0_MuxOut, B1_MuxOut, A1_MuxOut;
20 wire [17:0]B_first_mux_out;
21 wire [17:0]Pre_Adder_Subtractor_Out, Pre_Adder_Subtractor_MuxOut;
22 wire [47:0]C_MuxOut;
23 wire [7:0]OPMODE_MuxOut;
24 wire CARRYIN CASCADE_MuxOut, CARRYIN_MuxOut;
25 wire [35:0]Multiplier_Out;
26 wire [35:0]M_MuxOut;
27 wire [47:0]X_MuxOut, Z_MuxOut;
28 wire [47:0]Post_Adder_Subtractor_Out;
29 wire Post_Adder_Subtractor_Cout;
30 wire [47:0]D_A_B_CONCATENATED;
```

D:\sublime\_text\sublime\_text\_build\_4169\_x64\Projects\Project 1\Spartan6\_DSP48A1.v - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

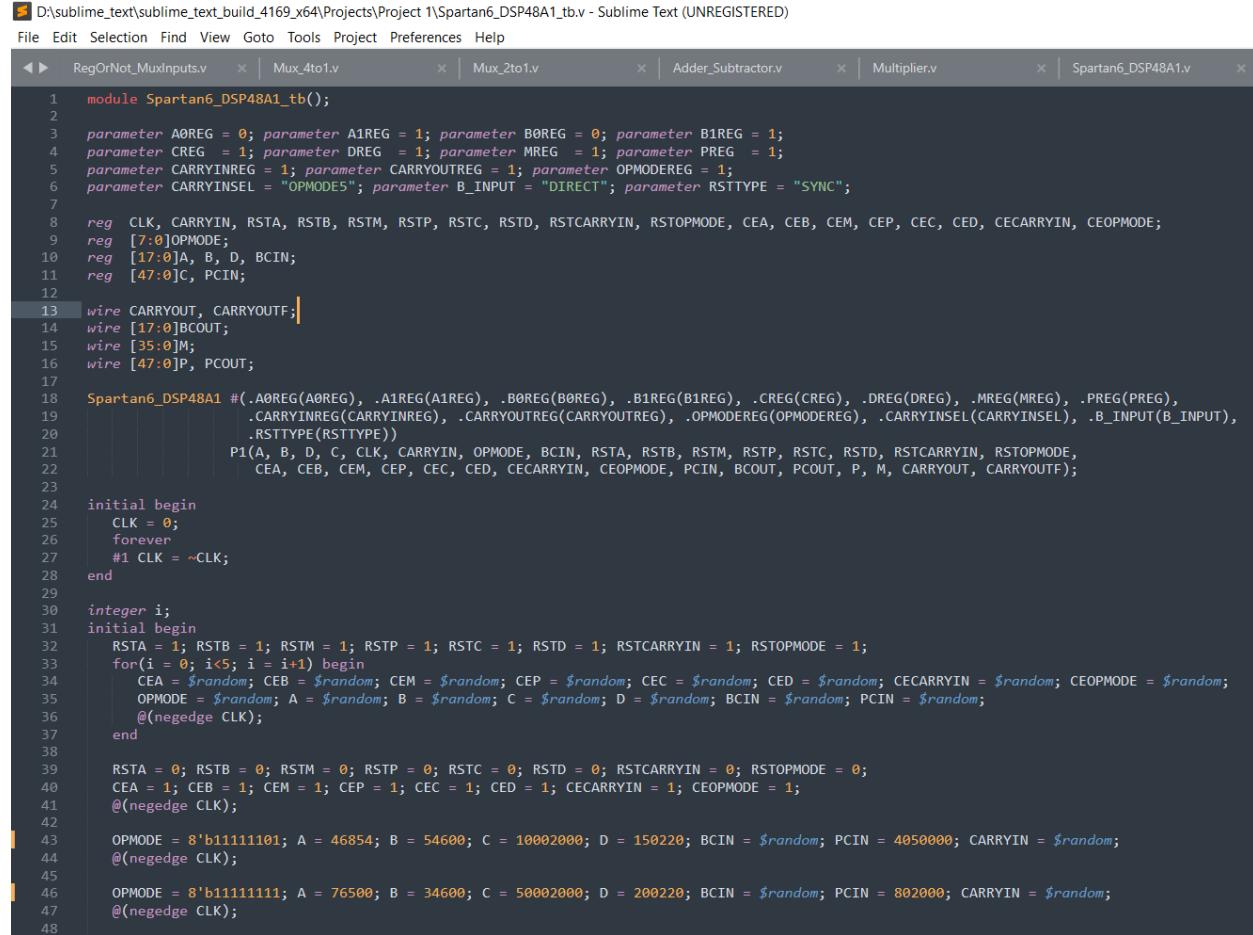
RegOrNot\_MuxInputs.v | Mux\_4to1.v | Mux\_2to1.v | Adder\_Subtractor.v | Multiplier.v | Spartan6\_DSP48A1.v | Spartan6\_DSP48A1\_tb.v | Co

```

31 RegOrNot_MuxInputs #(.(WIDTH(18)), .RSTTYPE(RSTTYPE)) I_D0(CED, CLK, RSTD, DREG, D_MuxOut);
32 RegOrNot_MuxInputs #(.(WIDTH(18)), .RSTTYPE(RSTTYPE)) I_B0(B_first_mux_out, CEB, CLK, RSTB, B0REG, B0_MuxOut);
33 RegOrNot_MuxInputs #(.(WIDTH(18)), .RSTTYPE(RSTTYPE)) I_A0(A, CEA, CLK, RSTA, A0REG, A0_MuxOut);
34 RegOrNot_MuxInputs #(.(WIDTH(48)), .RSTTYPE(RSTTYPE)) I_C(C, CEC, CLK, RSTC, CREG, C_MuxOut);
35 RegOrNot_MuxInputs #(.(WIDTH(8)), .RSTTYPE(RSTTYPE)) I_OPMODE(OPMODE, CEOPMODE, CLK, RSTOPMODE, OPMODEREG, OPMODE_MuxOut);
36
37 Adder_Subtractor #(.(WIDTH(18))) Pre_Adder_Subtractor(D_MuxOut, B0_MuxOut, 0, OPMODE_MuxOut[6], Pre_Adder_Subtractor_Out);
38 Mux_2to1 #(.(WIDTH(18))) Pre_Adder_Subtractor_MUX(B0_MuxOut, Pre_Adder_Subtractor_Out, OPMODE_MuxOut[4], Pre_Adder_Subtractor_MuxOut);
39
40 RegOrNot_MuxInputs #(.(WIDTH(18)), .RSTTYPE(RSTTYPE)) I_B1(Pre_Adder_Subtractor_MuxOut, CEB, CLK, RSTB, B1REG, B1_MuxOut);
41 RegOrNot_MuxInputs #(.(WIDTH(18)), .RSTTYPE(RSTTYPE)) I_A1(A0_MuxOut, CEA, CLK, RSTA, A1REG, A1_MuxOut);
42
43 Multiplier I_MUL(A1_MuxOut, B1_MuxOut, Multiplier_Out);
44 RegOrNot_MuxInputs #(.(WIDTH(36)), .RSTTYPE(RSTTYPE)) I_M(Multiplier_Out, CEM, CLK, RSTM, MREG, M_MuxOut);
45 RegOrNot_MuxInputs #(.(WIDTH(1)), .RSTTYPE(RSTTYPE)) I_CARRYIN(CARRYIN CASCADE_MuxOut, CECARRYIN, CLK, RSTCARRYIN, CARRYINREG, CARRYIN_MuxOut);
46
47 Mux_4to1 #(.(WIDTH(48))) I_Mux_X({12'b0, M_MuxOut}, P, D_A_B_CONCATENATED, OPMODE_MuxOut[1:0], X_MuxOut);
48 Mux_4to1 #(.(WIDTH(48))) I_Mux_Z(PCIN, P, C_MuxOut, OPMODE_MuxOut[3:2], Z_MuxOut);
49
50 Adder_Subtractor #(.(WIDTH(48))) Post_Adder_Subtractor(Z_MuxOut, X_MuxOut, CARRYIN_MuxOut, OPMODE_MuxOut[7], Post_Adder_Subtractor_Out, Post_Adder_Subtractor_Cout);
51 RegOrNot_MuxInputs #(.(WIDTH(1)), .RSTTYPE(RSTTYPE)) I_CARRYOUT(Post_Adder_Subtractor_Cout, CECARRYIN, CLK, RSTCARRYIN, CARRYOUTREG, CARRYOUT);
52 RegOrNot_MuxInputs #(.(WIDTH(48)), .RSTTYPE(RSTTYPE)) I_P(Post_Adder_Subtractor_Out, CEP, CLK, RSTP, PREG, P);
53
54 assign B_first_mux_out = (B_INPUT == "DIRECT") ? B : (B_INPUT == "CASCADE") ? BCIN : 0;
55
56 assign CARRYIN CASCADE_MuxOut = (CARRYINSEL == "OPMODES") ? OPMODE_MuxOut[5] : (CARRYINSEL == "CARRYIN") ? CARRYIN : 0;
57
58 assign BCOUT = B1_MuxOut;
59 assign D_A_B_CONCATENATED = {D[11:0], A, B};
60 assign M = M_MuxOut;
61 assign CARRYOUTF = CARRYOUT;
62 assign PCOUT = P;
63
64
65 endmodule
```

# Testbench Code:

## TB\_Code:



```
1 module Spartan6_DSP48A1_tb();
2
3 parameter A0REG = 0; parameter A1REG = 1; parameter B0REG = 0; parameter B1REG = 1;
4 parameter CREG = 1; parameter DREG = 1; parameter MREG = 1; parameter PREG = 1;
5 parameter CARRYINREG = 1; parameter CARRYOUTREG = 1; parameter OPMODEREG = 1;
6 parameter CARRYINSEL = "OPMODE5"; parameter B_INPUT = "DIRECT"; parameter RSTTYPE = "SYNC";
7
8 reg CLK, CARRYIN, RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE, CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE;
9 reg [7:0]OPMODE;
10 reg [17:0]A, B, D, BCIN;
11 reg [47:0]C, PCIN;
12
13 wire CARRYOUT, CARRYOUTF;
14 wire [17:0]BCOUT;
15 wire [35:0]M;
16 wire [47:0]P, PCOUT;
17
18 Spartan6_DSP48A1 #( .A0REG(A0REG), .A1REG(A1REG), .B0REG(B0REG), .B1REG(B1REG), .CREG(CREG), .DREG(DREG), .MREG(MREG), .PREG(PREG),
19 .CARRYINREG(CARRYINREG), .CARRYOUTREG(CARRYOUTREG), .OPMODEREG(OPMODEREG), .CARRYINSEL(CARRYINSEL), .B_INPUT(B_INPUT),
20 .RSTTYPE(RSTTYPE))
21     P1(A, B, D, C, CLK, CARRYIN, OPMODE, BCIN, RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE,
22     CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE, PCIN, BCOUT, PCOUT, P, M, CARRYOUT, CARRYOUTF);
23
24 initial begin
25     CLK = 0;
26     forever
27         #1 CLK = ~CLK;
28 end
29
30 integer i;
31 initial begin
32     RSTA = 1; RSTB = 1; RSTM = 1; RSTP = 1; RSTC = 1; RSTD = 1; RSTCARRYIN = 1; RSTOPMODE = 1;
33     for(i = 0; i<5; i = i+1) begin
34         CEA = $random; CEB = $random; CEM = $random; CEP = $random; CEC = $random; CED = $random; CECARRYIN = $random; CEOPMODE = $random;
35         OPMODE = $random; A = $random; B = $random; C = $random; D = $random; BCIN = $random; PCIN = $random;
36         @(negedge CLK);
37     end
38
39     RSTA = 0; RSTB = 0; RSTM = 0; RSTP = 0; RSTC = 0; RSTD = 0; RSTCARRYIN = 0; RSTOPMODE = 0;
40     CEA = 1; CEB = 1; CEM = 1; CEP = 1; CEC = 1; CED = 1; CECARRYIN = 1; CEOPMODE = 1;
41     @(negedge CLK);
42
43     OPMODE = 8'b11111101; A = 46854; B = 54600; C = 10002000; D = 150220; BCIN = $random; PCIN = 4050000; CARRYIN = $random;
44     @(negedge CLK);
45
46     OPMODE = 8'b11111111; A = 76500; B = 34600; C = 50002000; D = 200220; BCIN = $random; PCIN = 802000; CARRYIN = $random;
47     @(negedge CLK);
48
```

```

49 OPMODE = 8'b11110101; A = 6730; B = 8420; C = 1804400; D = 240500; BCIN = $random; PCIN = 4597800; CARRYIN = $random;
50 @(negedge CLK);
51
52 OPMODE = 8'b11110111; A = 78940; B = 35100; C = 500800; D = 79120; BCIN = $random; PCIN = 879797; CARRYIN = $random;
53 @(negedge CLK);
54
55 OPMODE = 8'b11111001; A = 13320; B = 70800; C = 460000; D = 120600; BCIN = $random; PCIN = 320000; CARRYIN = $random;
56 @(negedge CLK);
57
58 OPMODE = 8'b11111011; A = 54000; B = 3700; C = 142500; D = 15020; BCIN = $random; PCIN = 7641000; CARRYIN = $random;
59 @(negedge CLK);
60
61 OPMODE = 8'b11111110; A = 2013; B = 43610; C = 1346200; D = 127820; BCIN = $random; PCIN = 4561320; CARRYIN = $random;
62 @(negedge CLK);
63
64 OPMODE = 8'b00111101; A = 46854; B = 54600; C = 10002000; D = 150220; BCIN = $random; PCIN = 4050000; CARRYIN = $random;
65 @(negedge CLK);
66
67 OPMODE = 8'b00111111; A = 76500; B = 34600; C = 50002000; D = 200220; BCIN = $random; PCIN = 802000; CARRYIN = $random;
68 @(negedge CLK);
69
70 OPMODE = 8'b00110101; A = 6730; B = 8420; C = 1804400; D = 240500; BCIN = $random; PCIN = 4597800; CARRYIN = $random;
71 @(negedge CLK);
72
73 OPMODE = 8'b00110111; A = 78940; B = 35100; C = 500800; D = 79120; BCIN = $random; PCIN = 879797; CARRYIN = $random;
74 @(negedge CLK);
75
76 OPMODE = 8'b00111001; A = 13320; B = 70800; C = 460000; D = 120600; BCIN = $random; PCIN = 320000; CARRYIN = $random;
77 @(negedge CLK);
78
79 OPMODE = 8'b00111011; A = 54000; B = 3700; C = 142500; D = 15020; BCIN = $random; PCIN = 7641000; CARRYIN = $random;
80 @(negedge CLK);
81
82 OPMODE = 8'b00111110; A = 2013; B = 43610; C = 1346200; D = 127820; BCIN = $random; PCIN = 4561320; CARRYIN = $random;
83 @(negedge CLK);
84
85 OPMODE = 8'b11001101; A = 46854; B = 54600; C = 10002000; D = 150220; BCIN = $random; PCIN = 4050000; CARRYIN = $random;
86 @(negedge CLK);
87
88 OPMODE = 8'b11001111; A = 76500; B = 34600; C = 50002000; D = 200220; BCIN = $random; PCIN = 802000; CARRYIN = $random;
89
90 OPMODE = 8'b11000101; A = 6730; B = 8420; C = 1804400; D = 240500; BCIN = $random; PCIN = 4597800; CARRYIN = $random;
91 @(negedge CLK);
92
93 OPMODE = 8'b11000111; A = 78940; B = 35100; C = 500800; D = 79120; BCIN = $random; PCIN = 879797; CARRYIN = $random;
94 @(negedge CLK);
95

```

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```

96
97 OPMODE = 8'b11001001; A = 13320; B = 70800; C = 460000; D = 120600; BCIN = $random; PCIN = 320000; CARRYIN = $random;
98 @ (negedge CLK);
99
100 OPMODE = 8'b11001011; A = 54000; B = 3700; C = 142500; D = 15020; BCIN = $random; PCIN = 7641000; CARRYIN = $random;
101 @ (negedge CLK);
102
103 OPMODE = 8'b11001110; A = 2013; B = 43610; C = 1346200; D = 127820; BCIN = $random; PCIN = 4561320; CARRYIN = $random;
104 @ (negedge CLK);
105
106 OPMODE = 8'b00001101; A = 46854; B = 54600; C = 10002000; D = 150220; BCIN = $random; PCIN = 4050000; CARRYIN = $random;
107 @ (negedge CLK);
108
109 OPMODE = 8'b00001111; A = 76500; B = 34600; C = 50002000; D = 200220; BCIN = $random; PCIN = 802000; CARRYIN = $random;
110 @ (negedge CLK);
111
112 OPMODE = 8'b0000101; A = 6730; B = 8420; C = 1804400; D = 240500; BCIN = $random; PCIN = 4597800; CARRYIN = $random;
113 @ (negedge CLK);
114
115 OPMODE = 8'b00001111; A = 78940; B = 35100; C = 500800; D = 79120; BCIN = $random; PCIN = 879797; CARRYIN = $random;
116 @ (negedge CLK);
117
118 OPMODE = 8'b00001001; A = 13320; B = 70800; C = 460000; D = 120600; BCIN = $random; PCIN = 320000; CARRYIN = $random;
119 @ (negedge CLK);
120
121 OPMODE = 8'b00001011; A = 54000; B = 3700; C = 142500; D = 15020; BCIN = $random; PCIN = 7641000; CARRYIN = $random;
122 @ (negedge CLK);
123
124 OPMODE = 8'b00001110; A = 2013; B = 43610; C = 1346200; D = 127820; BCIN = $random; PCIN = 4561320; CARRYIN = $random;
125 @ (negedge CLK);
126
127 $stop;
128
129 end
130
131 endmodule

```

## Do File:

run - Notepad

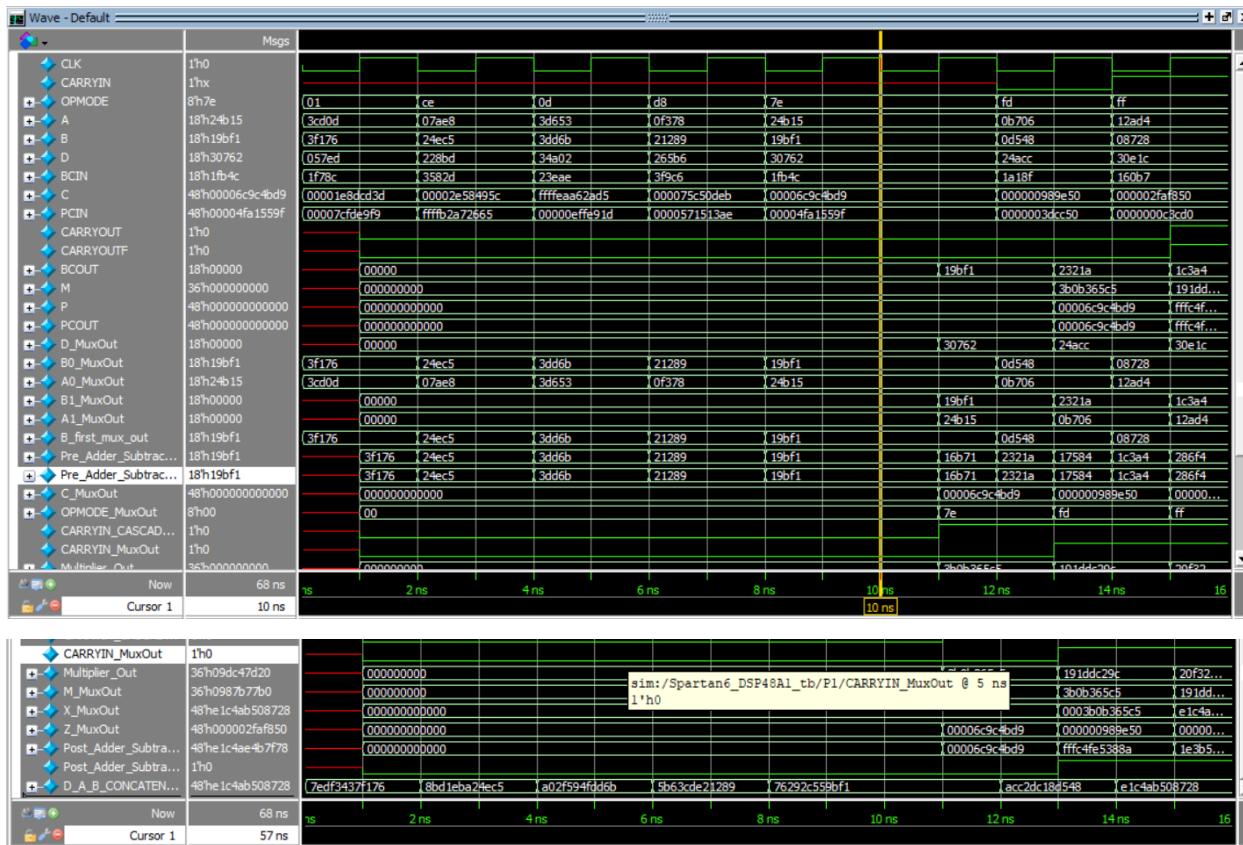
File Edit Format View Help

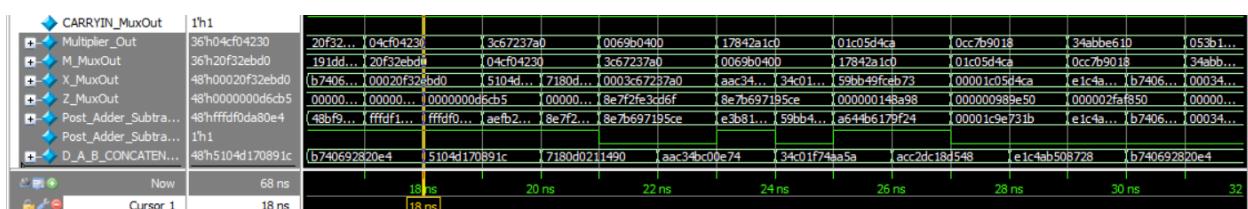
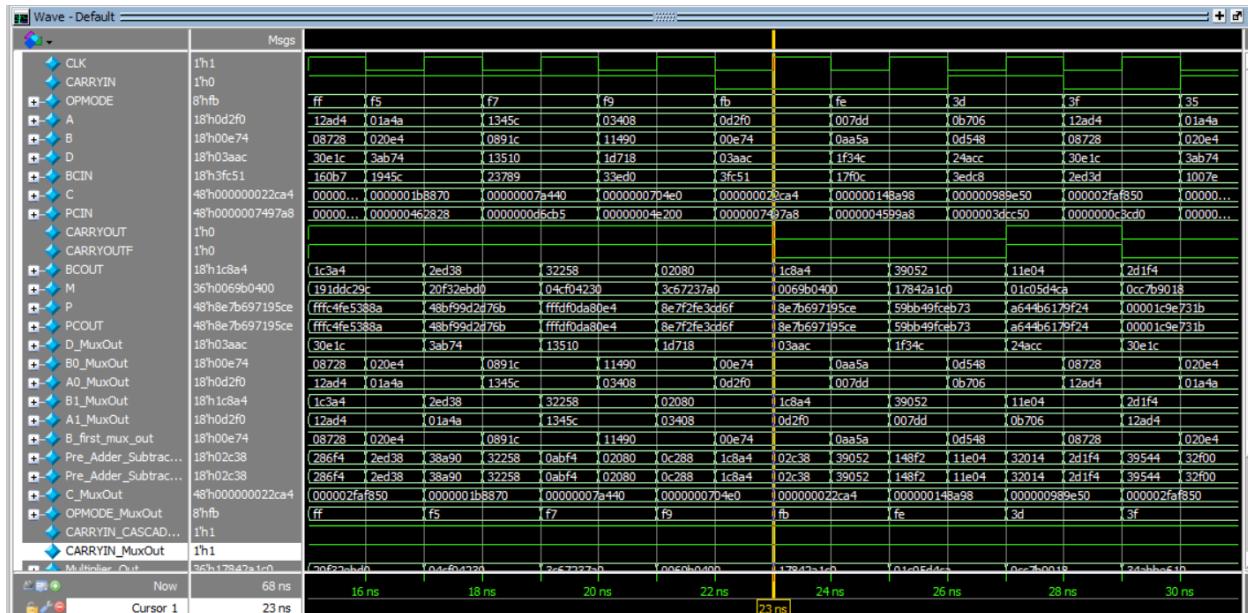
```

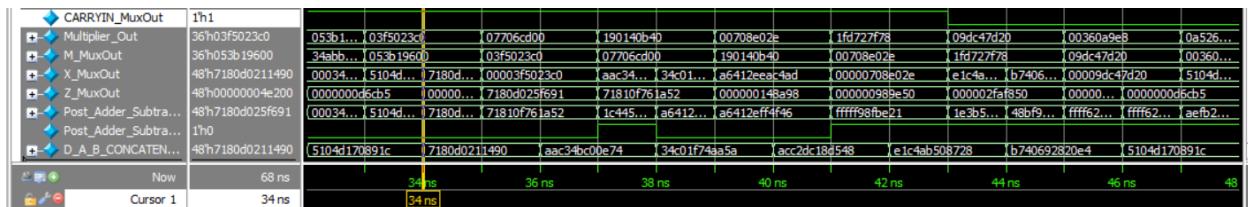
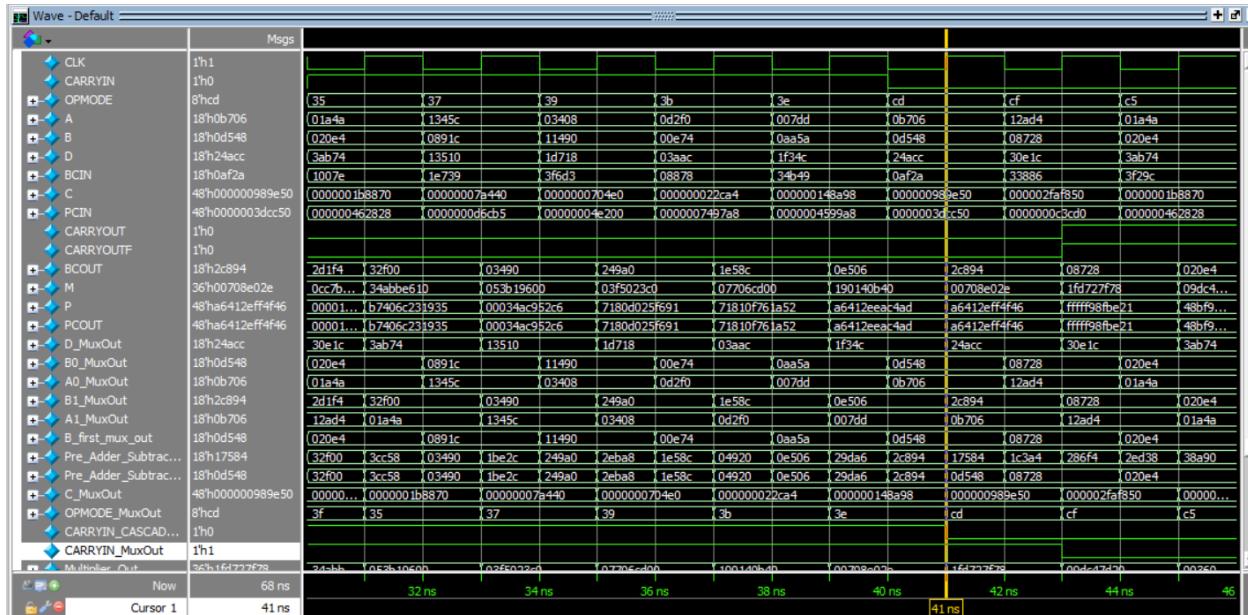
vlib work
vlog RegOrNot_MuxInputs.v Mux_2to1.v Mux_4to1.v Adder_Subtractor.v Multiplier.v Spartan6_DSP48A1.v Spartan6_DSP48A1_tb.v
vsim -voptargs+=acc work.Spartan6_DSP48A1_tb
add wave *
run -all
#quit -sim

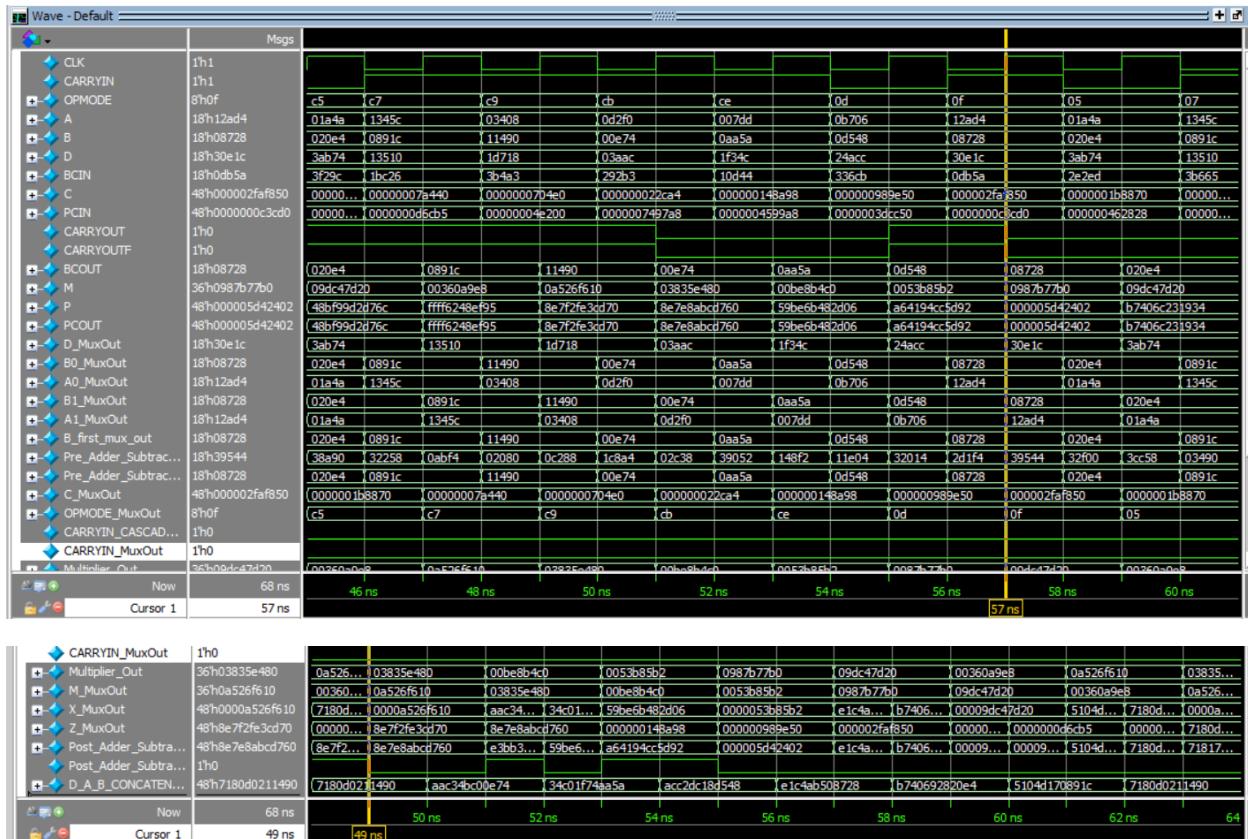
```

# QuestaSim Snippets:









# Constraint File:

D:\sublime\_text\sublime\_text\_build\_4169\_x64\Projects\Project 1\Constraints\_basys3.xdc - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

RegOrNot\_MuxInputs.v | Mux\_4to1.v | Mux\_2to1.v | Adder\_Subtractor.v | Multiplier.v

```
1 ## This file is a general .xdc for the Basys3 rev B board
2 ## To use it in a project:
3 ## - uncomment the lines corresponding to used pins
4 ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6 ## Clock signal
7 set_property -dict {PACKAGE_PIN W5 IO_STANDARD LVCMOS33} [get_ports CLK]
8 create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports CLK]
9
```

D:\sublime\_text\sublime\_text\_build\_4169\_x64\Projects\Project 1\Constraints\_basys3.xdc - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

RegOrNot\_MuxInputs.v | Mux\_4to1.v | Mux\_2to1.v | Adder\_Subtractor.v | Multiplier.v | Spartan6\_DSP48A1.v | Spartan6\_DSP48A1\_tb.v | Constraints\_basys3.xdc

```
151 ## Configuration options, can be used for all designs
152 set_property CONFIG_VOLTAGE 3.3 [current_design]
153 set_property CFGBVS VCCO [current_design]
154
155 ## SPI configuration mode options for QSPI boot, can be used for all designs
156 set_property BITSSTREAM_GENERAL_COMPRESS TRUE [current_design]
157 set_property BITSSTREAM_CONFIG_CONFIGRATE 33 [current_design]
158 set_property CONFIG_MODE SPIx4 [current_design]
159
160 create_debug_core u_ilia_0 ilia
161 set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ilia_0]
162 set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ilia_0]
163 set_property ALL_PROBE_SAME_MU_SEL 0 [get_debug_cores u_ilia_0]
164 set_property C_DATA_DEPTH 1024 [get_debug_cores u_ilia_0]
165 set_property C_EN_STRG_QUAL False [get_debug_cores u_ilia_0]
166 set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ilia_0]
167 set_property C_TRIGGER_EN False [get_debug_cores u_ilia_0]
168 set_property C_TRIGGER_EN false [get_debug_cores u_ilia_0]
169 set_property C_TRIGGER_EN false [get_debug_cores u_ilia_0]
170 set_property C_TRIGGER_EN false [get_debug_cores u_ilia_0]
171 connect_debug_port u_ilia_0/clock [get_nets [list CLK_IBUF_BUFG]]
172 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe0]
173 set_property port_width 18 [get_debug_ports u_ilia_0/probe0]
174 connect_debug_port u_ilia_0/probe0 [get_nets [list {A_IBUF[0]} {A_IBUF[1]} {A_IBUF[2]} {A_IBUF[3]} {A_IBUF[4]} {A_IBUF[5]} {A_IBUF[6]} {A_IBUF[7]} {A_IBUF[8]} {A_IBUF[9]} {A_IBUF[10]} {A_IBUF[11]} {A_IBUF[12]} {A_IBUF[13]} {A_IBUF[14]} {A_IBUF[15]} {A_IBUF[16]} {A_IBUF[17]}]]
175 create_debug_port u_ilia_0 probe
176 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe1]
177 set_property port_width 18 [get_debug_ports u_ilia_0/probe1]
178 connect_debug_port u_ilia_0/probe1 [get_nets [list {D_IBUF[0]} {D_IBUF[1]} {D_IBUF[2]} {D_IBUF[3]} {D_IBUF[4]} {D_IBUF[5]} {D_IBUF[6]} {D_IBUF[7]} {D_IBUF[8]} {D_IBUF[9]} {D_IBUF[10]} {D_IBUF[11]} {D_IBUF[12]} {D_IBUF[13]} {D_IBUF[14]} {D_IBUF[15]} {D_IBUF[16]} {D_IBUF[17]}]]
179 create_debug_port u_ilia_0 probe
180 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe2]
181 set_property port_width 18 [get_debug_ports u_ilia_0/probe2]
182 connect_debug_port u_ilia_0/probe2 [get_nets [list {B_IBUF[0]} {B_IBUF[1]} {B_IBUF[2]} {B_IBUF[3]} {B_IBUF[4]} {B_IBUF[5]} {B_IBUF[6]} {B_IBUF[7]} {B_IBUF[8]} {B_IBUF[9]} {B_IBUF[10]} {B_IBUF[11]} {B_IBUF[12]} {B_IBUF[13]} {B_IBUF[14]} {B_IBUF[15]} {B_IBUF[16]} {B_IBUF[17]}]]
183 create_debug_port u_ilia_0 probe
184 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe3]
185 connect_debug_port u_ilia_0/probe3 [get_nets [list {BCOUT_OBUF[0]} {BCOUT_OBUF[1]} {BCOUT_OBUF[2]} {BCOUT_OBUF[3]} {BCOUT_OBUF[4]} {BCOUT_OBUF[5]} {BCOUT_OBUF[6]} {BCOUT_OBUF[7]} {BCOUT_OBUF[8]} {BCOUT_OBUF[9]} {BCOUT_OBUF[10]} {BCOUT_OBUF[11]} {BCOUT_OBUF[12]} {BCOUT_OBUF[13]} {BCOUT_OBUF[14]} {BCOUT_OBUF[15]} {BCOUT_OBUF[16]} {BCOUT_OBUF[17]}]]
186 create_debug_port u_ilia_0 probe
187 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe4]
188 set_property port_width 18 [get_debug_ports u_ilia_0/probe4]
189 connect_debug_port u_ilia_0/probe4 [get_nets [list {M_OBUF[0]} {M_OBUF[1]} {M_OBUF[2]} {M_OBUF[3]} {M_OBUF[4]} {M_OBUF[5]} {M_OBUF[6]} {M_OBUF[7]} {M_OBUF[8]} {M_OBUF[9]} {M_OBUF[10]} {M_OBUF[11]} {M_OBUF[12]} {M_OBUF[13]} {M_OBUF[14]} {M_OBUF[15]} {M_OBUF[16]} {M_OBUF[17]} {M_OBUF[18]} {M_OBUF[19]} {M_OBUF[20]} {M_OBUF[21]} {M_OBUF[22]} {M_OBUF[23]} {M_OBUF[24]} {M_OBUF[25]} {M_OBUF[26]} {M_OBUF[27]} {M_OBUF[28]} {M_OBUF[29]} {M_OBUF[30]} {M_OBUF[31]} {M_OBUF[32]} {M_OBUF[33]} {M_OBUF[34]} {M_OBUF[35]}]]
190 create_debug_port u_ilia_0 probe
191 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ilia_0/probe5]
192 set_property port_width 18 [get_debug_ports u_ilia_0/probe5]
193 connect_debug_port u_ilia_0/probe5 [get_nets [list {PCIN_IBUF[0]} {PCIN_IBUF[1]} {PCIN_IBUF[2]} {PCIN_IBUF[3]} {PCIN_IBUF[4]} {PCIN_IBUF[5]} {PCIN_IBUF[6]} {PCIN_IBUF[7]} {PCIN_IBUF[8]} {PCIN_IBUF[9]} {PCIN_IBUF[10]} {PCIN_IBUF[11]} {PCIN_IBUF[12]} {PCIN_IBUF[13]} {PCIN_IBUF[14]} {PCIN_IBUF[15]} {PCIN_IBUF[16]} {PCIN_IBUF[17]} {PCIN_IBUF[18]} {PCIN_IBUF[19]} {PCIN_IBUF[20]} {PCIN_IBUF[21]} {PCIN_IBUF[22]} {PCIN_IBUF[23]} {PCIN_IBUF[24]} {PCIN_IBUF[25]} {PCIN_IBUF[26]} {PCIN_IBUF[27]} {PCIN_IBUF[28]} {PCIN_IBUF[29]} {PCIN_IBUF[30]} {PCIN_IBUF[31]} {PCIN_IBUF[32]} {PCIN_IBUF[33]} {PCIN_IBUF[34]} {PCIN_IBUF[35]} {PCIN_IBUF[36]} {PCIN_IBUF[37]} {PCIN_IBUF[38]} {PCIN_IBUF[39]} {PCIN_IBUF[40]} {PCIN_IBUF[41]} {PCIN_IBUF[42]} {PCIN_IBUF[43]} {PCIN_IBUF[44]} {PCIN_IBUF[45]} {PCIN_IBUF[46]} {PCIN_IBUF[47]}]]
```

Line 218, Column 50 Tab Size: 4

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File Edit Selection Find Goto Tools Project Preferences Help

RegOrNot\_MuxInputs.v | Mux\_4to1.v | Mux\_2to1.v | Adder\_Subtractor.v | Multiplier.v | Spartan6\_DSP48A1.v | Spartan6\_DSP48A1\_tb.v | Constraints\_basys3.xdc

```

209 create_debug_port u_il0_0 probe
210 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe6]
211 set_property port_width 48 [get_debug_ports u_il0_0/probe6]
212 connect_debug_port u_il0_0/probe6 [get_nets [list {P_OBUF[0]} {P_OBUF[1]} {P_OBUF[2]} {P_OBUF[3]} {P_OBUF[4]} {P_OBUF[5]} {P_OBUF[6]} {P_OBUF[7]} {P_OBUF[8]} {P_OBUF[9]} {P_OBUF[10]} {P_OBUF[11]} {P_OBUF[12]} {P_OBUF[13]} {P_OBUF[14]} {P_OBUF[15]} {P_OBUF[16]} {P_OBUF[17]} {P_OBUF[18]} {P_OBUF[19]} {P_OBUF[20]} {P_OBUF[21]} {P_OBUF[22]} {P_OBUF[23]} {P_OBUF[24]} {P_OBUF[25]} {P_OBUF[26]} {P_OBUF[27]} {P_OBUF[28]} {P_OBUF[29]} {P_OBUF[30]} {P_OBUF[31]} {P_OBUF[32]} {P_OBUF[33]} {P_OBUF[34]} {P_OBUF[35]} {P_OBUF[36]} {P_OBUF[37]} {P_OBUF[38]} {P_OBUF[39]} {P_OBUF[40]} {P_OBUF[41]} {P_OBUF[42]} {P_OBUF[43]} {P_OBUF[44]} {P_OBUF[45]} {P_OBUF[46]} {P_OBUF[47]}]]
213 create_debug_port u_il0_0 probe
214 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe7]
215 set_property port_width 48 [get_debug_ports u_il0_0/probe7]
216 connect_debug_port u_il0_0/probe7 [get_nets [list {C_IBUF[0]} {C_IBUF[1]} {C_IBUF[2]} {C_IBUF[3]} {C_IBUF[4]} {C_IBUF[5]} {C_IBUF[6]} {C_IBUF[7]} {C_IBUF[8]} {C_IBUF[9]} {C_IBUF[10]} {C_IBUF[11]} {C_IBUF[12]} {C_IBUF[13]} {C_IBUF[14]} {C_IBUF[15]} {C_IBUF[16]} {C_IBUF[17]} {C_IBUF[18]} {C_IBUF[19]} {C_IBUF[20]} {C_IBUF[21]} {C_IBUF[22]} {C_IBUF[23]} {C_IBUF[24]} {C_IBUF[25]} {C_IBUF[26]} {C_IBUF[27]} {C_IBUF[28]} {C_IBUF[29]} {C_IBUF[30]} {C_IBUF[31]} {C_IBUF[32]} {C_IBUF[33]} {C_IBUF[34]} {C_IBUF[35]} {C_IBUF[36]} {C_IBUF[37]} {C_IBUF[38]} {C_IBUF[39]} {C_IBUF[40]} {C_IBUF[41]} {C_IBUF[42]} {C_IBUF[43]} {C_IBUF[44]} {C_IBUF[45]} {C_IBUF[46]} {C_IBUF[47]}]]
217 create_debug_port u_il0_0 probe
218 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe8]
219 set_property port_width 8 [get_debug_ports u_il0_0/probe8]
220 connect_debug_port u_il0_0/probe8 [get_nets [list {OPMODE_IBUF[0]} {OPMODE_IBUF[1]} {OPMODE_IBUF[2]} {OPMODE_IBUF[3]} {OPMODE_IBUF[4]} {OPMODE_IBUF[5]} {OPMODE_IBUF[6]} {OPMODE_IBUF[7]}]]
221 create_debug_port u_il0_0 probe
222 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe9]
223 set_property port_width 1 [get_debug_ports u_il0_0/probe9]
224 connect_debug_port u_il0_0/probe9 [get_nets [list {CARRYOUT_IBUF}]]
225 create_debug_port u_il0_0 probe
226 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe10]
227 set_property port_width 1 [get_debug_ports u_il0_0/probe10]
228 connect_debug_port u_il0_0/probe10 [get_nets [list {CEA_IBUF}]]
229 create_debug_port u_il0_0 probe
230 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe11]
231 set_property port_width 1 [get_debug_ports u_il0_0/probe11]
232 connect_debug_port u_il0_0/probe11 [get_nets [list {CEB_IBUF}]]
233 create_debug_port u_il0_0 probe
234 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe12]
235 set_property port_width 1 [get_debug_ports u_il0_0/probe12]
236 connect_debug_port u_il0_0/probe12 [get_nets [list {CEC_IBUF}]]
237 create_debug_port u_il0_0 probe
238 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe13]
239 set_property port_width 1 [get_debug_ports u_il0_0/probe13]
240 connect_debug_port u_il0_0/probe13 [get_nets [list {CEARIN_IBUF}]]
241 create_debug_port u_il0_0 probe
242 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe14]
243 set_property port_width 1 [get_debug_ports u_il0_0/probe14]
244 connect_debug_port u_il0_0/probe14 [get_nets [list {CEO_IBUF}]]
245 create_debug_port u_il0_0 probe
246 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe15]
247 set_property port_width 1 [get_debug_ports u_il0_0/probe15]
248 connect_debug_port u_il0_0/probe15 [get_nets [list {CEH_IBUF}]]
249 create_debug_port u_il0_0 probe
250 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe16]
251 set_property port_width 1 [get_debug_ports u_il0_0/probe16]
252 connect_debug_port u_il0_0/probe16 [get_nets [list {CEOOPMODE_IBUF}]]
253 create_debug_port u_il0_0 probe
254 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_il0_0/probe17]
255 set_property port_width 1 [get_debug_ports u_il0_0/probe17]
256 connect_debug_port u_il0_0/probe17 [get_nets [list {CEP_IBUF}]]

```

Line 218, Column 50

D:\sublime\_text\sublime\_text\_build\_4169\_x64\Projects\Project 1\Constraints\_basys3.xdc • - Sublime Text (UNF)

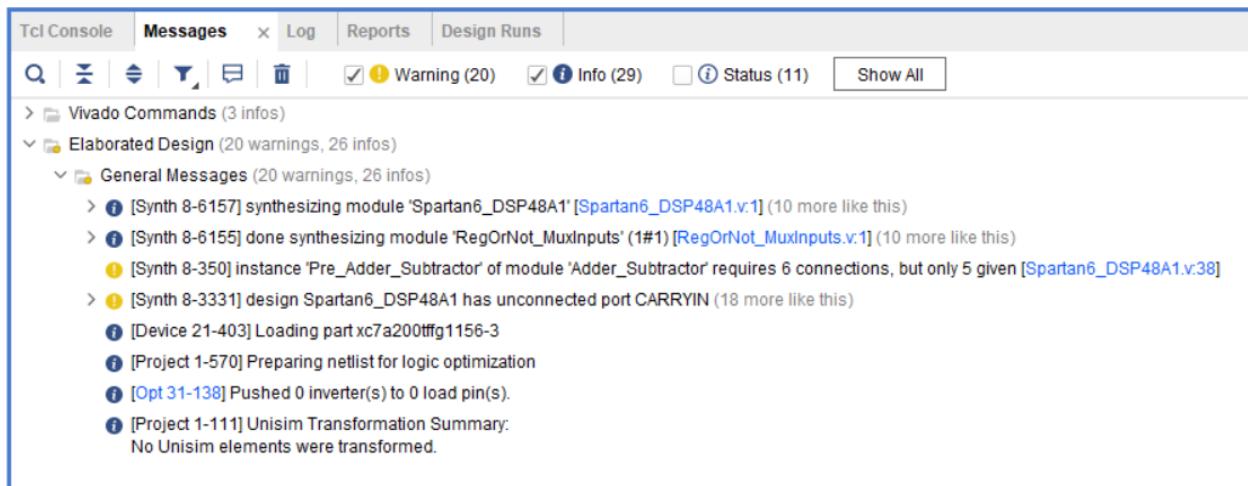
File Edit Selection Find View Goto Tools Project Preferences Help

```
RegOrNot_MuxInputs.v      Mux_4to1.v      Mux_2to1.v      Adder_...
```

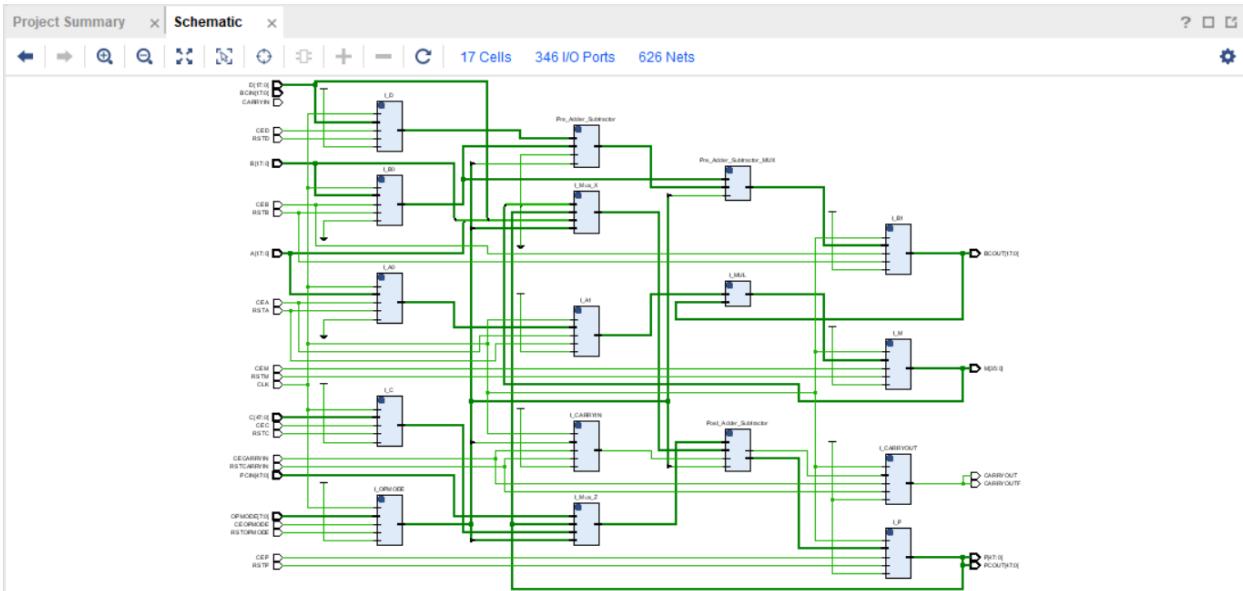
```
259 create_debug_port u_ila_0 probe
260 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
261 set_property port_width 1 [get_debug_ports u_ila_0/probe18]
262 connect_debug_port u_ila_0/probe18 [get_nets [list CLK_IBUF]]
263 create_debug_port u_ila_0 probe
264 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
265 set_property port_width 1 [get_debug_ports u_ila_0/probe19]
266 connect_debug_port u_ila_0/probe19 [get_nets [list RSTA_IBUF]]
267 create_debug_port u_ila_0 probe
268 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
269 set_property port_width 1 [get_debug_ports u_ila_0/probe20]
270 connect_debug_port u_ila_0/probe20 [get_nets [list RSTB_IBUF]]
271 create_debug_port u_ila_0 probe
272 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
273 set_property port_width 1 [get_debug_ports u_ila_0/probe21]
274 connect_debug_port u_ila_0/probe21 [get_nets [list RSTC_IBUF]]
275 create_debug_port u_ila_0 probe
276 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
277 set_property port_width 1 [get_debug_ports u_ila_0/probe22]
278 connect_debug_port u_ila_0/probe22 [get_nets [list RSTCARRYIN_IBUF]]
279 create_debug_port u_ila_0 probe
280 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
281 set_property port_width 1 [get_debug_ports u_ila_0/probe23]
282 connect_debug_port u_ila_0/probe23 [get_nets [list RSTD_IBUF]]
283 create_debug_port u_ila_0 probe
284 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
285 set_property port_width 1 [get_debug_ports u_ila_0/probe24]
286 connect_debug_port u_ila_0/probe24 [get_nets [list RSTM_IBUF]]
287 create_debug_port u_ila_0 probe
288 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe25]
289 set_property port_width 1 [get_debug_ports u_ila_0/probe25]
290 connect_debug_port u_ila_0/probe25 [get_nets [list RSTOPMODE_IBUF]]
291 create_debug_port u_ila_0 probe
292 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe26]
293 set_property port_width 1 [get_debug_ports u_ila_0/probe26]
294 connect_debug_port u_ila_0/probe26 [get_nets [list RSTP_IBUF]]
295 set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
296 set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
297 set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
298 connect_debug_port dbg_hub/clk [get_nets CLK_IBUF_BUFG]
299
```

# Elaboration:

## Messages Tab:



## Schematic:



# Synthesis:

## Messages Tab:

The screenshots show the Vivado Messages tab with three different synthesis runs. Each screenshot includes a toolbar at the top with icons for search, filter, and file operations, and a status bar at the bottom.

- Screenshot 1 (Top):** Shows synthesis results for a Spartan6-DSP48A1 device. It includes 41 warnings and 58 infos. Key messages include: "Got license for feature 'Synthesis' and/or device 'xc7a200t'", "synthesizing module 'Spartan6\_DSP48A1'[Spartan6\_DSP48A1.v1]", and "instance 'Pre\_Adder\_Subtractor' of module 'Adder\_Subtractor' requires 6 connections, but only 5 given [Spartan6\_DSP48A1.v38]."
- Screenshot 2 (Middle):** Shows synthesis results for a Spartan6-DSP48A1 device. It includes 41 warnings and 67 infos. Key messages include: "HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [Adder\_Subtractor.v9]", "Unused sequential element 'L\_B0/Q\_reg[0]' was removed [RegOrNot\_MuxInputs.v16]", and "Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [Multiplier.v6]."
- Screenshot 3 (Bottom):** Shows synthesis results for a Spartan6-DSP48A1 device. It includes 41 warnings and 67 infos. Key messages include: "The checkpoint 'D:/sublime\_text/sublime\_text\_build\_4169\_x64/Projects/Project 1/project\_1/runs/synth\_1/Spartan6\_DSP48A1.dcp' has been generated.", "Executing : report\_utilization -file Spartan6\_DSP48A1\_utilization\_synth.rpt -pb Spartan6\_DSP48A1\_utilization\_synth.pb", and "Exiting Vivado at Wed Jul 31 14:39:01 2024.."

## Utilization Report:

Tcl Console | Messages | Log | Reports | Design Runs | Utilization | Debug | Hierarchy

**Hierarchy**

Name	1	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	
<b>N Spartan6_DSP48A1</b>	230	142	1	327	1	0	0
I_B1 (RegOrNot_MuxIn...	1	18	0	0	0	0	0
I_C (RegOrNot_MuxIn...	0	48	0	0	0	0	0
I_CARRYIN (RegOrNot...	1	1	0	0	0	0	0
I_CARRYOUT (RegOr...	0	1	0	0	0	0	0
I_D (RegOrNot_MuxIn...	35	18	0	0	0	0	0
I_MUL (Multiplier)	0	0	1	0	0	0	0

utilization\_1

Tcl Console | Messages | Log | Reports | Design Runs | Utilization | Debug | Hierarchy

**Hierarchy**

Name	1	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	
I_CARRYOUT (RegOr...	0	1	0	0	0	0	0
I_D (RegOrNot_MuxIn...	35	18	0	0	0	0	0
I_MUL (Multiplier)	0	0	1	0	0	0	0
I_OPMODE (RegOrNot...	193	8	0	0	0	0	0
I_P (RegOrNot_MuxIn...	0	48	0	0	0	0	0
Post_Adder_Subtract...	0	0	0	0	0	0	0
Pre_Adder_Subtractor ...	0	0	0	0	0	0	0

utilization\_1

## Timing Report:

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Utilization | Debug | Design Timing Summary

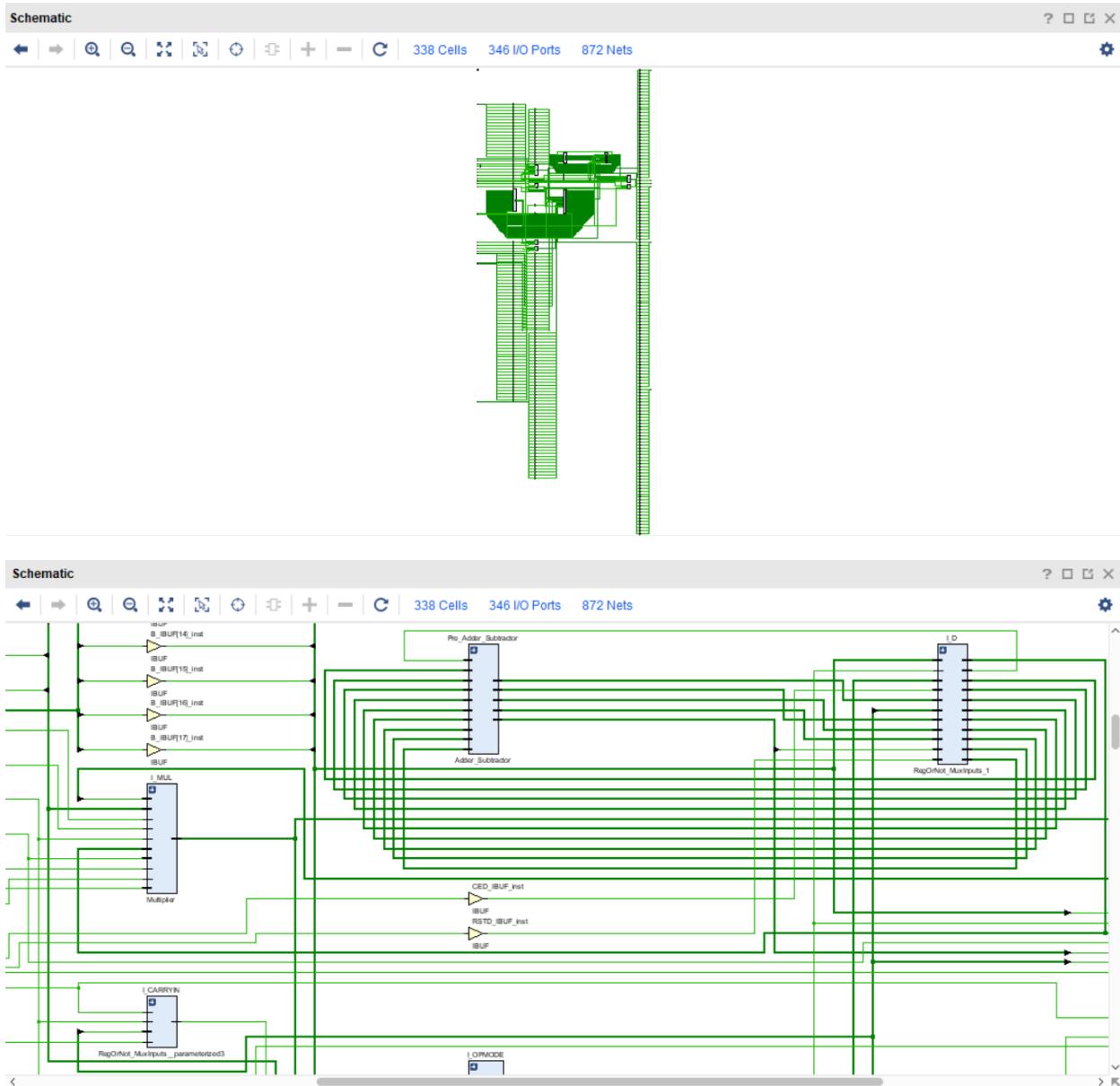
**Design Timing Summary**

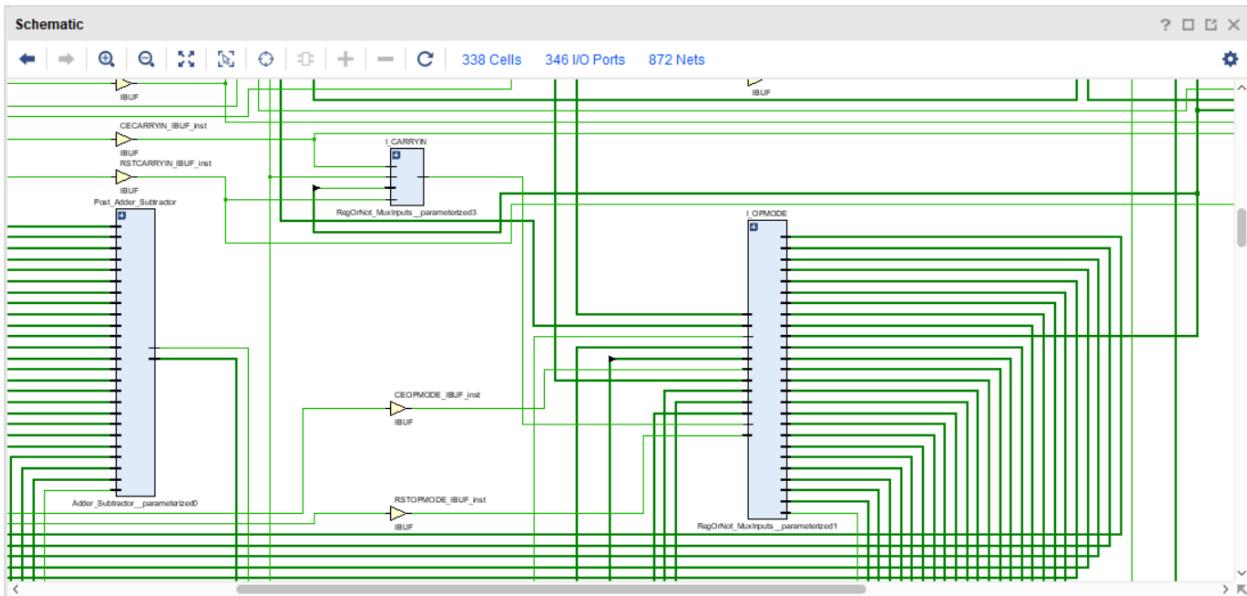
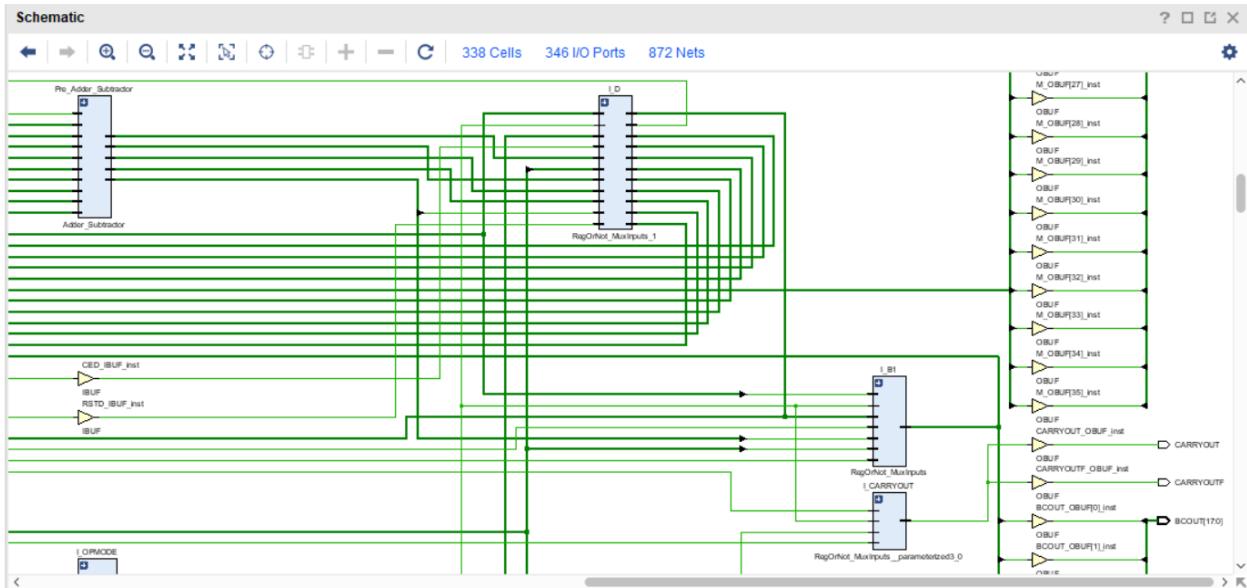
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.819 ns	Worst Hold Slack (WHS):	0.003 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWNS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	87	Total Number of Endpoints:	87	Total Number of Endpoints:	144

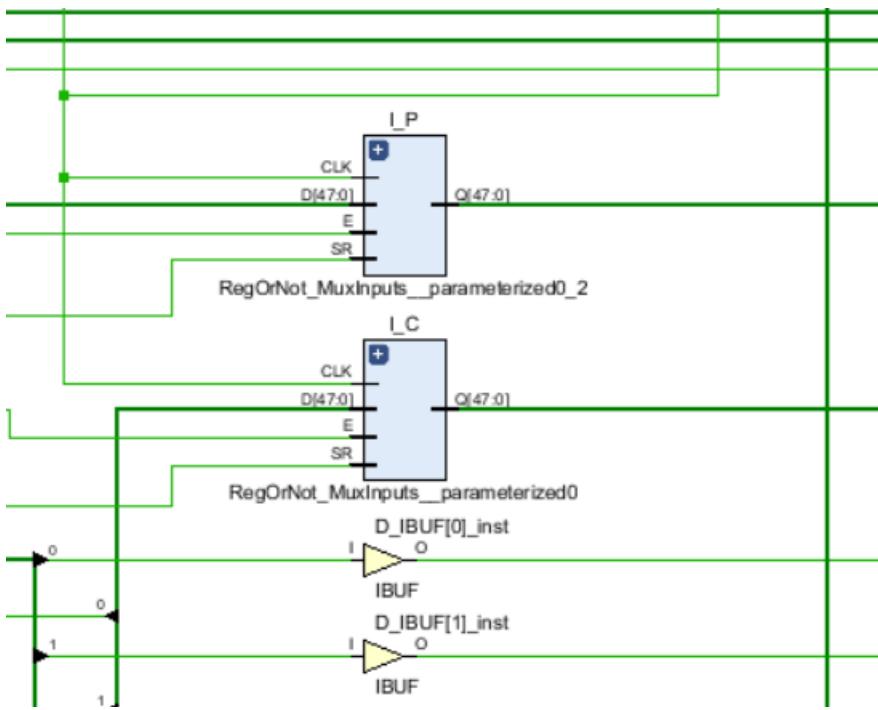
All user specified timing constraints are met.

Timing Summary - timing\_1

## Schematic:







## Implementation:

## Messages Tab:

## Utilization Report:

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization | ? - □ □

**Hierarchy**

Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSPs (740)
↳ I_CARRYOUT (RegOr...	0	1	0	0	1	0	0	0	0	0
↳ I_D (RegOrNot_MuxInp...	35	18	0	0	16	35	0	0	0	0
↳ I_MUL (Multiplier)	0	0	0	0	0	0	0	0	0	1
↳ I_OPMODE (RegOrNot...	193	8	0	0	69	193	0	0	0	0
↳ I_P (RegOrNot_MuxInp...	0	48	0	0	12	0	0	0	0	0
↳ Post_Adder_Subtract...	0	0	0	0	13	0	0	0	0	0
↳ Pre_Adder_Subtractor ...	0	0	0	0	5	0	0	0	0	0
> u_ilia_0 (u_ilia_0)	1998	3338	97	12	1187	1548	450	1241	8	0

utilization\_1

## Timing Report:

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization | ? - □ □

**Design Timing Summary**

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	<b>2.228 ns</b>	Worst Hold Slack (WHS):	<b>0.079 ns</b>	Worst Pulse Width Slack (WPWS):	<b>3.950 ns</b>
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWNS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8058	Total Number of Endpoints:	8042	Total Number of Endpoints:	5118

All user specified timing constraints are met.

Timing Summary - impl\_1 (saved) × Timing Summary - timing\_1 ×

## Device:

