

Project 2

RAM Code:

D:\sublime_text\sublime_text_build_4169_x64\Projects\Project 2\sp_async_ram.v - Sublime Text

File Edit Selection Find View Goto Tools Project Preferences Help

```
1 module sp_async_ram(clk, rst_n, rx_valid, tx_valid, din, dout);
2
3 parameter MEM_DEPTH = 256; parameter ADDR_SIZE = 8;
4
5 input clk, rst_n, rx_valid;
6 input [9:0]din;
7 output reg tx_valid;
8 output reg [7:0]dout;
9
10 reg [7:0] mem [MEM_DEPTH-1:0];
11
12 reg [ADDR_SIZE-1:0]addr_wr;
13 reg [ADDR_SIZE-1:0]addr_rd;
14
15 always @(posedge clk) begin
16
17     if (~rst_n) begin
18         addr_wr <= 0; addr_rd <= 0;
19         tx_valid <= 1'b0;
20         dout <= 0;
21     end
22     else begin
23         if(rx_valid == 1) begin
24             if(din[9:8] == 2'b00) begin
25                 tx_valid <= 0;
26                 addr_wr <= din[7:0];
27             end
28             else if(din[9:8] == 2'b01) begin
29                 tx_valid <= 0;
30                 mem[addr_wr] <= din[7:0];
31             end
32             else if(din[9:8] == 2'b10) begin
33                 tx_valid <= 0;
34                 addr_rd <= din[7:0];
35             end
36             else begin
37                 tx_valid <= 1'b1;
38                 dout <= mem[addr_rd];
39             end
40         end
41     end
42 end
43
44 end
45
46 endmodule
```

SPI Slave Code:

D:\sublime_text\sublime_text_build_4169_x64\Projects\Project 2\spi_slave.v - Sublime Text (UNREGISTERED)

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```
1 module spi_slave(clk, rst_n, SS_n, MOSI, MISO, rx_valid, rx_data, tx_valid, tx_data);
2
3 parameter IDLE = 3'b000; parameter CHK_CMD = 3'b001; parameter WRITE = 3'b010; parameter READ_ADD = 3'b011; parameter READ_DATA = 3'b100;
4
5 input clk, rst_n, SS_n, MOSI, tx_valid;
6 input [7:0]tx_data;
7 output reg MISO, rx_valid;
8 output reg [9:0]rx_data;
9
10 (*fsm_encoding = "gray")
11 //(*fsm_encoding = "one_hot")
12 //(*fsm_encoding = "sequential")
13 reg [2:0]cs, ns;
14 reg read_add; //if High, read address has already been received.
15 reg [3:0]count;
16 //Next State Logic
17
18 always @(*) begin
19   case(cs)
20     IDLE: begin
21       if(SS_n) begin
22         ns = IDLE;
23       end
24       else begin
25         ns = CHK_CMD;
26       end
27     end
28     CHK_CMD: begin
29       if(SS_n) begin
30         ns = IDLE;
31       end
32       else begin
33         if(MOSI) begin
34           if(read_add) begin
35             ns = READ_DATA;
36           end
37           else begin
38             ns = READ_ADD;
39           end
40         end
41         else begin
42           ns = WRITE;
43         end
44       end
45     end
46   end
47 end
```

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◀ ▶ sp_async_ram.v × spi_slave.v

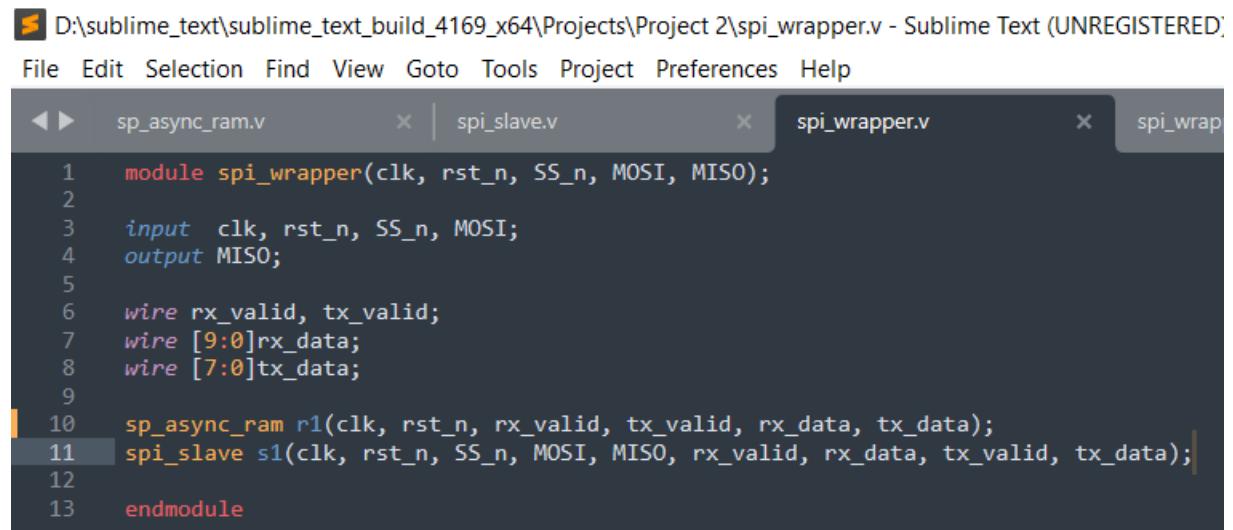
```
46     WRITE: begin
47         if(SS_n) begin
48             ns = IDLE;
49         end
50         else begin
51             ns = WRITE;
52         end
53     end
54     READ_ADD: begin
55         if(SS_n) begin
56             ns = IDLE;
57         end
58         else begin
59             ns = READ_ADD;
60         end
61     end
62     READ_DATA: begin
63         if(SS_n) begin
64             ns = IDLE;
65         end
66         else begin
67             ns = READ_DATA;
68         end
69     end
70     default: ns = IDLE;
71
72     endcase
73
74 end
75
76 //State Memory
77
78 always @(posedge clk) begin
79     if(~rst_n) begin
80         cs <= IDLE;
81     end
82     else begin
83         cs <= ns;
84     end
85 end
86
```

D:\sublime_text\sublime_text_build_4169_x64\Projects\Project 2\spi_slave.v - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

```
sp_async_ram.v      spi_slave.v      spi_wrapper.v      spi_wrapper_tb.v
86
87 //Output Logic
88
89 always @(posedge clk) begin
90     if(~rst_n) begin
91         rx_valid <= 0; rx_data <= 0;
92         MISO <= 0; read_add <= 0;
93     end
94     else begin
95         if((cs == IDLE) || (cs == CHK_CMD)) begin
96             MISO <= 0; rx_valid <= 0; count <= 0;
97         end
98         else if(cs == WRITE) begin
99             if(count < 10) begin
100                 rx_data <= {rx_data[8:0], MOSI}; rx_valid <= 0; count <= count + 1;
101             end
102             if(count == 10) begin
103                 rx_valid <= 1;
104             end
105         end
106         else if(cs == READ_ADD) begin
107             if(count < 10) begin
108                 rx_data <= {rx_data[8:0], MOSI}; rx_valid <= 0; count <= count + 1;
109             end
110             if(count == 10) begin
111                 rx_valid <= 1; read_add <= 1;
112             end
113         end
114         else begin
115             if(tx_valid == 0) begin
116                 if(count < 10) begin
117                     rx_data <= {rx_data[8:0], MOSI}; rx_valid <= 0; count <= count + 1;
118                 end
119                 if(count == 10) begin
120                     rx_valid <= 1; read_add <= 0;
121                 end
122             end
123             else begin
124                 if(count >= 3) begin
125                     MISO <= tx_data[count - 3];
126                     count <= count - 1;
127                 end
128             end
129         end
130     end
131
132 end
133
134 endmodule
```

SPI Wrapper Code:

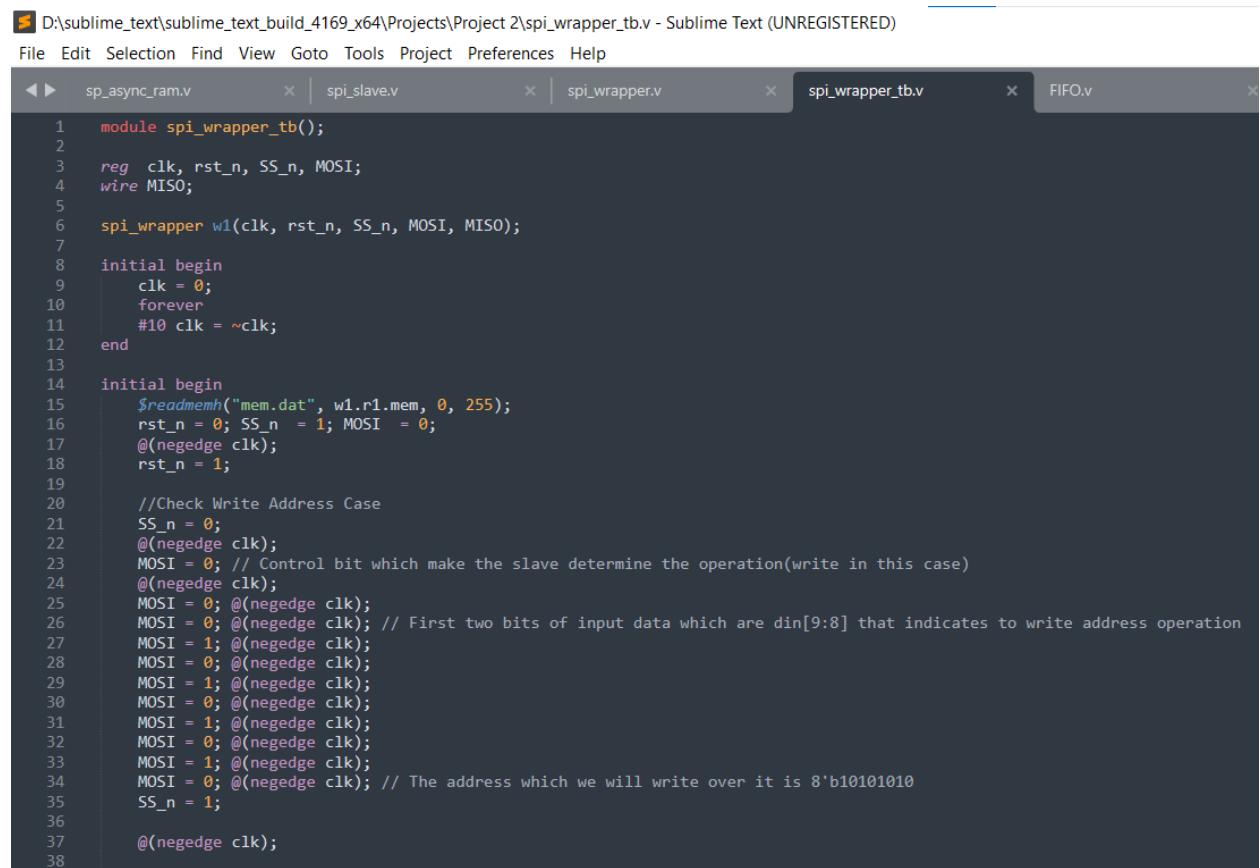


D:\sublime_text\sublime_text_build_4169_x64\Projects\Project 2\spi_wrapper.v - Sublime Text (UNREGISTERED)

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```
sp_async_ram.v | spi_slave.v | spi_wrapper.v | spi_wrap
1 module spi_wrapper(clk, rst_n, SS_n, MOSI, MISO);
2
3   input  clk, rst_n, SS_n, MOSI;
4   output MISO;
5
6   wire rx_valid, tx_valid;
7   wire [9:0]rx_data;
8   wire [7:0]tx_data;
9
10  sp_async_ram r1(clk, rst_n, rx_valid, tx_valid, rx_data, tx_data);
11  spi_slave s1(clk, rst_n, SS_n, MOSI, MISO, rx_valid, rx_data, tx_valid, tx_data);
12
13 endmodule
```

Testbench Code:



D:\sublime_text\sublime_text_build_4169_x64\Projects\Project 2\spi_wrapper_tb.v - Sublime Text (UNREGISTERED)

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```
sp_async_ram.v | spi_slave.v | spi_wrapper.v | spi_wrapper_tb.v | FIFO.v
1 module spi_wrapper_tb();
2
3   reg  clk, rst_n, SS_n, MOSI;
4   wire MISO;
5
6   spi_wrapper w1(clk, rst_n, SS_n, MOSI, MISO);
7
8   initial begin
9     clk = 0;
10    forever
11      #10 clk = ~clk;
12  end
13
14  initial begin
15    $readmemh("mem.dat", w1.r1.mem, 0, 255);
16    rst_n = 0; SS_n = 1; MOSI = 0;
17    @(negedge clk);
18    rst_n = 1;
19
20    //Check Write Address Case
21    SS_n = 0;
22    @(negedge clk);
23    MOSI = 0; // Control bit which make the slave determine the operation(write in this case)
24    @(negedge clk);
25    MOSI = 0; @(negedge clk);
26    MOSI = 0; @(negedge clk); // First two bits of input data which are din[9:8] that indicates to write address operation
27    MOSI = 1; @(negedge clk);
28    MOSI = 0; @(negedge clk);
29    MOSI = 1; @(negedge clk);
30    MOSI = 0; @(negedge clk);
31    MOSI = 1; @(negedge clk);
32    MOSI = 0; @(negedge clk);
33    MOSI = 1; @(negedge clk);
34    MOSI = 0; @(negedge clk); // The address which we will write over it is 8'b10101010
35    SS_n = 1;
36
37    @(negedge clk);
38
```

```
38 //Check Write Data Case
39 SS_n = 0;
40 @(negedge clk);
41 MOSI = 0; // Control bit which make the slave determine the operation(write in this case)
42 @(negedge clk);
43 MOSI = 0; @(negedge clk);
44 MOSI = 1; @(negedge clk); // First two bits of input data which are din[9:8] that indicates to write data operation
45 MOSI = 1; @(negedge clk);
46 MOSI = 0; @(negedge clk);
47 MOSI = 0; @(negedge clk);
48 MOSI = 1; @(negedge clk);
49 MOSI = 1; @(negedge clk);
50 MOSI = 0; @(negedge clk);
51 MOSI = 0; @(negedge clk);
52 MOSI = 1; @(negedge clk); // The data which we will write in the previous write address is 8'b10011001
53 SS_n = 1;
54
55 @(negedge clk);

56 //Check Read Address Case
57 SS_n = 0;
58 @(negedge clk);
59 MOSI = 1; // Control bit which make the slave determine the operation(read in this case)
60 @(negedge clk);
61 MOSI = 1; @(negedge clk);
62 MOSI = 1; @(negedge clk);
63 MOSI = 0; @(negedge clk);
64 MOSI = 1; @(negedge clk); // First two bits of input data which are din[9:8] that indicates to read address operation
65 MOSI = 1; @(negedge clk);
66 MOSI = 1; @(negedge clk);
67 MOSI = 0; @(negedge clk);
68 MOSI = 1; @(negedge clk);
69 MOSI = 1; @(negedge clk);
70 MOSI = 0; @(negedge clk);
71 MOSI = 1; @(negedge clk);
72 MOSI = 1; @(negedge clk); // The address which we will read from is 8'b11011011
73 SS_n = 1;
74
75 @(negedge clk);
```

D:\sublime_text\sublime_text_build_4169_x64\Projects\Project 2\spi_wrapper_tb.v - Sublime Text (UNREGISTERED)

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```
76 //Check Read Data Case
77 SS_n = 0;
78 @(negedge clk);
79 MOSI = 1; // Control bit which make the slave determine the operation(read in this case)
80 @(negedge clk);
81 MOSI = 1; @(negedge clk);
82 MOSI = 1; @(negedge clk); // First two bits of input data which are din[9:8] that indicates to read data operation
83 MOSI = 1; @(negedge clk);
84 MOSI = 1; @(negedge clk);
85 MOSI = 0; @(negedge clk);
86 MOSI = 1; @(negedge clk);
87 MOSI = 1; @(negedge clk);
88 MOSI = 1; @(negedge clk);
89 MOSI = 1; @(negedge clk);
90 MOSI = 1; @(negedge clk);
91 MOSI = 1; @(negedge clk); // Input bits in this case which are 8'b10111111 are ignored
92 repeat(8) begin
93     @(negedge clk);
94 end
95 SS_n = 1;
96
97 @(negedge clk);

98 //Check Read Address Case
99 SS_n = 0;
100 @(negedge clk);
101 MOSI = 1; // Control bit which make the slave determine the operation(read in this case)
102 @(negedge clk);
103 MOSI = 1; @(negedge clk);
104 MOSI = 0; @(negedge clk); // First two bits of input data which are din[9:8] that indicates to read address operation
105 MOSI = 1; @(negedge clk);
106 MOSI = 0; @(negedge clk);
107 MOSI = 1; @(negedge clk);
108 MOSI = 0; @(negedge clk);
109 MOSI = 1; @(negedge clk);
110 MOSI = 0; @(negedge clk);
111 MOSI = 1; @(negedge clk);
112 MOSI = 0; @(negedge clk); // The address which we will read from is 8'b10101010
113 SS_n = 1;
114
115 @(negedge clk);

116
```

D:\sublime_text\sublime_text_build_4169_x64\Projects\Project 2\spi_wrapper_tb.v - Sublime Text (UNREGISTERED)

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```
11/
118 //Check Read Data Case
119 SS_n = 0;
120 @(negedge clk);
121 MOSI = 1; // Control bit which make the slave determine the operation(read in this case)
122 @(negedge clk);
123 MOSI = 1; @(negedge clk);
124 MOSI = 1; @(negedge clk); // First two bits of input data which are din[9:8] that indicates to read data operation
125 MOSI = 1; @(negedge clk);
126 MOSI = 0; @(negedge clk);
127 MOSI = 1; @(negedge clk);
128 MOSI = 1; @(negedge clk);
129 MOSI = 1; @(negedge clk);
130 MOSI = 0; @(negedge clk);
131 MOSI = 1; @(negedge clk); MOSI = 1; @(negedge clk); // Input bits in this case which are 8'b10111011 are ignored
132 repeat(8) begin
133     @(negedge clk);
134 end
135 SS_n = 1;
136
137 @(negedge clk);
138
139 $stop;
140
141
142 endmodule
```

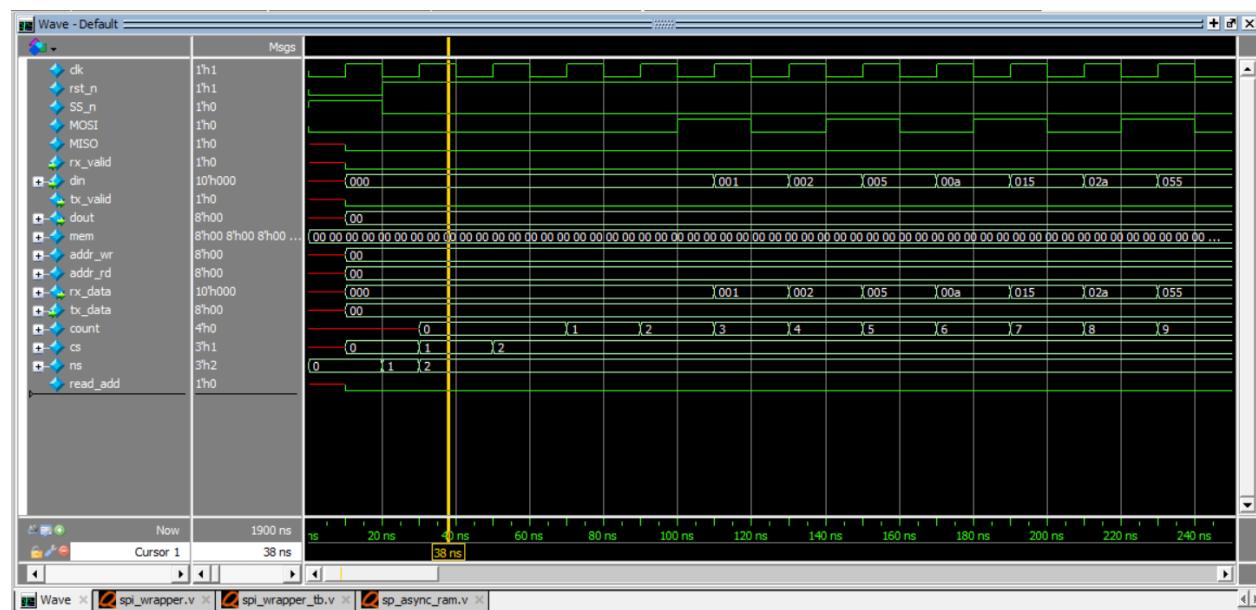
DO File:

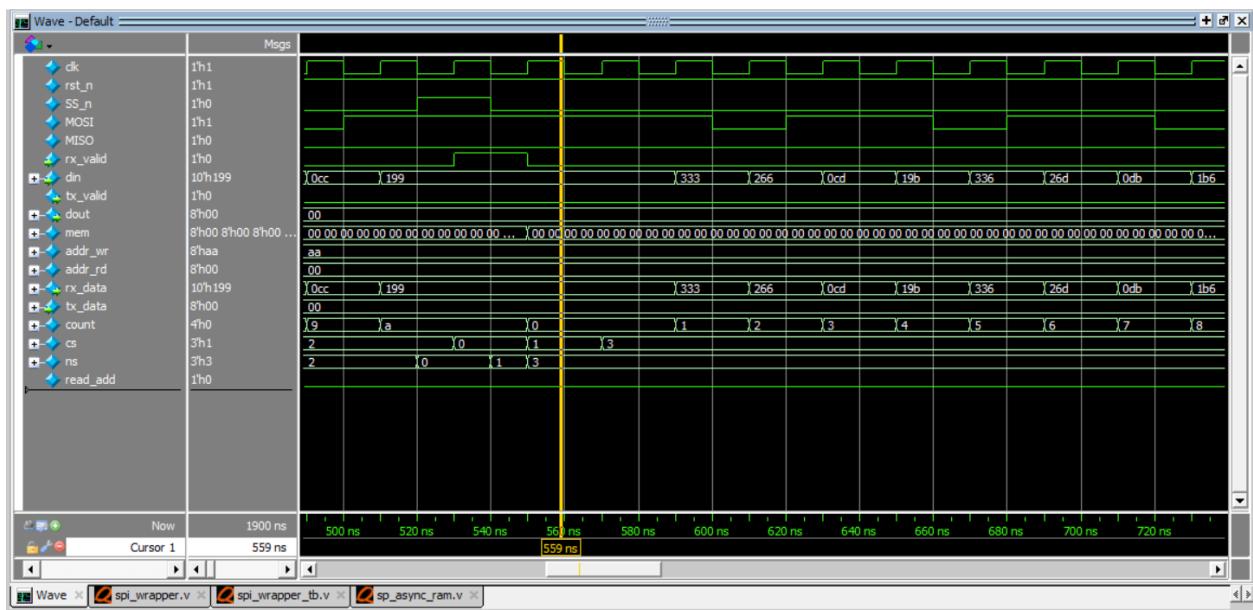
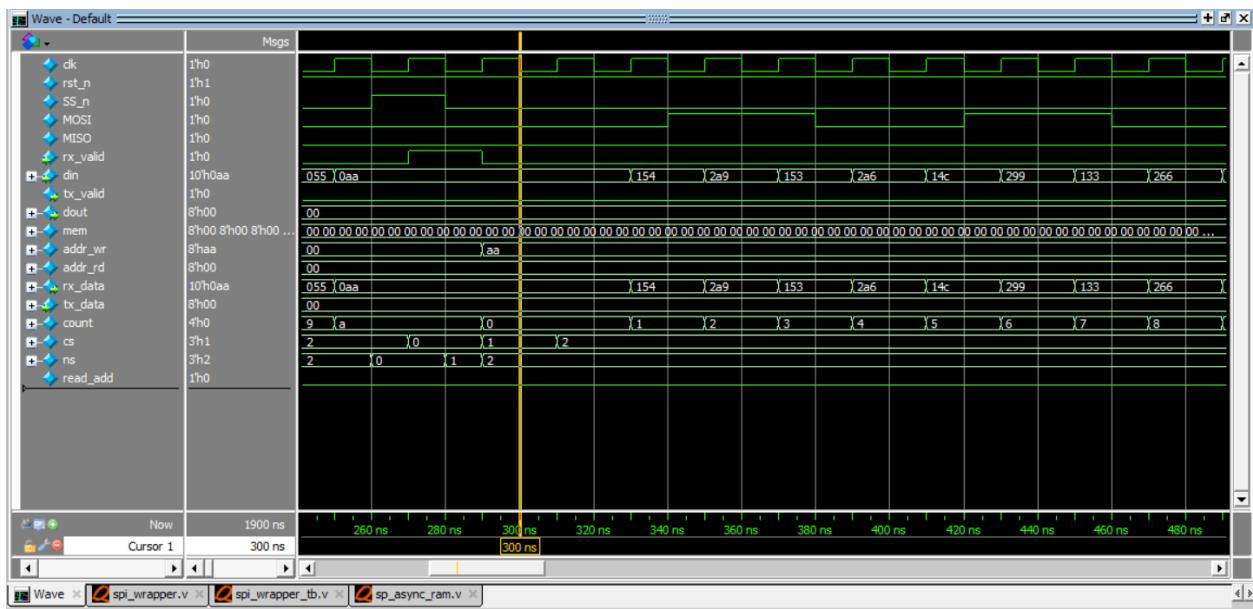
```
run - Notepad
File Edit Format View Help
vlib work
vlog sp_async_ram.v spi_slave.v spi_wrapper.v spi_wrapper_tb.v
vsim -voptargs=+acc work.spi_wrapper_tb
add wave *

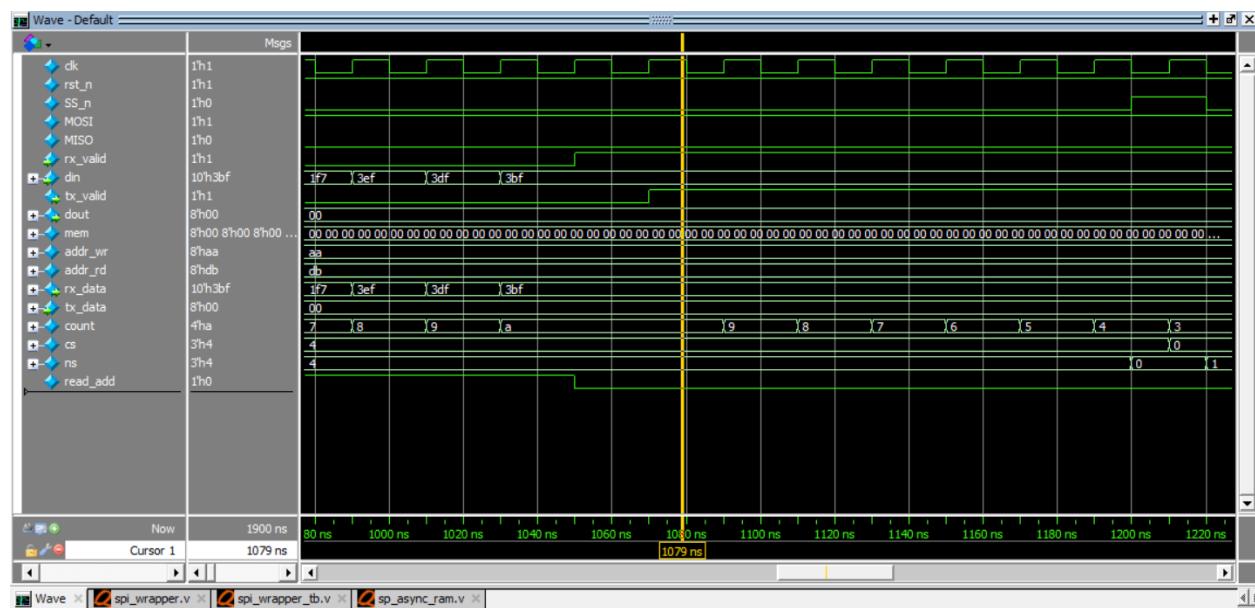
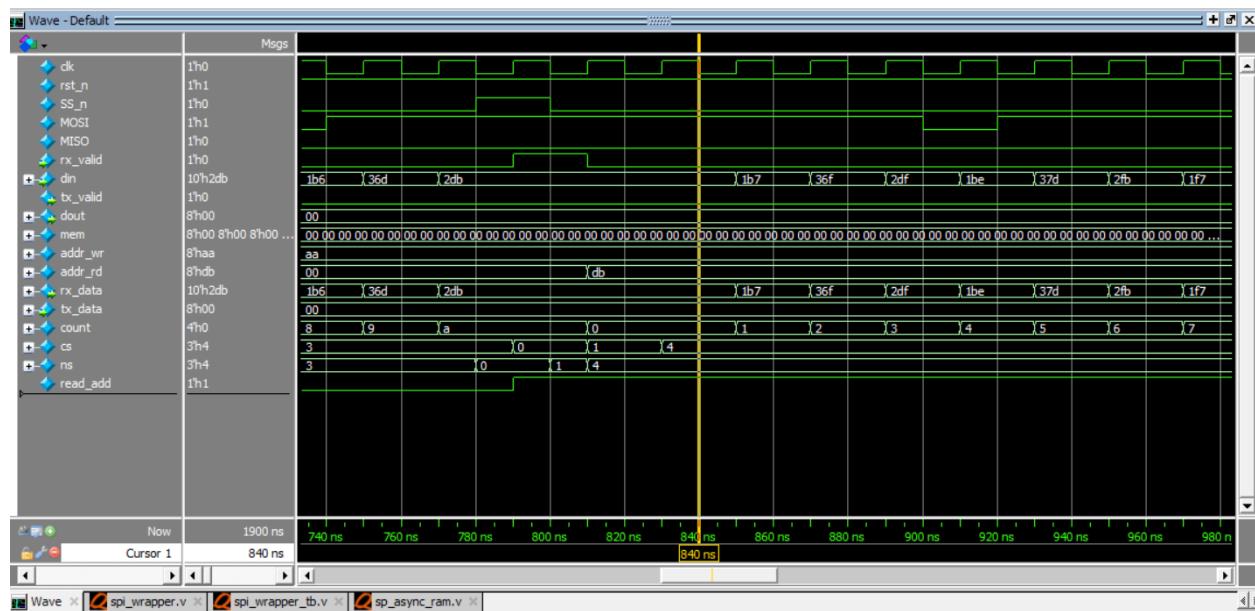
add wave -position insertpoint sim:/spi_wrapper_tb/w1/r1/rx_valid
add wave -position insertpoint sim:/spi_wrapper_tb/w1/r1/din
add wave -position insertpoint sim:/spi_wrapper_tb/w1/r1/tx_valid
add wave -position insertpoint sim:/spi_wrapper_tb/w1/r1/dout
add wave -position insertpoint sim:/spi_wrapper_tb/w1/r1/mem
add wave -position insertpoint sim:/spi_wrapper_tb/w1/r1/addr_wr
add wave -position insertpoint sim:/spi_wrapper_tb/w1/r1/addr_rd
add wave -position insertpoint sim:/spi_wrapper_tb/w1/s1/rx_data
add wave -position insertpoint sim:/spi_wrapper_tb/w1/s1/tx_data
add wave -position insertpoint sim:/spi_wrapper_tb/w1/s1/count
add wave -position insertpoint sim:/spi_wrapper_tb/w1/s1/cs
add wave -position insertpoint sim:/spi_wrapper_tb/w1/s1/ns
add wave -position insertpoint sim:/spi_wrapper_tb/w1/s1/read_add

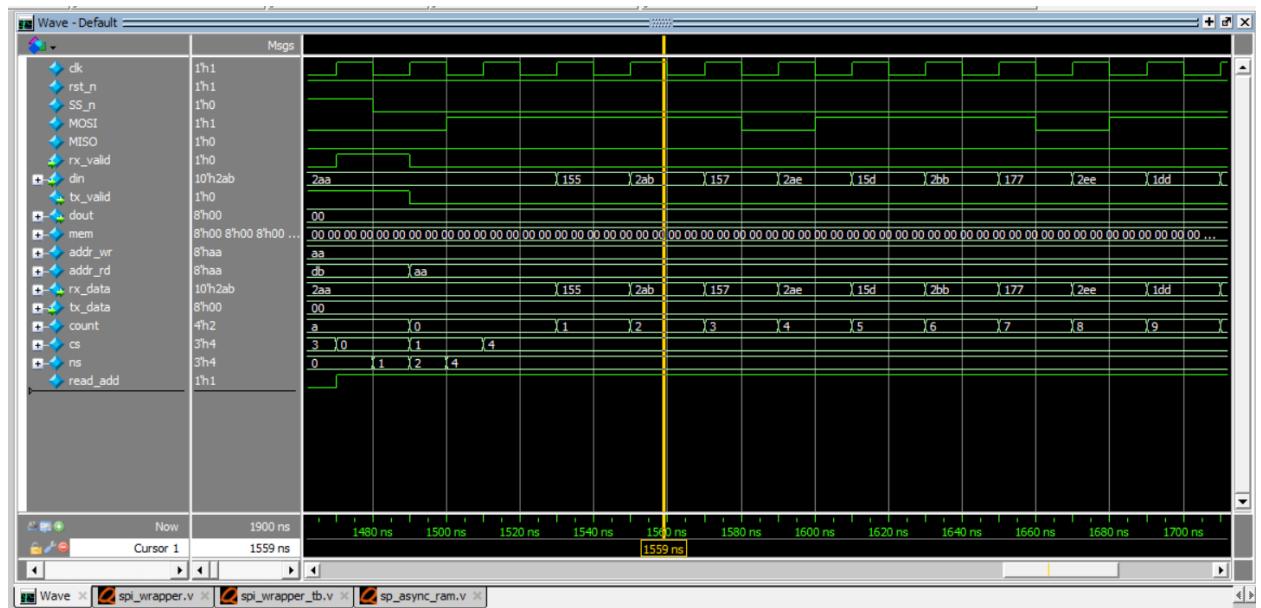
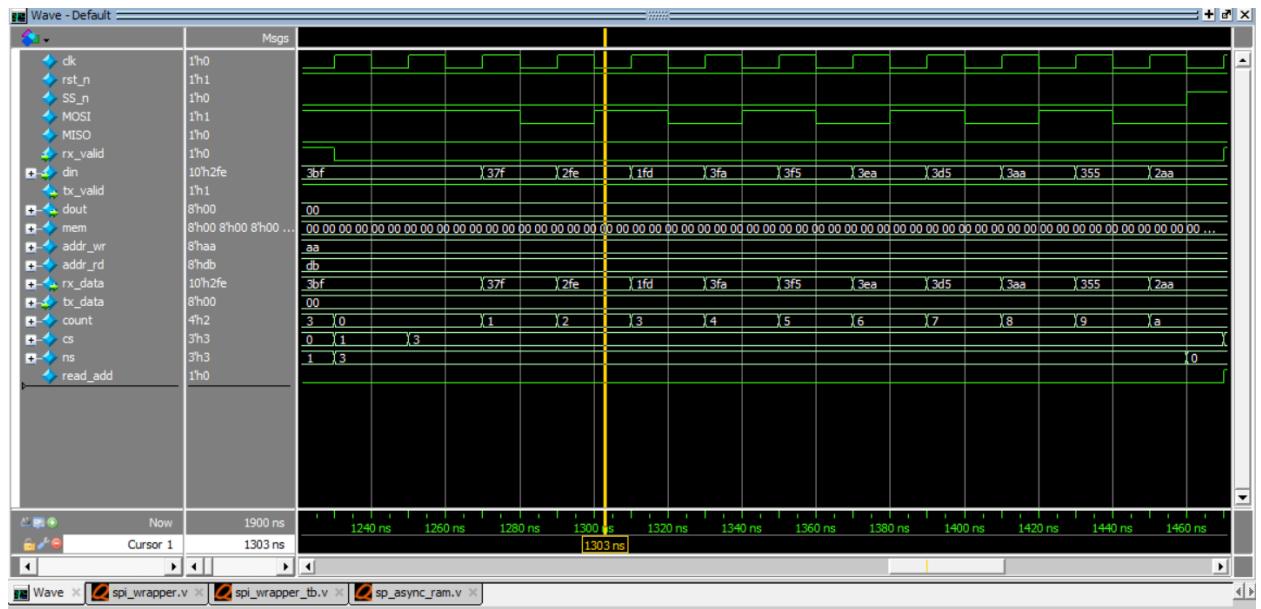
run -all
#quit -sim
```

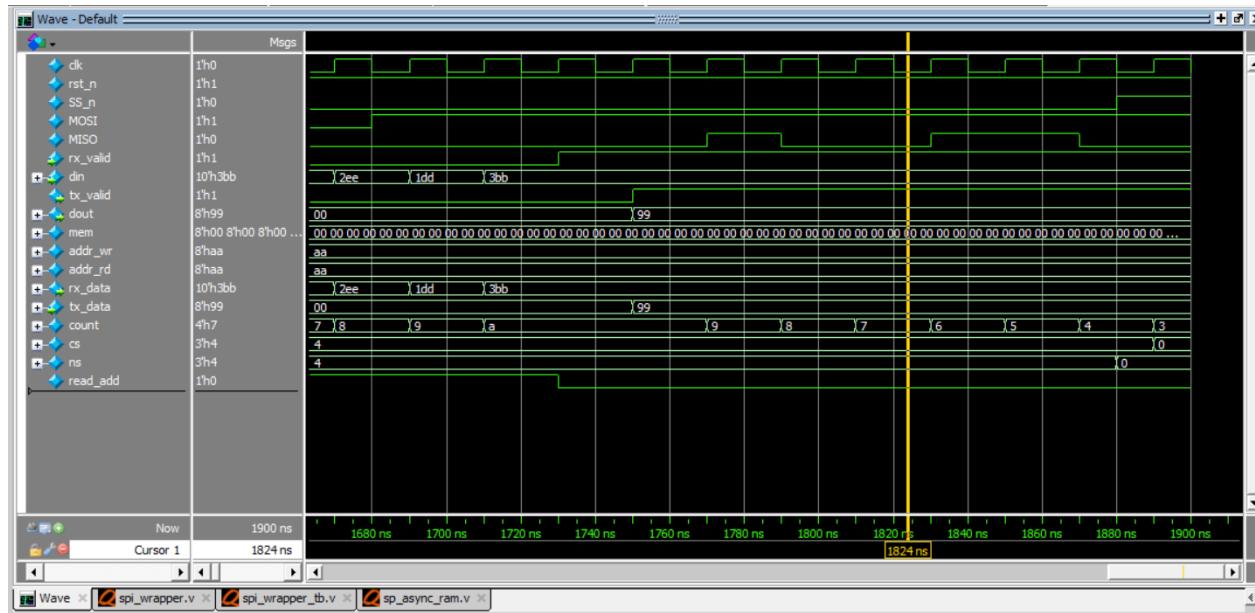
Waveform:







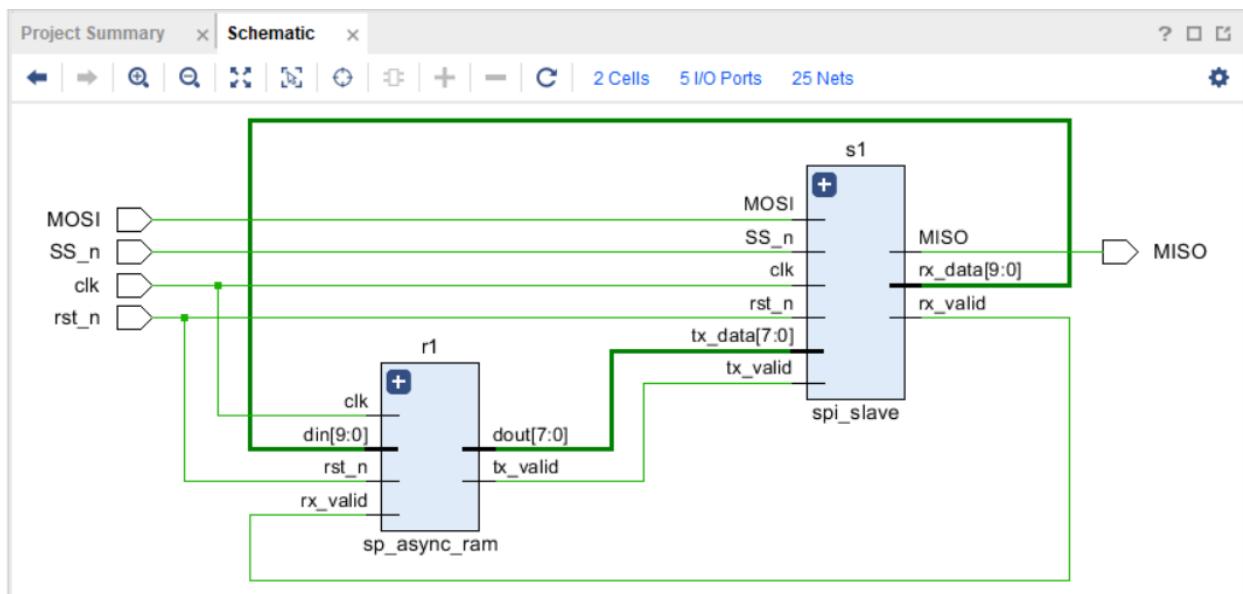




Gray Encoding Snippets:

Elaboration:

Schematic:



Messages Tab:

Tcl Console **Messages** Log Reports Design Runs

Q | | | | | | | Info (14) Status (11) Show All

▼ Vivado Commands (3 infos)
 ▼ General Messages (3 infos)
 [IP_Flow 19-234] Refreshing IP repositories
 [IP_Flow 19-1704] No user IP repositories specified
 [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
▼ Elaborated Design (11 infos)
 ▼ General Messages (11 infos)
 > [Synth 8-6157] synthesizing module 'spi_wrapper' [[spi_wrapper.v:1](#)] (2 more like this)
 [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [[spi_slave.v:13](#)]

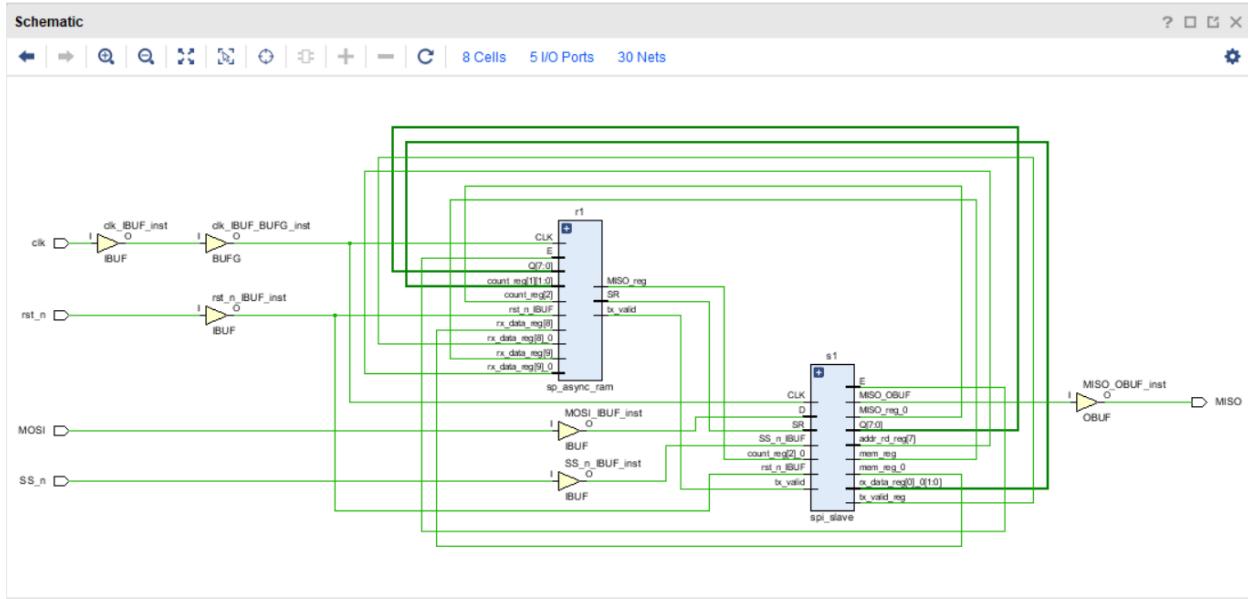
Tcl Console **Messages** Log Reports Design Runs

Q | | | | | | | Info (14) Status (11) Show All

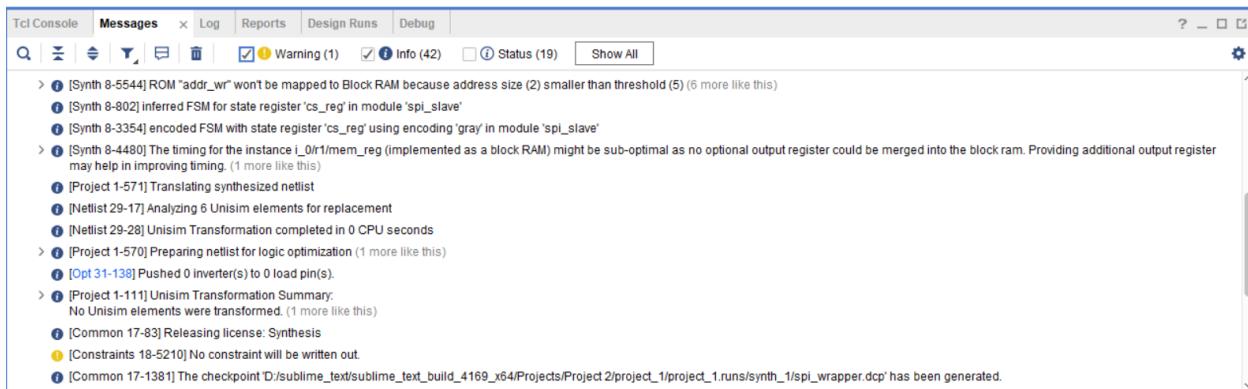
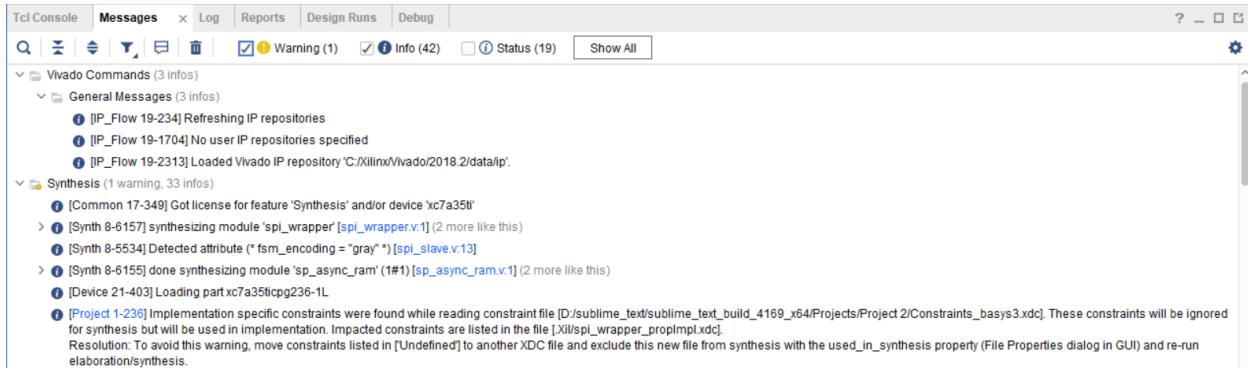
▼ General Messages (11 infos)
 > [Synth 8-6157] synthesizing module 'spi_wrapper' [[spi_wrapper.v:1](#)] (2 more like this)
 [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [[spi_slave.v:13](#)]
 > [Synth 8-6155] done synthesizing module 'sp_async_ram' (1#1) [[sp_async_ram.v:1](#)] (2 more like this)
 [Device 21-403] Loading part xc7a35ticpg236-1L
 [Project 1-570] Preparing netlist for logic optimization
 [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 [Project 1-111] Unisim Transformation Summary:
 No Unisim elements were transformed.

Synthesis:

Schematic:



Messages Tab:



Tcl Console Messages Log Reports Design Runs Debug

Q | X | D | T | M | B | Show All

Warning (1) Info (42) Status (19)

No Unisim elements were transformed. (1 more like this)

- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_1.runs/synth_1/spi_wrapper.dcp' has been generated.
- [runrtl-4] Executing : report_utilization -file spi_wrapper_utilization_synth.rpt -pb spi_wrapper_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Mon Aug 5 21:11:54 2024...

Synthesized Design (6 infos)

General Messages (6 infos)

- [Netlist 29-17] Analyzing 6 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Utilization Report:

Tcl Console Messages Log Reports Design Runs Utilization Debug

Q | X | D | T | % | Hierarchy

Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_wrapper	23	37	1	0.5	5	1	
r1 (sp_async_ram)	3	17	1	0.5	0	0	
s1 (spi_slave)	20	20	0	0	0	0	

Hierarchy

- Summary
- Slice Logic
 - Slice LUTs (<1%)
 - LUT as Logic (<1%)
 - Slice Registers (<1%)
 - Register as Flip Flop (F7 Muxes (<1%))
- Memory
 - Block RAM Tile (1%)
 - RAMB18 (1%)
 - RAMB18E1 only
- DSP

utilization_1

Timing Report:

Tcl Console Messages Log Reports Design Runs Timing Utilization Debug

Q | X | D | C | B | S | Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.261 ns	Worst Hold Slack (WHS): 0.146 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 98	Total Number of Endpoints: 98	Total Number of Endpoints: 40

All user specified timing constraints are met.

Clock Summary (1)

Check Timing (4)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

Unconstrained Paths

Synthesis Report:

Schematic × synth_1_synth_synthesis_report_0 - synth_1 ×

D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_1/runs/synth_1/spi_wrapper.vds

Q | F | ← | → | X | // | E | ? | Read-only | ⚙ |

```

29 Parameter CHK_CMD bound to: 3'b001
30 Parameter WRITE bound to: 3'b010
31 Parameter READ_ADD bound to: 3'b011
32 Parameter READ_DATA bound to: 3'b100
33 INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [D:/sublime_text/sublime_text_build_4169_x64/Projec
34 INFO: [Synth 8-6155] done synthesizing module 'spi_slave' (2#1) [D:/sublime_text/sublime_text_build_4169_x64/Projects/P
35 INFO: [Synth 8-6155] done synthesizing module 'spi_wrapper' (3#1) [D:/sublime_text/sublime_text_build_4169_x64/Projects
36 -----
37 Finished RTL Elaboration : Time (s): cpu = 00:00:07 ; elapsed = 00:00:07 . Memory (MB): peak = 410.055 ; gain = 152.484

```

Schematic × synth_1_synth_synthesis_report_0 - synth_1 ×

D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_1/runs/synth_1/spi_wrapper.vds

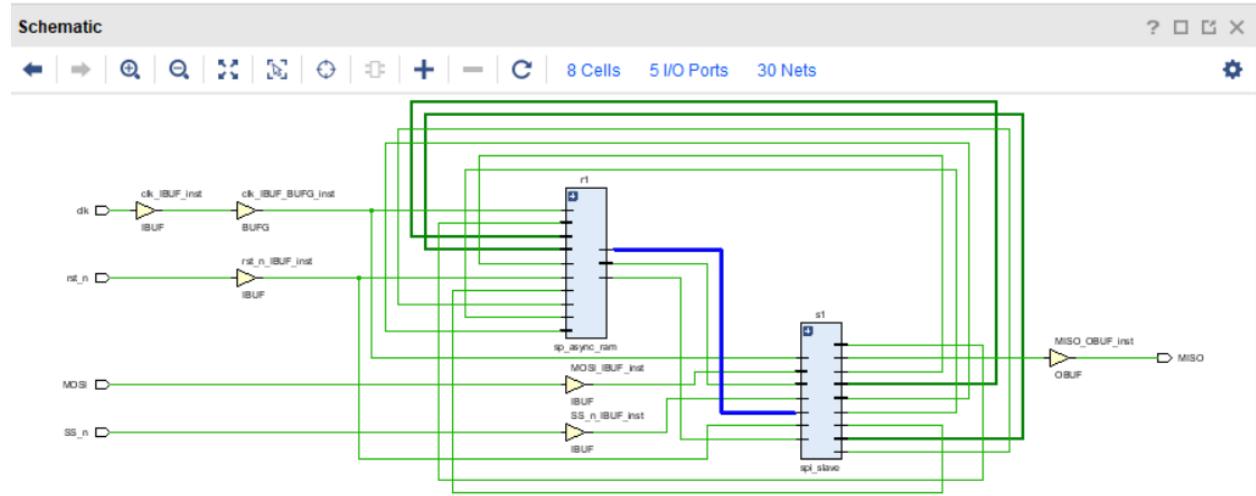
Q | F | ← | → | X | // | E | ? | Read-only | ⚙ |

```

93 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
94 -----
95      State |          New Encoding |          Previous Encoding
96 -----
97      IDLE |          000 |          000
98      CHK_CMD |        001 |        001
99      READ_DATA |       011 |       100
100     READ_ADD |       010 |       011
101     WRITE |        111 |        010
102 -----
103 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'spi_slave'
104 -----
105 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:58 ; elapsed = 00:01:01 . Memory (MB): peak = 764.059 ; gain

```

Critical Path:



Implementation:

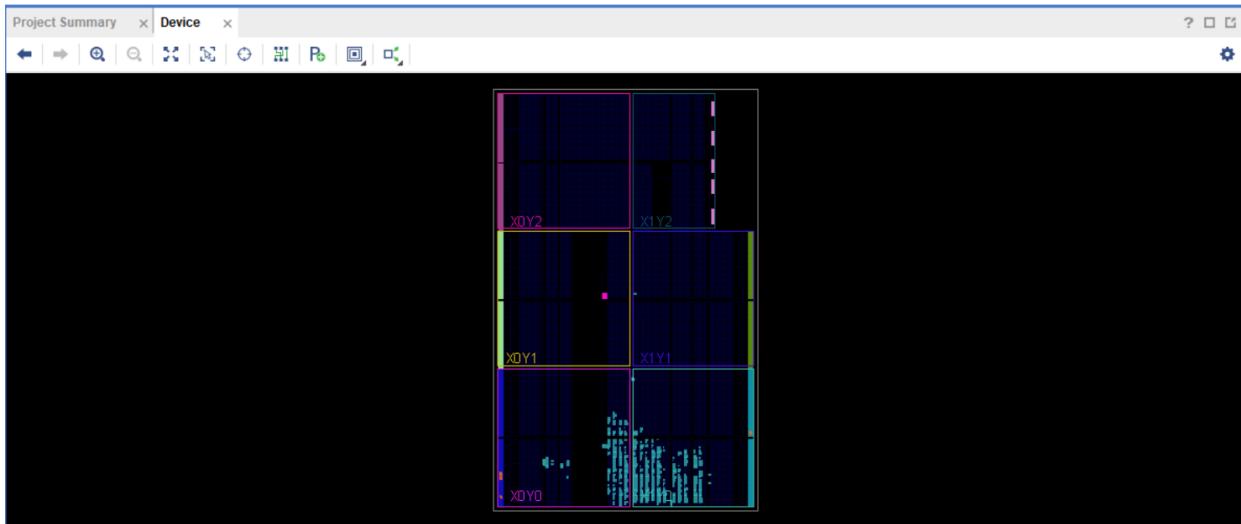
Utilization Report:

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCAN2 (4)
N spi_wrapper	1262	1953	11	603	1154	108	751	1	5	2	1
> dbg_hub (dbg_hub)	475	727	0	237	451	24	313	0	0	1	1
> r1 (sp_async_ram)	3	17	1	5	3	0	0	0.5	0	0	0
> s1 (spi_slave)	20	20	0	8	20	0	9	0	0	0	0
> u_ila_0 (u_ila_0)	764	1189	10	359	680	84	425	0.5	0	0	0

Timing Report:

Design Timing Summary			
General Information	Setup	Hold	Pulse Width
	Worst Negative Slack (WNS): 3.022 ns	Worst Hold Slack (WHS): -0.272 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Clock Summary (2)	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): -0.388 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
> Check Timing (4)	Number of Failing Endpoints: 0	Number of Failing Endpoints: 2	Number of Failing Endpoints: 0
> Intra-Clock Paths	Total Number of Endpoints: 3883	Total Number of Endpoints: 3867	Total Number of Endpoints: 2140
> Inter-Clock Paths	Timing constraints are not met.		
> Other Path Groups			
> User Ignored Paths			
> Unconstrained Paths			

FPGA Device:



Messages Tab:

Tcl Console **Messages** x Log Reports Design Runs

Critical warning (2) Warning (7)

- Implementation (1 critical warning, 3 warnings, 108 infos)
 - Design Initialization (11 infos)
 - [Netlist 29-17] Analyzing 6 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a35ticpg236-1L
 - [Project 1-570] Preparing netlist for logic optimization
 - [Timing 38-478] Restoring timing data from binary archive.
 - [Timing 38-479] Binary timing data restore complete.
 - [Project 1-856] Restoring constraints from binary archive.
 - [Project 1-853] Binary constraint restore complete.
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
 - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
 - Opt Design (35 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
 - [Project 1-461] DRC finished with 0 Errors

Tcl Console **Messages** x Log Reports Design Runs

Critical warning (2) Warning (7) Info (252) Status (511) Show All

- [Project 1-462] Please refer to the DRC report (report_drc) for more information.
- [IP_Flow 19-234] Refreshing IP repositories
- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- > [Chipscope 16-329] Generating Script for core instance : dbg_hub (1 more like this)
- > [IP_Flow 19-3806] Processing IP xilinx.com:ip:xsdbm:3.0 for cell dbg_hub_CV. (1 more like this)
 - [Opt 31-49] Retargeted 0 cell(s).
- > [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)
- > [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
 - [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
- > [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
- > [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
- > [Pwropt 34-9] Applying IDT optimizations ...
- > [Pwropt 34-10] Applying ODC optimizations ...
- > [Physopt 32-619] Estimated Timing Summary | WNS=4.856 | TNS=0.000 |
- > [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 2 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.

Tcl Console Messages Log Reports Design Runs

Q | X | ↻ | ⌂ | T | M | B | Critical warning (2) Warning (7) Info (252) Status (511) Show All

- ① [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports
- ① [Common 17-83] Releasing license: Implementation
- ① [Timing 38-480] Writing timing data to binary archive.
- ① [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_1/runs/impl_1/spi_wrapper_opt.dcp' has been generated.
- ① [runrtl-4] Executing : report_drc -file spi_wrapper_drc_opted.rpt -pb spi_wrapper_drc_opted.pb -px spi_wrapper_drc_opted.ppx
- ① [IP_Flow 19-1839] IP Catalog is up to date.
- > ① [DRC 23-27] Running DRC with 2 threads (1 more like this)
- ① [Corertl 2-168] The results of DRC are in file [spi_wrapper_drc_opted.rpt](#).
- Place Design (24 infos)
 - ① [Chipscope 16-240] Debug cores have already been implemented
 - ① [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
 - > ① [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - > ① [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
 - > ① [Vivado_Tcl 4-199] Please refer to the DRC report ([report_drc](#)) for more information. (1 more like this)
 - ① [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
 - ① [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Tcl Console Messages Log Reports Design Runs

Q | X | ↻ | ⌂ | T | M | B | Critical warning (2) Warning (7) Info (252) Status (511) Show All

- > ① [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
- ① [Physopt 32-65] No nets found for high-fanout optimization.
- ① [Physopt 32-232] Optimized 0 net. Created 0 new instance.
- ① [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
- ① [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
- ① [Place 30-746] Post Placement Timing Summary WNS=4.081. For the most accurate timing information please run [report_timing](#).
- ① [Common 17-83] Releasing license: Implementation
- ① [Timing 38-480] Writing timing data to binary archive.
- ① [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_1/runs/impl_1/spi_wrapper_placed.dcp' has been generated.
- > ① [runrtl-4] Executing : report_io -file spi_wrapper_io_placed.rpt (2 more like this)
- Route Design (1 critical warning, 3 warnings, 38 infos)
 - ① [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
 - ① [Vivado_Tcl 4-198] DRC finished with 0 Errors
 - ① [Vivado_Tcl 4-199] Please refer to the DRC report ([report_drc](#)) for more information.
 - ① [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
 - > ① [Route 35-416] Intermediate Timing Summary | WNS=4.164 | TNS=0.000 | WHS=-1.152 | THS=-79.452| (6 more like this)
 - ① [Route 35-459] Router was unable to fix hold violation on 2 pins. This could be due to a combination of congestion_blockages and run-time limitations. Such pins are:

Tcl Console Messages Log Reports Design Runs

Q | X | ↻ | ⌂ | T | M | B | Critical warning (2) Warning (7) Info (252) Status (511) Show All

- ① [Route 35-459] Router was unable to fix hold violation on 2 pins. This could be due to a combination of congestion, blockages and run-time limitations. Such pins are:
u_ll_a_0/instlla_core_inst/lshifted_data_in_reg[7]0_srl8/D
u_ll_a_0/instlla_core_inst/probeDelay[0]_1[2]
- Resolution: You may try high effort hold fixing by turning on param route.enableGlobalHolditer.
- ① [Route 35-57] Estimated Timing Summary | WNS=3.019 | TNS=0.000 | WHS=-0.273 | THS=-0.390 |
- ① [Route 35-328] Router estimated timing not met.
- Resolution: For a complete and accurate timing signoff, [report_timing_summary](#) must be run after [route_design](#). Alternatively, [route_design](#) can be run with the -timing_summary option to enable a complete timing signoff at the end of [route_design](#).
- ① [Route 35-16] Router Completed Successfully
- ① [Common 17-83] Releasing license: Implementation
- ① [Timing 38-480] Writing timing data to binary archive.
- ① [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_1/runs/impl_1/spi_wrapper_routed.dcp' has been generated.
- ① [IP_Flow 19-1839] IP Catalog is up to date.
- > ① [DRC 23-27] Running DRC with 2 threads (1 more like this)
- ① [Corertl 2-168] The results of DRC are in file [spi_wrapper_drc_routed.rpt](#).
- > ① [runrtl-4] Executing : report_drc -file spi_wrapper_drc_routed.rpt -pb spi_wrapper_drc_routed.pb -px spi_wrapper_drc_routed.ppx (7 more like this)
- > ① [Timing 38-35] Done setting XDC timing constraints. (2 more like this)

```

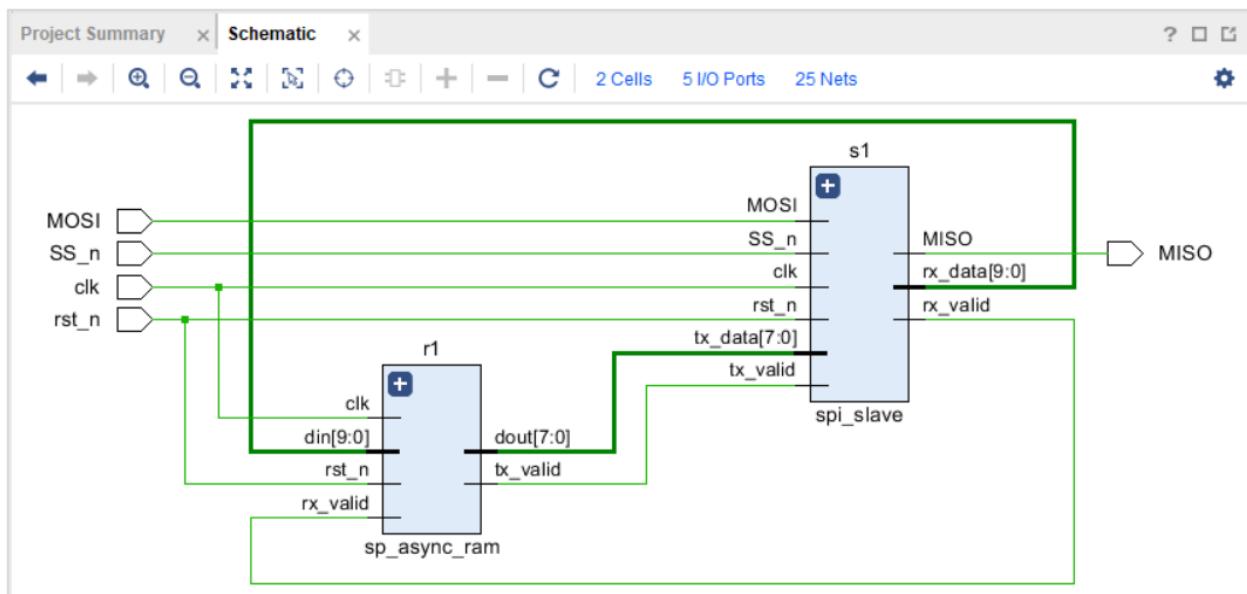
➊ [IP_Flow 19-1839] IP Catalog is up to date.
> ➋ [DRC 23-27] Running DRC with 2 threads (1 more like this)
➋ [Corertl 2-168] The results of DRC are in file spi\_wrapper\_drc\_routed.rpt.
> ➋ [rundcl-4] Executing : report_drc -file spi_wrapper_drc_routed.rpt -pb spi_wrapper_drc_routed.pb -rpx spi_wrapper_drc_routed.rpx (7 more like this)
➋ [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
➋ [DRC 23-133] Running Methodology with 2 threads
➋ [Corertl 2-1520] The results of Report Methodology are in file spi\_wrapper\_methodology\_drc\_routed.rpt.
➌ [Timing 38-282] The design failed to meet the timing requirements. Please see the timing summary report for details on the timing violations.
➍ [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.
➋ [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
> ➋ [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
➋ [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)

```

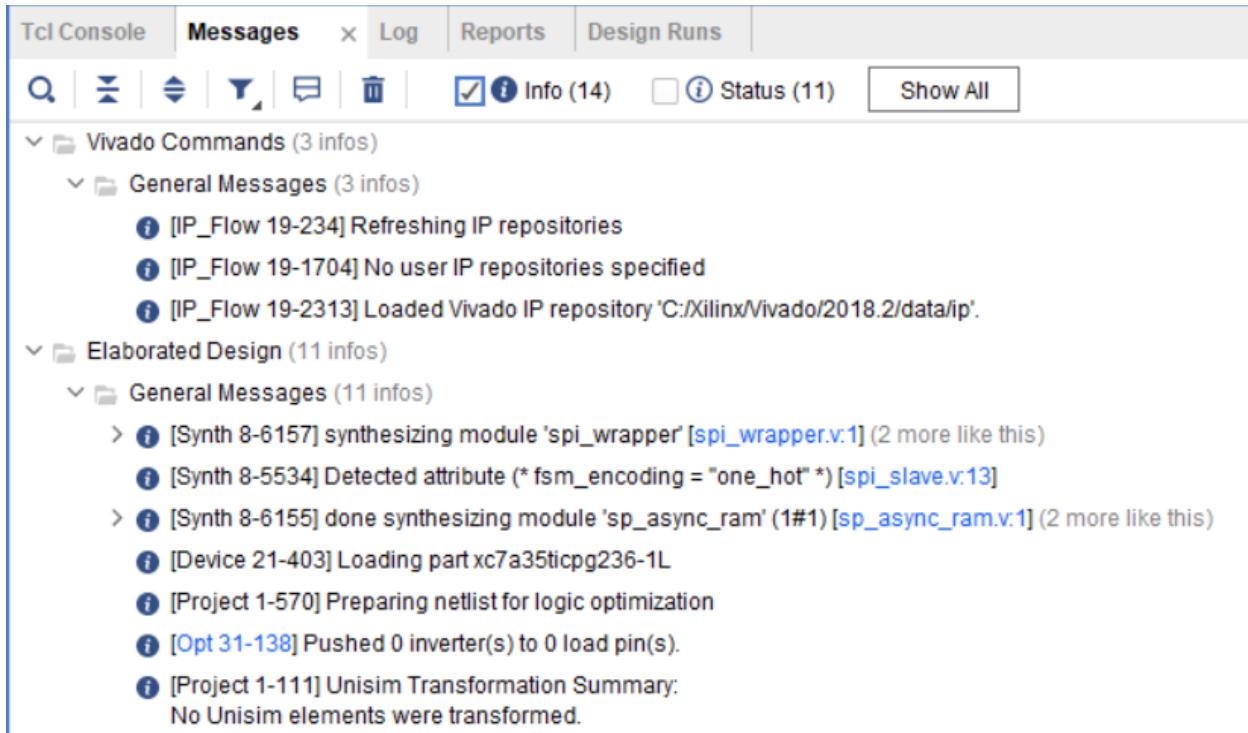
One_Hot Encoding Snippets:

Elaboration:

Schematic:

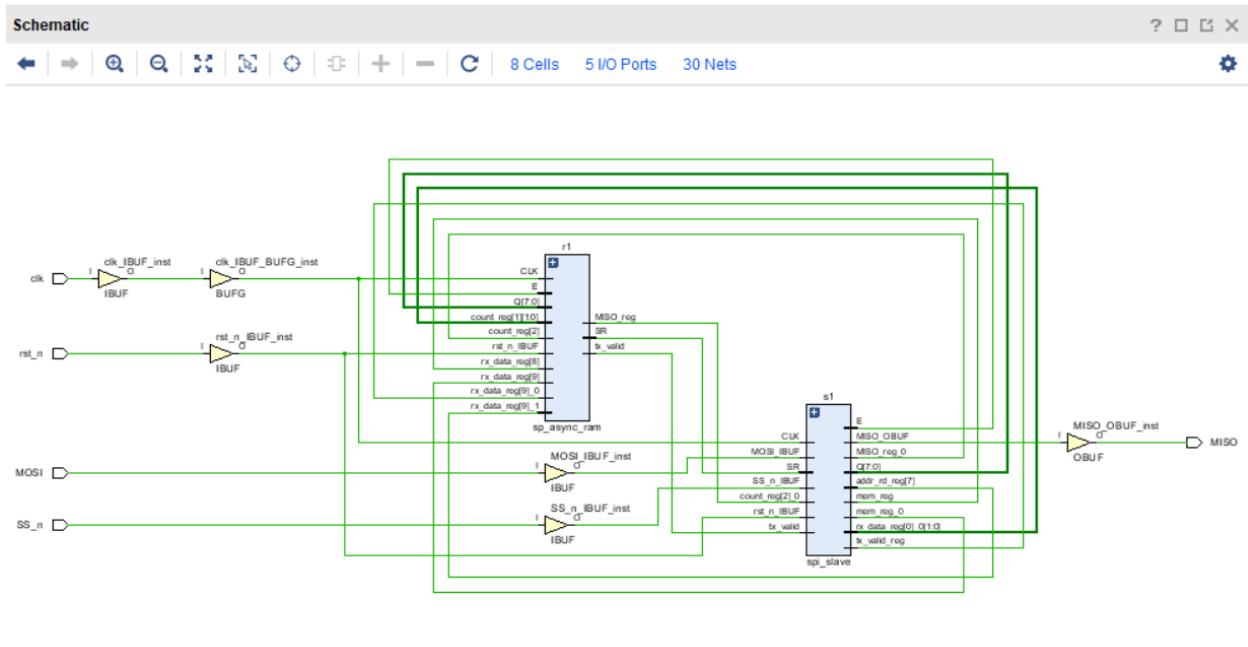


Messages Tab:



Synthesis:

Schematic:



Messages Tab:

Tcl Console **Messages** Log Reports Design Runs Debug

Warning (1) Info (42) Status (19) Show All

- ✓ Vivado Commands (3 infos)
 - ✓ General Messages (3 infos)
 - ✓ [IP_Flow 19-234] Refreshing IP repositories
 - ✓ [IP_Flow 19-1704] No user IP repositories specified
 - ✓ [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
 - ✓ Synthesis (1 warning, 33 infos)
 - ✓ [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
 - > ✓ [Synth 8-6157] synthesizing module 'spi_wrapper' [[spi_wrapper.v1](#)] (2 more like this)
 - ✓ [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [[spi_slave.v13](#)]
 - > ✓ [Synth 8-6155] done synthesizing module 'sp_async_ram' (1#1) [[sp_async_ram.v1](#)] (2 more like this)
 - ✓ [Device 21-403] Loading part xc7a35ticpg236-1L

Tcl Console **Messages** Log Reports Design Runs Debug ? □

Warning (1) Info (42) Status (19) Show All

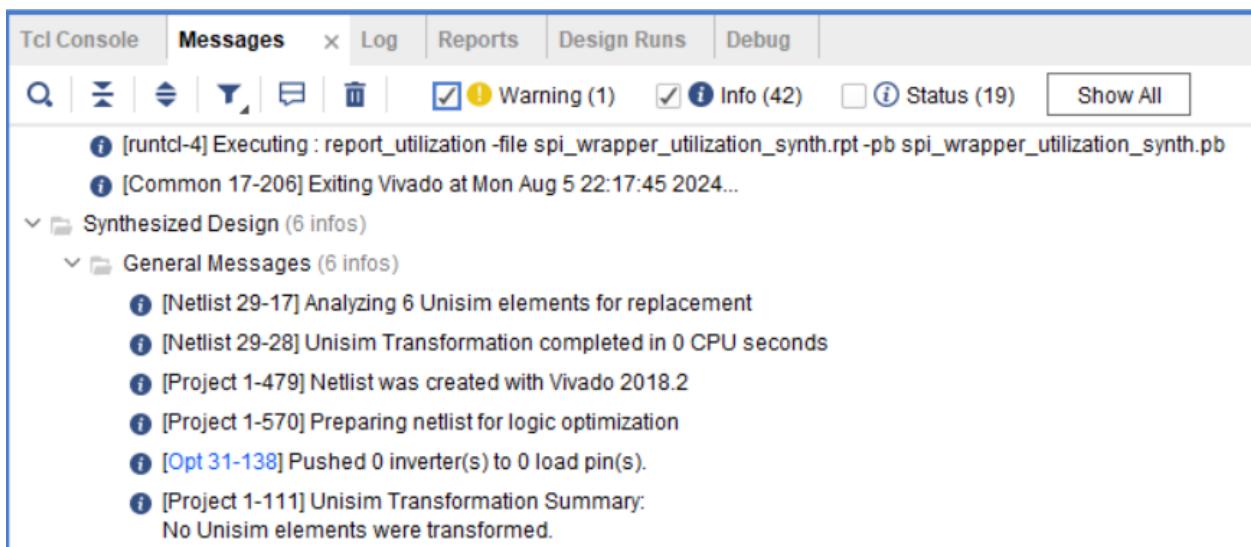
✓ [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/Constraints_basys3_original.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xil/spi_wrapper_propimpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

- > ✓ [Synth 8-5544] ROM "addr_wr" won't be mapped to Block RAM because address size (2) smaller than threshold (5) (6 more like this)
- ✓ [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'spi_slave'
- ✓ [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave'
- > ✓ [Synth 8-4480] The timing for the instance i_0/r1/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
- ✓ [Project 1-571] Translating synthesized netlist
- ✓ [Netlist 29-17] Analyzing 6 Unisim elements for replacement
- ✓ [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

Tcl Console **Messages** Log Reports Design Runs Debug

Warning (1) Info (42) Status (19) Show All

- > ✓ [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- ✓ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > ✓ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- ✓ [Common 17-83] Releasing license. Synthesis
- ✓ [Constraints 18-5210] No constraint will be written out.
- ✓ [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_2/project_2.runs/synth_1/spi_wrapper.dcp' has been generated.
- ✓ [rundc-4] Executing : report_utilization -file spi_wrapper_utilization_synth.rpt -pb spi_wrapper_utilization_synth.pb
- ✓ [Common 17-206] Exiting Vivado at Mon Aug 5 22:17:45 2024...
- ✓ Synthesized Design (6 infos)
 - ✓ General Messages (6 infos)



Utilization Report:

The screenshot shows the Vivado Utilization Report window. The utilization table is as follows:

Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
N spi_wrapper	27	39	1	0.5	5	1	0	
r1(sp_async_ram)	3	17	1	0.5	0	0	0	
s1(sp_slave)	24	22	0	0	0	0	0	

Timing Report:

The screenshot shows the Timing tab selected in a software interface. On the left, there's a tree view with nodes like General Information, Timer Settings, Design Timing Summary (which is expanded), Clock Summary (1), Check Timing (4), Intra-Clock Paths, Inter-Clock Paths, Other Path Groups, and User Ignored Paths. The main pane displays the 'Design Timing Summary' with sections for Setup, Hold, and Pulse Width. Under Setup, it shows Worst Negative Slack (WNS) as 6.261 ns, Total Negative Slack (TNS) as 0.000 ns, Number of Failing Endpoints as 0, and Total Number of Endpoints as 100. Under Hold, it shows Worst Hold Slack (WHS) as 0.139 ns, Total Hold Slack (THS) as 0.000 ns, Number of Failing Endpoints as 0, and Total Number of Endpoints as 100. Under Pulse Width, it shows Worst Pulse Width Slack (WPWS) as 4.500 ns, Total Pulse Width Negative Slack (TPWS) as 0.000 ns, Number of Failing Endpoints as 0, and Total Number of Endpoints as 42. A message at the bottom states "All user specified timing constraints are met." Below the main pane, a tab labeled "Timing Summary - timing_1" is visible.

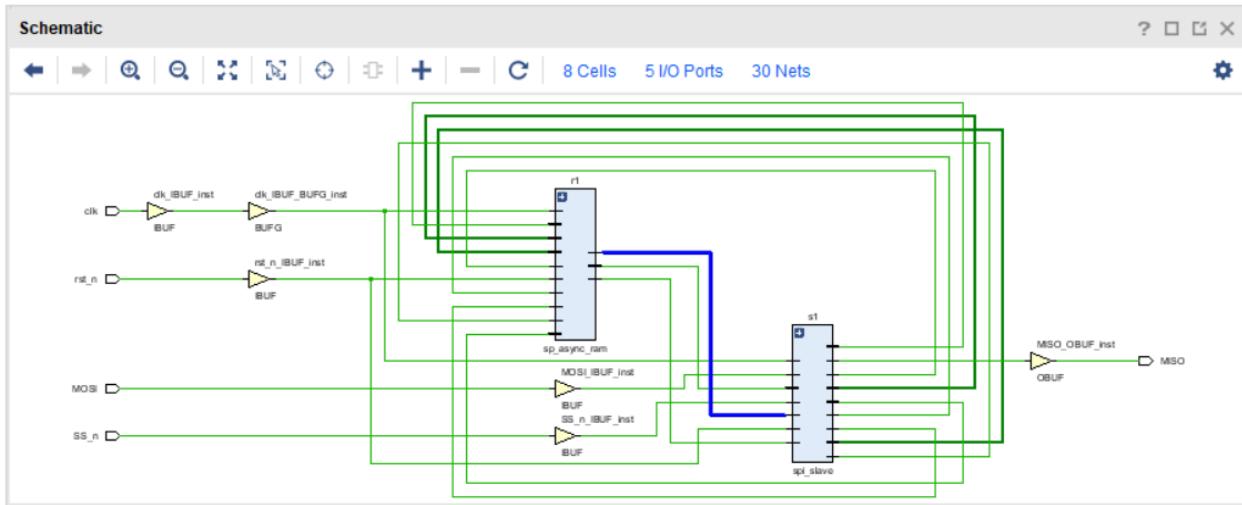
Synthesis Report:

The screenshot shows a synthesis report window titled "synth_1_synth_synthesis_report_0 - synth_1". The status bar indicates the file path: D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_2/runs/synth_1/spi_wrapper.vds. The report is "Read-only". The text content includes module parameters (READ_ADD, READ_DATA), synthesis info messages (INFO: [Synth 8-5534], INFO: [Synth 8-6155]), and a summary line: "Finished RTL Elaboration : Time (s): cpu = 00:00:06 ; elapsed = 00:00:07 . Memory (MB): peak = 410.461 ; gain = 153.930". It also includes a "Report Check Netlist" section with a table showing errors, warnings, and status for multi-driven nets.

The screenshot shows a synthesis report window titled "synth_1_synth_synthesis_report_0 - synth_1". The status bar indicates the file path: D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_2/runs/synth_1/spi_wrapper.vds. The report is "Read-only". The text content includes an info message about ROM mapping, a state encoding table for a FSM, and a summary line: "Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:59 ; elapsed = 00:01:03 . Memory (MB): peak = 763.812 ; gain".

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
READ_DATA	00100	100
READ_ADD	01000	011
WRITE	10000	010

Critical Path:



Implementation:

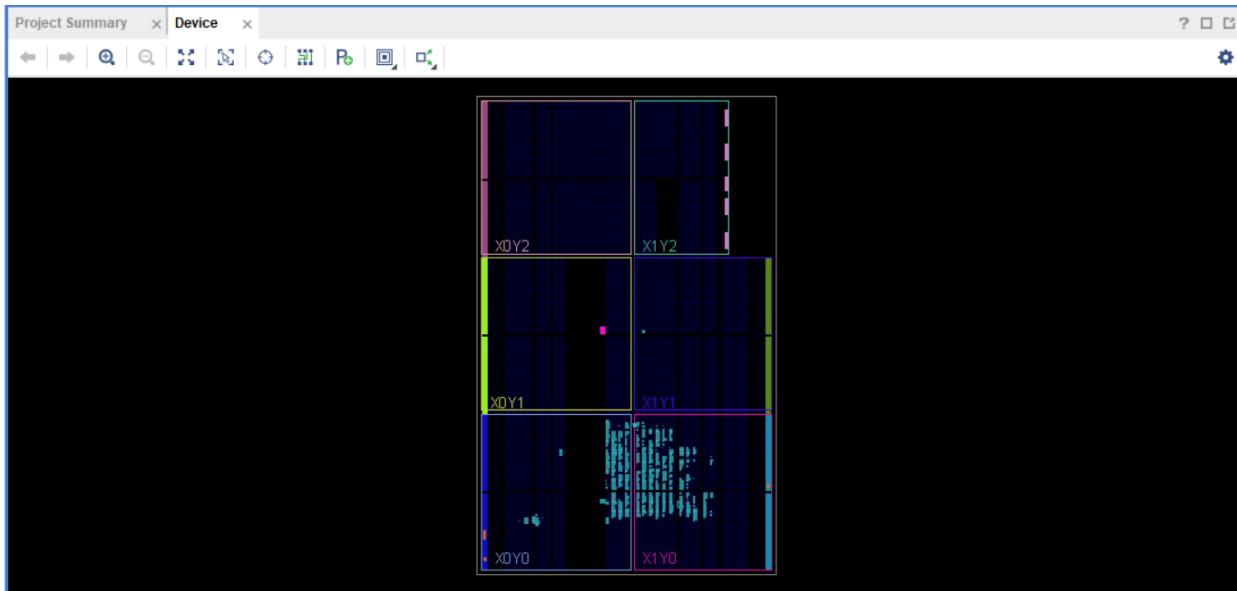
Utilization Report:

Hierarchy												
	Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCAN2 (4)
N	spi_wrapper	1265	1955	11	633	1157	108	739	1	5	2	1
> I	dbg_hub (dbg_hub)	475	727	0	241	451	24	303	0	0	1	1
I	r1 (sp_async_ram)	3	17	1	5	3	0	0	0.5	0	0	0
I	s1 (spi_slave)	24	22	0	9	24	0	12	0	0	0	0
> I	U_ilia_0 (u_ilia_0)	763	1189	10	386	679	84	422	0.5	0	0	0

Timing Report:

Design Timing Summary											
General Information				Setup				Hold			
Timer Settings				Worst Negative Slack (WNS): 2.759 ns				Worst Hold Slack (WHS): 0.016 ns			
Design Timing Summary				Total Negative Slack (TNS): 0.000 ns				Total Hold Slack (THS): 0.000 ns			
Clock Summary (2)				Number of Failing Endpoints: 0				Number of Failing Endpoints: 0			
> I Check Timing (4)				Total Number of Endpoints: 3885				Total Number of Endpoints: 3869			
> I Intra-Clock Paths											
> I Inter-Clock Paths											
All user specified timing constraints are met.											
Timing Summary - impl_1 (saved)				Timing Summary - timing_1							

FPGA Device:



Messages Tab:

The screenshot shows the 'Messages' tab in the Vivado interface. The top navigation bar includes tabs for 'Tcl Console', 'Messages', 'Log', 'Reports', and 'Design Runs'. Below the tabs is a toolbar with icons for search, filter, and file operations. The main pane displays a hierarchical list of build logs:

- Implementation (2 warnings, 131 infos)
 - [Netlist 29-17] Analyzing 6 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a35ticpg236-1L
 - [Project 1-570] Preparing netlist for logic optimization
 - [Timing 38-478] Restoring timing data from binary archive.
 - [Timing 38-479] Binary timing data restore complete.
 - [Project 1-856] Restoring constraints from binary archive.
 - [Project 1-853] Binary constraint restore complete.
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
 - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
- Design Initialization (11 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
 - [Project 1-461] DRC finished with 0 Errors
- Opt Design (35 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
 - [Project 1-461] DRC finished with 0 Errors

Tcl Console Messages Log Reports Design Runs

Q | X | 🔍 | T | M | 🗑 | Critical warning (1) Warning (5) Info (298) Status (533) Show All

- ⓘ [Project 1-462] Please refer to the DRC report (report_drc) for more information.
- ⓘ [IP_Flow 19-234] Refreshing IP repositories
- ⓘ [IP_Flow 19-1704] No user IP repositories specified
- ⓘ [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- > ⓘ [Chipscope 16-329] Generating Script for core instance : dbg_hub (1 more like this)
- > ⓘ [IP_Flow 19-3806] Processing IP xilinx.com:ip:xsdbm:3.0 for cell dbg_hub_CV. (1 more like this)
- ⓘ [Opt 31-49] Retargeted 0 cell(s).
- > ⓘ [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)
- > ⓘ [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
- ⓘ [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
- ⓘ [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
- > ⓘ [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
- ⓘ [Pwropt 34-9] Applying IDT optimizations ...
- ⓘ [Pwropt 34-10] Applying ODC optimizations ...
- ⓘ [Physopt 32-619] Estimated Timing Summary | WNS=4.856 | TNS=0.000 |
- ⓘ [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 2 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.
- ⓘ [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports

Tcl Console Messages Log Reports Design Runs

Q | X | 🔍 | T | M | 🗑 | Critical warning (1) Warning (5) Info (298) Status (533) Show All

- ⓘ [Common 17-83] Releasing license: Implementation
- ⓘ [Timing 38-480] Writing timing data to binary archive.
- ⓘ [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_2/runs/impl_1/spi_wrapper_opt.dcp' has been generated.
- ⓘ [runrtl-4] Executing : report_drc -file spi_wrapper_drc_opted.rpt -pb spi_wrapper_drc_opted.pb -rpx spi_wrapper_drc_opted.rpx
- ⓘ [IP_Flow 19-1839] IP Catalog is up to date.
- > ⓘ [DRC 23-27] Running DRC with 2 threads (1 more like this)
- ⓘ [Coretl 2-168] The results of DRC are in file spi_wrapper_drc_opted.rpt.
- ▼ Place Design (24 infos)
 - ⓘ [Chipscope 16-240] Debug cores have already been implemented
 - ⓘ [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
 - > ⓘ [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - > ⓘ [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
 - > ⓘ [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
 - ⓘ [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - > ⓘ [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 - ⓘ [Physopt 32-65] No nets found for high-fanout optimization.

Tcl Console Messages Log Reports Design Runs

Q | X | 🔍 | T | M | 🗑 | Critical warning (1) Warning (5) Info (298) Status (533) Show All

- ⓘ [Physopt 32-232] Optimized 0 net. Created 0 new instance.
- ⓘ [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
- ⓘ [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
- ⓘ [Place 30-746] Post Placement Timing Summary WNS=4.824. For the most accurate timing information please run report_timing.
- ⓘ [Common 17-83] Releasing license: Implementation
- ⓘ [Timing 38-480] Writing timing data to binary archive.
- ⓘ [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_2/runs/impl_1/spi_wrapper_placed.dcp' has been generated.
- > ⓘ [runrtl-4] Executing : report_io -file spi_wrapper_io_placed.rpt (2 more like this)
- ▼ Route Design (1 warning, 38 infos)
 - ⓘ [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
 - ⓘ [Vivado_Tcl 4-198] DRC finished with 0 Errors
 - ⓘ [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
 - ⓘ [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
 - > ⓘ [Route 35-416] Intermediate Timing Summary | WNS=4.841 | TNS=0.000 | WHS=-1.242 | THS=-84.656| (5 more like this)
 - ⓘ [Route 35-57] Estimated Timing Summary | WNS=2.756 | TNS=0.000 | WHS=0.015 | THS=0.000 |
 - ⓘ [Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summary.
 - ⓘ [Route 35-16] Router Completed Successfully

Tcl Console **Messages** x Log Reports Design Runs

Q | Critical warning (1) Warning (5) Info (298) Status (533) Show All

- info [Common 17-83] Releasing license: Implementation
- info [Timing 38-480] Writing timing data to binary archive.
- info [Common 17-1381] The checkpoint D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_2/runs/impl_1/spi_wrapper_routed.dcp has been generated.
- info [IP_Flow 19-1839] IP Catalog is up to date.
- > info [DRC 23-27] Running DRC with 2 threads (1 more like this)
- info [CoreDl 2-168] The results of DRC are in file `spi_wrapper_drc_routed.rpt`.
- > info [runrtl-4] Executing : report_drc -file spi_wrapper_drc_routed.rpt -pb spi_wrapper_drc_routed.pb -rpx spi_wrapper_drc_routed.rpx (7 more like this)
- > info [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
- info [DRC 23-133] Running Methodology with 2 threads
- info [CoreDl 2-1520] The results of Report Methodology are in file `spi_wrapper_methodology_drc_routed.rpt`.
- info [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.
- info [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
- > info [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
- > info [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)

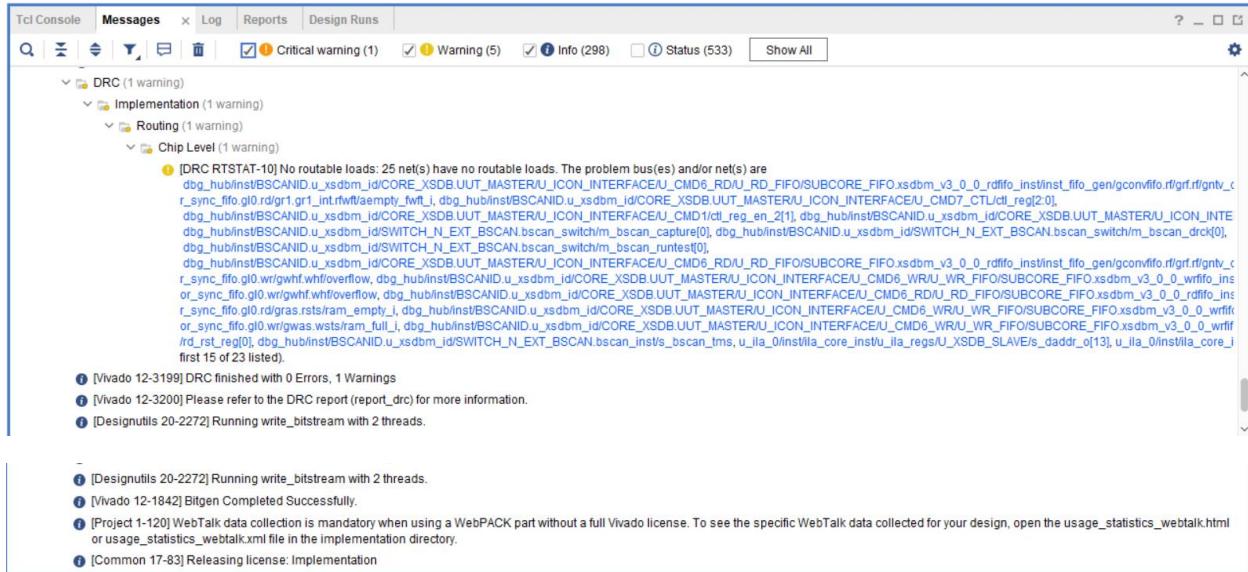
▼ Write Bitstream (1 warning, 23 infos)

- info [Netlist 29-17] Analyzing 104 Unisim elements for replacement
- info [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

Tcl Console **Messages** x Log Reports Design Runs

Q | Critical warning (1) Warning (5) Info (298) Status (533)

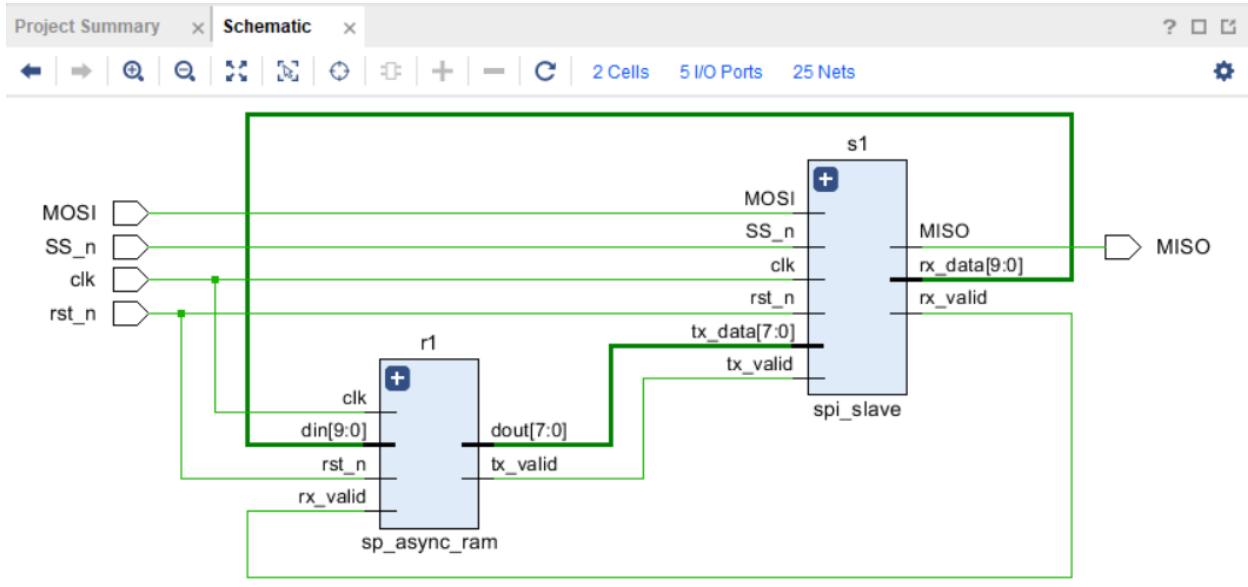
- info [Project 1-479] Netlist was created with Vivado 2018.2
- info [Device 21-403] Loading part xc7a35ticpg236-1L
- info [Project 1-570] Preparing netlist for logic optimization
- info [Chipscope 16-324] Core: u_ila_0 UUID: 23e7d65a-79bc-59f7-bc47-406c1714dfaef
- info [Timing 38-478] Restoring timing data from binary archive.
- info [Timing 38-479] Binary timing data restore complete.
- info [Project 1-856] Restoring constraints from binary archive.
- info [Project 1-853] Binary constraint restore complete.
- info [Project 1-111] Unisim Transformation Summary:
A total of 54 instances were transformed.
CFGLUT5 => CFGLUT5 (SRLC32E, SRL16E): 48 instances
RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 6 instances
- info [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
- info [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35t'
- info [IP_Flow 19-234] Refreshing IP repositories
- info [IP_Flow 19-1704] No user IP repositories specified
- info [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- info [DRC 23-27] Running DRC with 2 threads



Sequential Encoding Snippets:

Elaboration:

Schematic:



Messages Tab:

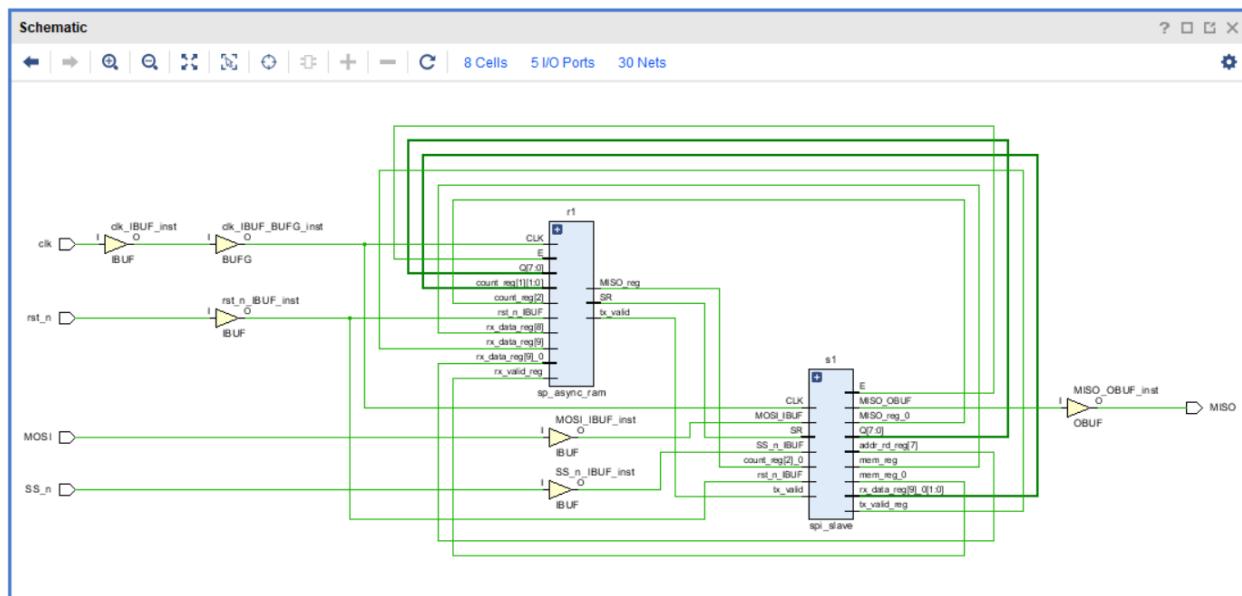
Tcl Console | **Messages** | Log | Reports | Design Runs |

Q | X | Log | Status | Show All | Info (14) | Status (11)

- ▼ Vivado Commands (3 infos)
 - ▼ General Messages (3 infos)
 - Info [IP_Flow 19-234] Refreshing IP repositories
 - Info [IP_Flow 19-1704] No user IP repositories specified
 - Info [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- ▼ Elaborated Design (11 infos)
 - ▼ General Messages (11 infos)
 - Info [Synth 8-6157] synthesizing module 'spi_wrapper' [spi_wrapper.v:1] (2 more like this)
 - Info [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential" *) [spi_slave - seq.v:13]
 - Info [Synth 8-6155] done synthesizing module 'sp_async_ram' (1#1) [sp_async_ram.v:1] (2 more like this)
 - Info [Device 21-403] Loading part xc7a35ticpg236-1L
 - Info [Project 1-570] Preparing netlist for logic optimization
 - Info [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - Info [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Synthesis:

Schematic:



Messages Tab:

Tcl Console Messages Log Reports Design Runs Debug ? _ X

Q | X | D | T | M | B | Show All

Warning (1) Info (42) Status (19)

Vivado Commands (3 infos)

- General Messages (3 infos)
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- Synthesis (1 warning, 33 infos)
 - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
 - [Synth 8-6157] synthesizing module 'spi_wrapper' [spi_wrapper.v]
 - [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential") [spi_slave - seq.v:13]
 - [Synth 8-6155] done synthesizing module 'sp_async_ram' (#1) [sp_async_ram.v:1]
 - [Device 21-403] Loading part xc7a35t^{icpg236-1L}
 - [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/Constraints_basys3_original_3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xil/spi_wrapper_propImpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Tcl Console Messages Log Reports Design Runs Debug ? _ X

Q | X | D | T | M | B | Show All

Warning (1) Info (42) Status (19)

- [Synth 8-5544] ROM "addr_wr" won't be mapped to Block RAM because address size (2) smaller than threshold (5) (6 more like this)
- [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'spi_slave'
- [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'spi_slave'
- [Synth 8-4480] The timing for the instance '_l/r/mem_reg' (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 6 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_3/runs/synth_1/spi_wrapper.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file spi_wrapper_utilization_rpt.rpt -pb spi_wrapper_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Mon Aug 5 22:38:58 2024...

Tcl Console Messages Log Reports Design Runs Debug ? _ X

Q | X | D | T | M | B | Show All

Warning (1) Info (42) Status (19)

No Unisim elements were transformed. (1 more like this)

- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_3/runs/synth_1/spi_wrapper.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file spi_wrapper_utilization_rpt.rpt -pb spi_wrapper_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Mon Aug 5 22:38:58 2024...

Synthesized Design (6 infos)

- General Messages (6 infos)
 - [Netlist 29-17] Analyzing 6 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Utilization Report:

The Utilization Report window displays the utilization of various resources across the design. The hierarchy tree on the left shows categories like Slice Logic, Memory, and DSP. The main table provides a detailed breakdown of resources used by specific components.

Name	1	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_wrapper	23	37	1	0.5	5	1	
r1(sp_async_ram)	3	17	1	0.5	0	0	
s1(sp_slave)	20	20	0	0	0	0	

Timing Report:

The Timing Report window displays timing constraints and their violations. The left sidebar lists various timing analysis categories. The main area shows the Design Timing Summary, which includes columns for Setup, Hold, and Pulse Width, along with a summary message indicating all constraints are met.

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.261 ns	Worst Hold Slack (WHS): 0.148 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 98	Total Number of Endpoints: 98	Total Number of Endpoints: 40

Synthesis Report:

The Synthesis Report window displays the synthesis log for the module 'spi_wrapper'. The log shows parameters defined, synthesis completed for modules 'spi_slave' and 'spi_wrapper', and a final message indicating the completion of RTL elaboration.

```

Parameter WRITE bound to: 3'b010
Parameter READ_ADD bound to: 3'b011
Parameter READ_DATA bound to: 3'b100
INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential" *) [D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_3/project_3.runs/synth_1/spi_wrapper.vds]
INFO: [Synth 8-6155] done synthesizing module 'spi_slave' (2#1) [D:/sublime_text/sublime_text_build_4169_x64/Projects/P
INFO: [Synth 8-6155] done synthesizing module 'spi_wrapper' (3#1) [D:/sublime_text/sublime_text_build_4169_x64/Projects
-----
Finished RTL Elaboration : Time (s): cpu = 00:00:16 ; elapsed = 00:00:18 . Memory (MB): peak = 409.441 ; gain = 153.141
-----
Report Check Netlist:
+-----+-----+-----+-----+
| Item | Errors | Warnings | Status | Description |
+-----+-----+-----+-----+
| 1 | multi_driven_nets | 0 | 0 | Passed | Multi driven nets |
+-----+

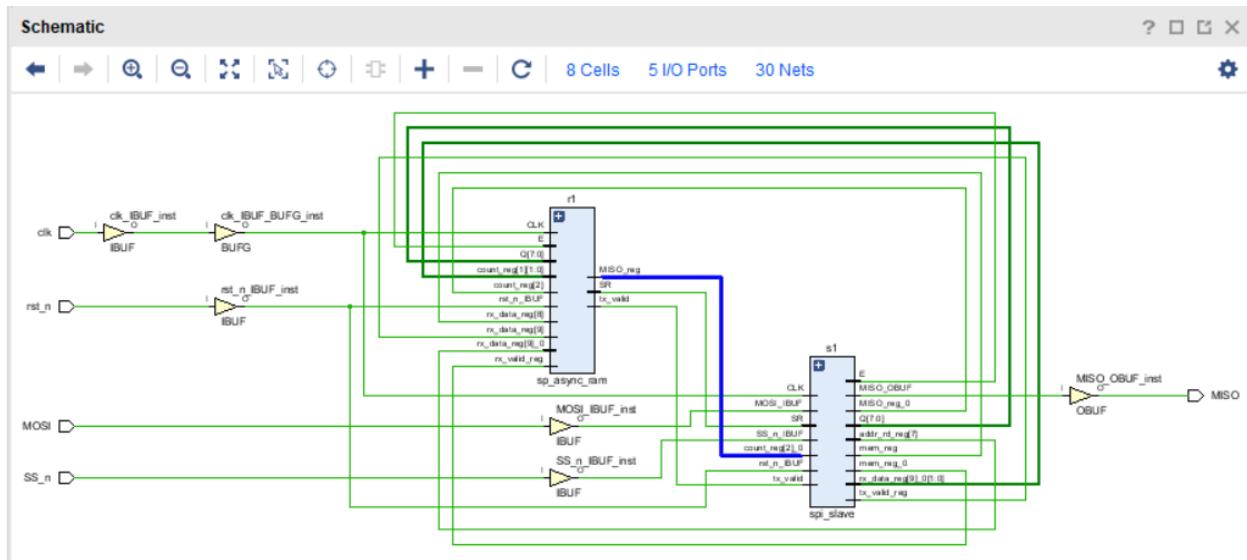
```

```

INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
-----
| State | New Encoding | Previous Encoding |
|-----|
| IDLE | 000 | 000 |
| CHK_CMD | 001 | 001 |
| READ_DATA | 010 | 100 |
| READ_ADD | 011 | 011 |
| WRITE | 100 | 010 |
-----
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'spi_slave'

```

Critical Path:



Implementation:

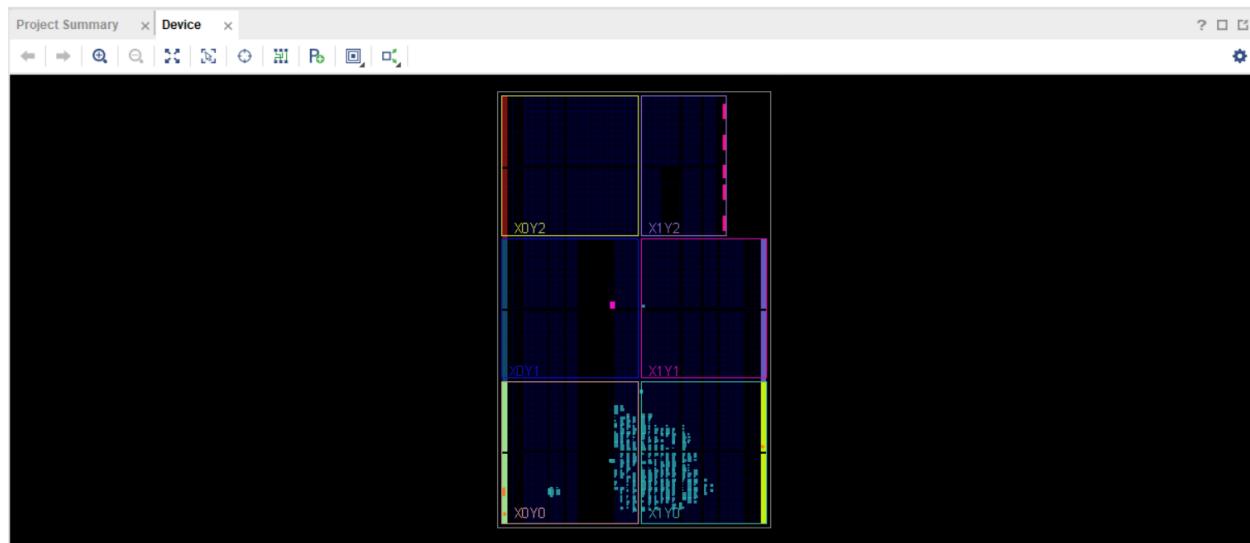
Utilization Report:

Utilization												
	Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
Hierarchy												
Summary												
Slice Logic												
Slice LUTs (6%)												
LUT as Memory (1%)												
LUT as Shift Register												
LUT as Distributed R/												
LUT as Logic (6%)												
F7 Muxes (<1%)												
dbg_hub (dbg_hub)	1261	1953	11	620	1153	108	739	1	5	2	1	1
r1 (sp_async_ram)	475	727	0	226	451	24	309	0	0	1	0	0
s1 (spi_slave)	3	17	1	5	3	0	0	0.5	0	0	0	0
u_il_0 (u_il_0)	20	20	0	10	20	0	8	0	0	0	0	0
u_il_0 (u_il_0)	763	1189	10	389	679	84	420	0.5	0	0	0	0

Timing Report:



FPGA Device:



Messages Tab:

Tcl Console **Messages** Log Reports Design Runs

Critical warning (2) Warning (7)

- Implementation (1 critical warning, 3 warnings, 107 infos)
 - Design Initialization (11 infos)
 - [Netlist 29-17] Analyzing 6 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a35ticpg236-1L
 - [Project 1-570] Preparing netlist for logic optimization
 - [Timing 38-478] Restoring timing data from binary archive.
 - [Timing 38-479] Binary timing data restore complete.
 - [Project 1-856] Restoring constraints from binary archive.
 - [Project 1-853] Binary constraint restore complete.
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
 - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
 - Opt Design (35 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
 - [Project 1-461] DRC finished with 0 Errors

Tcl Console **Messages** Log Reports Design Runs

Critical warning (2) Warning (7) Info (250) Status (505) Show All

- [Project 1-462] Please refer to the DRC report (report_drc) for more information.
- [IP_Flow 19-234] Refreshing IP repositories
- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- > [Chipscope 16-329] Generating Script for core instance : dbg_hub (1 more like this)
- > [IP_Flow 19-3806] Processing IP xilinx.com:ip:xsdbm:3.0 for cell dbg_hub_CV. (1 more like this)
- [Opt 31-49] Retargeted 0 cell(s).
- > [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)
- > [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
- [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
- [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
- > [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
- [Pwropt 34-9] Applying IDT optimizations ...
- [Pwropt 34-10] Applying ODC optimizations ...
- [Physopt 32-619] Estimated Timing Summary | WNS=4.856 | TNS=0.000 |
- [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 2 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.
- [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports

Tcl Console Messages Log Reports Design Runs

Critical warning (2) Warning (7) Info (250) Status (505) Show All

- ⓘ [Common 17-83] Releasing license: Implementation
- ⓘ [Timing 38-480] Writing timing data to binary archive.
- ⓘ [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_3/runs/impl_1/spi_wrapper_opt.dcp' has been generated.
- ⓘ [rundlc-4] Executing : report_drc -file spi_wrapper_drc_opted.rpt -pb spi_wrapper_drc_opted.pb -rpx spi_wrapper_drc_opted.rpx
- ⓘ [IP_Flow 19-1839] IP Catalog is up to date.
- > ⓘ [DRC 23-27] Running DRC with 2 threads (1 more like this)
- ⓘ [Coretdl 2-168] The results of DRC are in file [spi_wrapper_drc_opted.rpt](#).
- Place Design (24 infos)
 - ⓘ [Chipscope 16-240] Debug cores have already been implemented
 - ⓘ [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
 - > ⓘ [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - > ⓘ [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
 - > ⓘ [Vivado_Tcl 4-199] Please refer to the DRC report ([report_drc](#)) for more information. (1 more like this)
 - ⓘ [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
 - ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - > ⓘ [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 - ⓘ [Physopt 32-65] No nets found for high-fanout optimization.

Tcl Console Messages Log Reports Design Runs

Critical warning (2) Warning (7) Info (250) Status (505) Show All

- ⓘ [Physopt 32-232] Optimized 0 net. Created 0 new instance.
- ⓘ [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
- ⓘ [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
- ⓘ [Place 30-746] Post Placement Timing Summary WNS=4.510. For the most accurate timing information please run [report_timing](#).
- ⓘ [Common 17-83] Releasing license: Implementation
- ⓘ [Timing 38-480] Writing timing data to binary archive.
- ⓘ [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_3/runs/impl_1/spi_wrapper_placed.dcp' has been generated.
- > ⓘ [rundlc-4] Executing : report_io -file spi_wrapper_io_placed.rpt (2 more like this)
- Route Design (1 critical warning, 3 warnings, 37 infos)
 - ⓘ [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
 - ⓘ [Vivado_Tcl 4-198] DRC finished with 0 Errors
 - ⓘ [Vivado_Tcl 4-199] Please refer to the DRC report ([report_drc](#)) for more information.
 - ⓘ [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
 - > ⓘ [Route 35-416] Intermediate Timing Summary | WNS=4.619 | TNS=0.000 | WHS=-1.194 | THS=-77.827 (5 more like this)
 - ⓘ [Route 35-459] Router was unable to fix hold violation on 2 pins. This could be due to a combination of congestion, blockages and run-time limitations. Such pins are:
u_ilia_0/instUila_core_instshifted_data_in_reg[7][0].sr8/D
u_ilia_0/instUila_core_instprobeDelay[10].l_1/2

Tcl Console Messages Log Reports Design Runs

Critical warning (2) Warning (7) Info (250) Status (505) Show All

Resolution: You may try high effort hold fixing by turning on param route.enableGlobalHoldAfter.

- ⓘ [Route 35-57] Estimated Timing Summary | WNS=3.300 | TNS=0.000 | WHS=-0.333 | THS=-0.583 |
- ⓘ [Route 35-328] Router estimated timing not met.
Resolution: For a complete and accurate timing signoff, [report_timing_summary](#) must be run after route_design. Alternatively, route_design can be run with the -timing_summary option to enable a complete timing signoff at the end of route_design.
- ⓘ [Route 35-16] Router Completed Successfully
- ⓘ [Common 17-83] Releasing license: Implementation
- ⓘ [Timing 38-480] Writing timing data to binary archive.
- ⓘ [Common 17-1381] The checkpoint 'D:/sublime_text/sublime_text_build_4169_x64/Projects/Project 2/project_3/runs/impl_1/spi_wrapper_routed.dcp' has been generated.
- ⓘ [IP_Flow 19-1839] IP Catalog is up to date.
- > ⓘ [DRC 23-27] Running DRC with 2 threads (1 more like this)
- ⓘ [Coretdl 2-168] The results of DRC are in file [spi_wrapper_drc_routed.rpt](#).
- > ⓘ [rundlc-4] Executing : report_drc -file spi_wrapper_drc_routed.rpt -pb spi_wrapper_drc_routed.pb -rpx spi_wrapper_drc_routed.rpx (7 more like this)
- > ⓘ [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
- ⓘ [DRC 23-133] Running Methodology with 2 threads
- ⓘ [Coretdl 2-1520] The results of Report Methodology are in file [spi_wrapper_methodology_drc_routed.rpt](#).
- ⓘ [Timing 38-282] The design failed to meet the timing requirements. Please see the timing summary report for details on the timing violations.

- [Timing 38-282] The design failed to meet the timing requirements. Please see the timing summary report for details on the timing violations.
 - [Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.
 - [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
- > ● [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
- > ● [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
-