Implementing EDF Scheduler

Name: mohamed mohamed taha
Email: mohamed.ismail.mohamed.taha@gmail.com

Verifies system implementation with the EDF scheduler

Using Analytical Methods

1/ System Hyperperiod

Task	Periodicity
Button 1 Monitor	50
Button 2 Monitor	50
Periodic Transmitter	100
UART Transmitter	20
Load 1 Simulation	10
Load 2 Simulation	100

1/ System Hyperperiod

$Hyperperiod$ = Least Common Multiplier of all tasks periodicities

$Hyperperiod = LCM$ (50, 50, 100, 20, 10, 100)

$Hyperperiod$ = 100

2/ CPU Load

Task	Execution Time	Occurrence During Hyperperiod
Button 1 Monitor	29 us	2
Button 2 Monitor	29 us	2
Periodic Transmitter	93 us	1
UART Transmitter	30 us	5
Load 1 Simulation	5 us	10
Load 2 Simulation	12 us	1

2/ CPU Load

Utilization = Total Execution Time During Hyperperiod / Hyperperiod

U =[(29u*2)+(29u*2)+(93u*1)+(30u*5)+(5m*10)+(12m*1) / 100m] * 100% = 62%

3/ System Schedulability

Using Rate Monotonic Utilization Bound:

$U \leq n[\ 2\ \hat{}(1/n) - 1]$
U = 0.623&& Urm = 0.734
Therefore U < Urm

The system is feasible (Schedulable).

3/ System Schedulability

Using Time Demand Analysis

$Wi(t) = ei + \sum^{i-1}_{k=0}[Pk]ek$

critical instant = 100ms

3/ System Schedulability

Task	Execution Time	Periodicity
Button 1 Monitor	29 us	50
Button 2 Monitor	29 us	50
Periodic Transmitter	93 us	100
UART Transmitter	30 us	20
Load 1 Simulation	5 us	10
Load 2 Simulation	12 us	100

3/ System Schedulability

Task 1: Button 1 Monitor (E: 29us, P: 50ms, Provided Time=50ms)

$w3$ (50) = 29μ + (50/10) 5m + (50/20) 30μ = 25. 059 ms , w(50) = 25. 059 < 50

Button 1 Monitor task is schedulable

3/ System Schedulability

Task 2: Button 2 Monitor (E: 29us, P: 50ms, Provided Time=50ms)

w 4 (50) = 29μ + (50/10) 5m + (50/20) 30μ + (50/50)29μ = 25. 087 ms w (50) = 25. 087 < 50

Button 2 Monitor task is schedulable

3/ System Schedulability

Task 3: Load 1 Simulation (E: 5ms, P: 10ms, Provided Time=10ms)

$w1$ (10) = 5m + 0 = 5, w (10) = 5 < 10

Load 1 Simulation task is schedulable.

3/ System Schedulability

Task 4: UART Receiver (E: 30us, P: 20ms, Provided Time=20ms)

$w2$ (20) = 30μ + (20/10) $5m$ = 10. 03 ms, w(20) = 10. 03 < 20

UART Receiver task is schedulable.

3/ System Schedulability

Task 5: Periodic Transmitter (E: 93 us , P: 100ms, Provided Time=100ms)

$w5$ (100) = 93μ + (100/10) $5m$ + (100/20) 30μ + (100/50)29μ + (100/50)29μ = 50. 359 ms

w(100) = 50. 359 < 100

Periodic Transmitter task is schedulable

3/ System Schedulability

Task 6 : Load 2 Simulation (E: 12ms , P: 100ms, Provided Time=100ms)

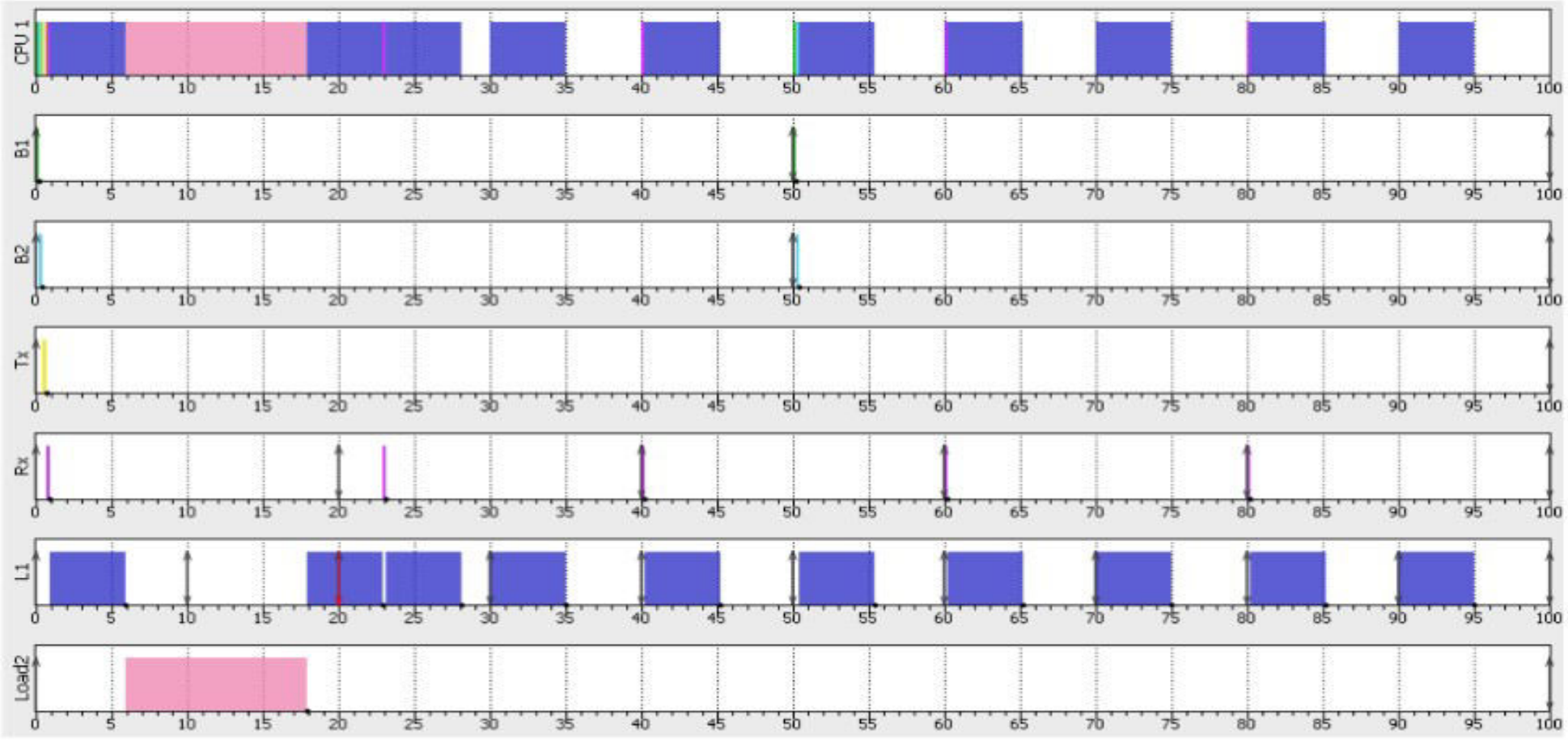
$w6$ (100) = 12m + (100/10)5m + (100/20)30μ + (100/50)29μ + (100/50)29μ + (100/100)93μ

w(100) = 62. 452 < 100

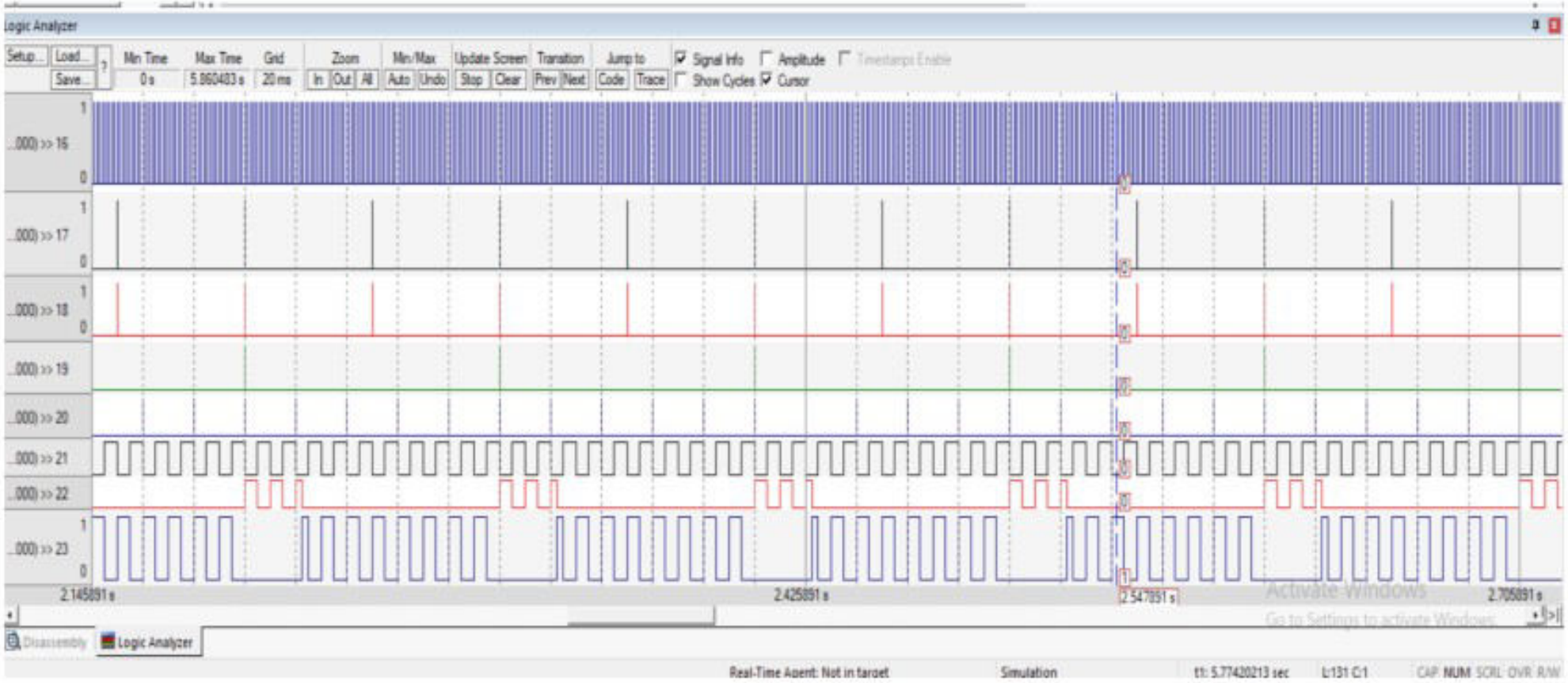
Load 2 Simulation Task is schedulable.

System is Schedulable

SIMSO Offline Simulator


CPU 1
B1
B2
Tx
Rx
L1
Load2
0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100

Kiel Simulator


Logic Analyzer
Setup...
Load...
Save...
Min Time
0 s
Max Time
5.860483 s
Grid
20 ms
Zoom
In
Out
All
Min/Max
Auto
Undo
Update Screen
Stop
Clear
Transition
Prev
Next
Jump to
Code
Trace
Signal Info
Amplitude
Show Cycles
Cursor
...000) >> 16
...000) >> 17
...000) >> 18
...000) >> 19
...000) >> 20
...000) >> 21
...000) >> 22
...000) >> 23
2.145891 s
2.425891 s
2.547891 s
2.705891 s
Disassembly
Logic Analyzer
Real-Time Agent: Not in target
Simulation
t1: 5.77420213 sec
L:131 C:1
CAP NUM SCRL OVR R/W

Watch 1

Name	Value	Type
L1_inTime	0x0013570F	uint
L2_inTime	0x0013526B	uint
Rx_inTime	0x00135713	uint
Tx_inTime	0x00134DBD	uint
cpu_load	63	uint
total_exeTime	0x000C37D2	uint
T1TC	0x001357C0	ulong
<Enter expression>		