

# Lab1

## ❖ Practical lab on STM32F103C6 Toggle LED

### ➤ High Pin -> ODR

The screenshot shows the Keil uVision IDE interface. The Logic Analyzer window displays a square wave signal on pin 13, indicating successful toggling. The code in `main.c` is as follows:

```
50 while(1){
51     GPIOA_ODR |= (1 << 13); // set bit 13
52     for(int i = 0; i < 5000; i++); // delay
53     GPIOA_ODR ^= (1 << 13); // clear bit 13
54     for(int i = 0; i < 5000; i++);
55 }
```

The GPIOA configuration window shows the following settings:

- Pin: 13
- Mode: Input
- CNF: Floating Input
- GPIOA\_CRH: 0x44244444
- GPIOA\_CRL: 0x44444444
- GPIOA\_IDR: 0x00002000
- GPIOA\_ODR: 0x00002000
- GPIOA\_LCKR: 0x00000000
- Pins: 0x00002000

The Command window shows the execution of the program, with the output of the `LA (PORTA & 0x00002000) >> 13` command displayed.

### ➤ Low Pin -> ODR

The screenshot shows the Keil uVision IDE interface. The Logic Analyzer window displays a square wave signal on pin 13, indicating successful toggling. The code in `main.c` is as follows:

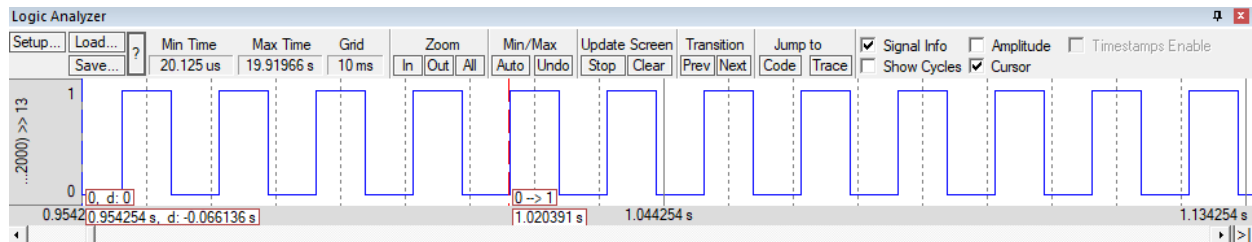
```
50 while(1){
51     GPIOA_ODR |= (1 << 13); // set bit 13
52     for(int i = 0; i < 5000; i++); // delay
53     GPIOA_ODR ^= (1 << 13); // clear bit 13
54     for(int i = 0; i < 5000; i++);
55 }
```

The GPIOA configuration window shows the following settings:

- Pin: 13
- Mode: Input
- CNF: Floating Input
- GPIOA\_CRH: 0x44244444
- GPIOA\_CRL: 0x44444444
- GPIOA\_IDR: 0x00000000
- GPIOA\_ODR: 0x00000000
- GPIOA\_LCKR: 0x00000000
- Pins: 0x00000000

The Command window shows the execution of the program, with the output of the `LA (PORTA & 0x00002000) >> 13` command displayed.

## ➤ Logic Analyzer



## ➤ MCU Clock (Default: HSI)

**Power, Reset and Clock Control (PRCC)**

**Clock Control & Configuration**

RCC\_CR:  ☐ CSSON ☐ HSEBYP ☐ HSERDY ☐ PLL Configuration

RCC\_CFGR:  ☐ HSEON ☒ HSIIRDY ☒ HSION

PPRE1:  MCO:  ☐ PLLON

PPRE2:  SW:  ☐ PLLRDY

HPRE:  SWS:  ☐ PLLSRC

ADCPRE:  PLLMUL:  ☐ PLLXTPRE

**Control/Status**

RCC\_CSR:  ☐ LPWRRSTF ☐ WWDGRSTF ☐ IWDGRSTF ☐ SFRSTF ☒ PORRSTF

☒ PINRSTF ☐ RMVF ☐ LSIRDY ☐ LSION

**Backup domain control**

RCC\_BDCR:  RTCSEL:

☐ BDRST ☐ RTCEN ☐ LSEBYP ☐ LSERDY ☐ LSEON

**Clock Interrupt**

RCC\_CIR:

☐ CSSC ☐ UNLKC ☐ PLLRDYC ☐ HSERDYC ☐ HSIIRDYC ☐ LSERDYC ☐ LSIRDYC

☐ CSSIE ☐ UNLKIE ☐ PLLRDYIE ☐ HSERDYIE ☐ HSIIRDYIE ☐ LSERDYIE ☐ LSIRDYIE

☐ CSSF ☐ UNLKF ☐ PLLRDYF ☐ HSERDYF ☐ HSIIRDYF ☐ LSERDYF ☐ LSIRDYF

**Power Control & Status**

PWR\_CR:  PLS:  ☐ DBP ☐ PVDE ☐ CSBF

PWR\_CSR:  ☐ EWUP ☐ CWUF ☐ PDDS ☐ LPDS

☐ PVDO ☐ SBF ☐ WUF

**Core & Memory and Peripheral Clocks**

OSC:  MHz RTCLK:  kHz HCLK:  MHz

OCS32:  kHz MCO:  MHz PCLK1:  MHz

HSI\_RC:  MHz IWDGCLK:  kHz PCLK2:  MHz

LSI\_RC:  kHz USBCLK:  MHz TIMCLK:  MHz

SYSCCLK:  MHz ADCCLK:  MHz TIM1CLK:  MHz

## Lab2

❖ Change the SYSCLK, HCLK, PCLK1, and PCLK2 with different frequencies

➤ Configure Board to run with the following rates:

- APB1 Bus Frequency 4MHz
- APB2 Bus Frequency 2MHz
- AHB Frequency 8MHz
- SYSCLK 8MHz
- Use only internal HIS\_RC

**Power, Reset and Clock Control (PRCC)**

**Clock Control & Configuration**

RCC\_CR: 0x00000083  
RCC\_CFGR: 0x00002C00

PPRE1: 4: HCLK / 2  
PPRE2: 5: HCLK / 4  
HPRE: 0: SYSCLK  
ADCPRE: 0: PCLK2 / 2

CSSON  
HSEON  
USBPRE

HSEBYP  
HSIRDY  
HSERDY  
HSION

MCO: 0: No clock  
SW: 0: HSI clock  
SWS: 0: HSI oscillator clock used

**PLL Configuration**

PLLON  
PLLRDY  
PLLSRC  
PLLXTPRE

PLLMUL: 0: PLL Clock \* 2

**Control/Status**

RCC\_CSR: 0x0C000000

LPWRRSTF  
PINRSTF  
WWDGRSTF  
RMVF  
IWDGRSTF  
LSIRDY  
SFTRSTF  
LSION  
PORRSTF

**Backup domain control**

RCC\_BDCR: 0x00000000  
RTCSEL: 0: No clock

BDRST  
RTCEN  
LSEBYP  
LSERDY  
LSEON

**Clock Interrupt**

RCC\_CIR: 0x00000000

CSSC  
CSSIE  
CSSF  
UNLKC  
UNLKIE  
UNLKF  
PLLRDYC  
PLLRDYIE  
PLLRDYF  
HSERDYC  
HSERDYIE  
HSERDYF  
HSIRDYC  
HSIRDYIE  
HSIRDYF  
LSERDYC  
LSERDYIE  
LSERDYF  
LSIRDYC  
LSIRDYIE  
LSIRDYF

**Power Control & Status**

PWR\_CR: 0x00000000  
PWR\_CSR: 0x00000000

PLS: 0: TBD

DBP  
CWUF  
PVDO  
PVDE  
PDDS  
SBF  
CSBF  
LPDS  
WUF

**Core & Memory and Peripheral Clocks**

OSC: 12.000000 MHz  
OCS32: 32.768 kHz  
HSI\_RC: 8.000000 MHz  
LSI\_RC: 32.768 kHz  
SYSCLK: 8.000000 MHz

RTCLK: 32.768 kHz  
MCO: 0.000000 MHz  
IWDGCLK: 32.768 kHz  
USBCLK: 2.666666 MHz  
ADCCLK: 1.000000 MHz

HCLK: 8.000000 MHz  
PCLK1: 4.000000 MHz  
PCLK2: 2.000000 MHz  
TIMXCLK: 8.000000 MHz  
TIM1CLK: 4.000000 MHz

## Lab3

❖ Change the SYSCLK, HCLK, PCLK1, and PCLK2 with different frequencies

➤ Configure Board to run with the following rates:

- APB1 Bus Frequency 16MHz
- APB2 Bus Frequency 8MHz
- AHB Frequency 32MHz
- SYSCLK 32MHz
- Use only internal HIS\_RC

**Power, Reset and Clock Control (PRCC)**

**Clock Control & Configuration**

RCC\_CR: 0x03000083 ☐ CSSON ☐ HSEBYP ☐ HSERDY  
RCC\_CFGR: 0x00182C0A ☐ HSEON ☒ HSIRDY ☒ HSION  
☐ USBPRE  
PPRE1: 4: HCLK / 2 MCO: 0: No clock  
PPRE2: 5: HCLK / 4 SW: 2: PLL clock  
HPRE: 0: SYSCLK SWS: 2: PLL clock used  
ADCPRE: 0: PCLK2 / 2

**PLL Configuration**

☒ PLLON  
☒ PLLRDY  
☐ PLLSRC  
☐ PLLXTPRE  
PLLMUL: 6: PLL Clock \* 8

**Control/Status**

RCC\_CSR: 0x0C000000 ☐ LPWRRSTF ☐ WWDGRSTF ☐ IWDGRSTF ☐ SFRSTF ☒ PORRSTF  
☒ PINRSTF ☐ RMVF ☐ LSIRDY ☐ LSION

**Backup domain control**

RCC\_BDCR: 0x00000000 RTCSEL: 0: No clock  
☐ BDRST ☐ RTCEN ☐ LSEBYP ☐ LSERDY ☐ LSEON

**Clock Interrupt**

RCC\_CIR: 0x00000000  
☐ CSSC ☐ UNLKC ☐ PLLRDYC ☐ HSERDYC ☐ HSIRDYC ☐ LSERDYC ☐ LSIRDYC  
☐ CSSIE ☐ UNLKIE ☐ PLLRDYIE ☐ HSERDYIE ☐ HSIRDYIE ☐ LSERDYIE ☐ LSIRDYIE  
☐ CSSF ☐ UNLKF ☐ PLLRDYF ☐ HSERDYF ☐ HSIRDYF ☐ LSERDYF ☐ LSIRDYF

**Power Control & Status**

PWR\_CR: 0x00000000 PLS: 0: TBD ☐ DBP ☐ PVDE ☐ CSBF  
PWR\_CSR: 0x00000000 ☐ EWUP ☐ CWUF ☐ PDDS ☐ LPDS  
☐ PVDO ☐ SBF ☐ WUF

**Core & Memory and Peripheral Clocks**

OSC: 12.000000 MHz	RTCCLK: 32.768 kHz	HCLK: 32.000000 MHz
OCS32: 32.768 kHz	MCO: 0.000000 MHz	PCLK1: 16.000000 MHz
HSI_RC: 8.000000 MHz	IWDGCLK: 32.768 kHz	PCLK2: 8.000000 MHz
LSI_RC: 32.768 kHz	USBCLK: 21.333333 MHz	TIMXCLK: 32.000000 MHz
SYSCLK: 32.000000 MHz	ADCCLK: 4.000000 MHz	TIM1CLK: 16.000000 MHz