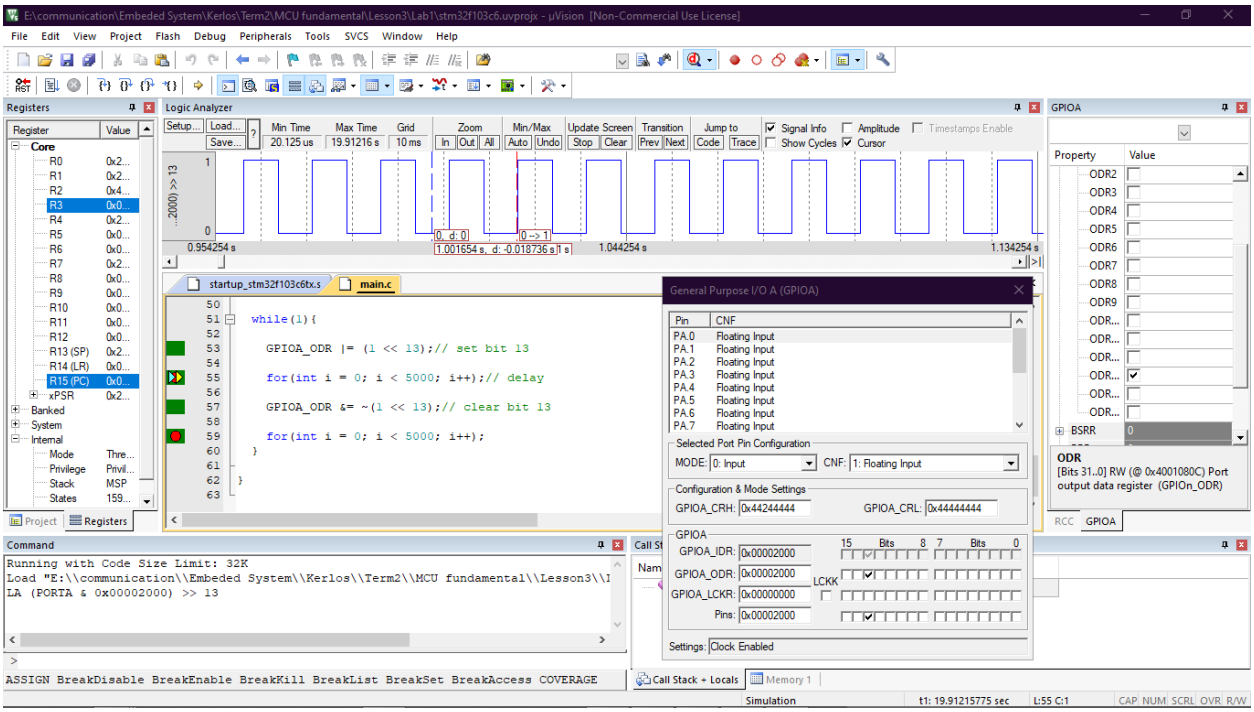
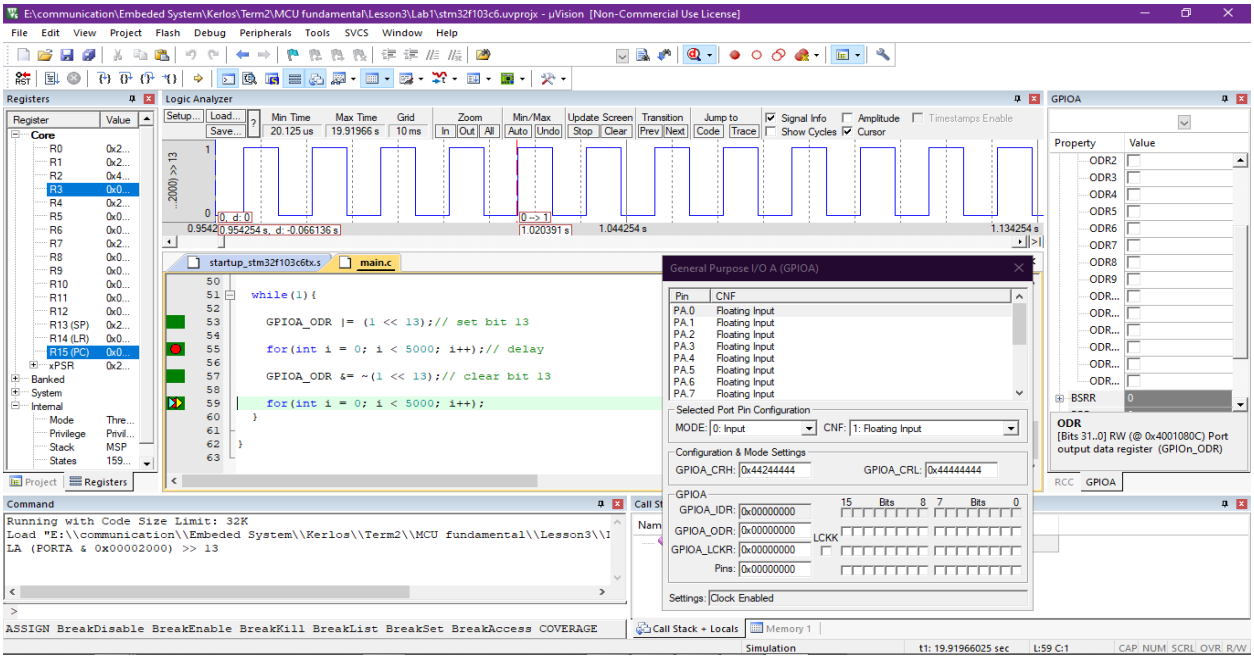
Lab1

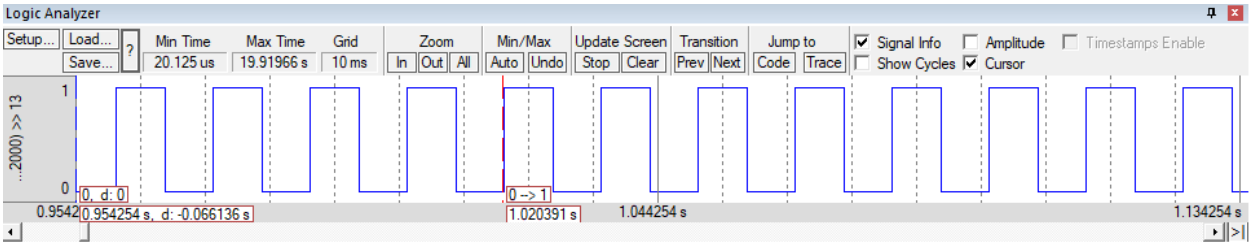
- Practical lab on STM32F103C6 Toggle LED
  - High Pin -> ODR



  - Low Pin -> ODR



➢ Logic Analyzer



➢ MCU Clock (Default: HSI)

Power, Reset and Clock Control (PRCC)

Clock Control & Configuration

RCC_CR: 0x00000083 — CSSON, HSEBYP, HSERDY, HSEON, HSIRDY, HSION, USBPRE

RCC_CFGR: 0x00000000

PPRE1: 0: HCLK — MCO: 0: No clock

PPRE2: 0: HCLK — SW: 0: HSI clock

HPRE: 0: SYSCLK — SWS: 0: HSI oscillator clock used

ADCPRE: 0: PCLK2 / 2

PLL Configuration

PLLON, PLLRDY, PLLSRC, PLLXTPRE

PLLMUL: 0: PLL Clock * 2

Control/Status

RCC_CSR: 0x0C000000 — LPWRRSTF, WWDGRSTF, IWDGRSTF, SFTRSTF, PORRSTF, PINRSTF, RMVF, LSIRDY, LSION

Backup domain control

RCC_BDCR: 0x00000000 — RTCSEL: 0: No clock

BDRST, RTCEN, LSEBYP, LSERDY, LSEON

Clock Interrupt

RCC_CIR: 0x00000000

CSSC, UNLKC, PLLRDYC, HSERDYC, HSIRDYC, LSERDYC, LSIRDYC

CSSIE, UNLKIE, PLLRDYIE, HSERDYIE, HSIRDYIE, LSERDYIE, LSIRDYIE

CSSF, UNLKF, PLLRDYF, HSERDYF, HSIRDYF, LSERDYF, LSIRDYF

Power Control & Status

PWR_CR: 0x00000000 — PLS: 0: TBD

PWR_CSR: 0x00000000

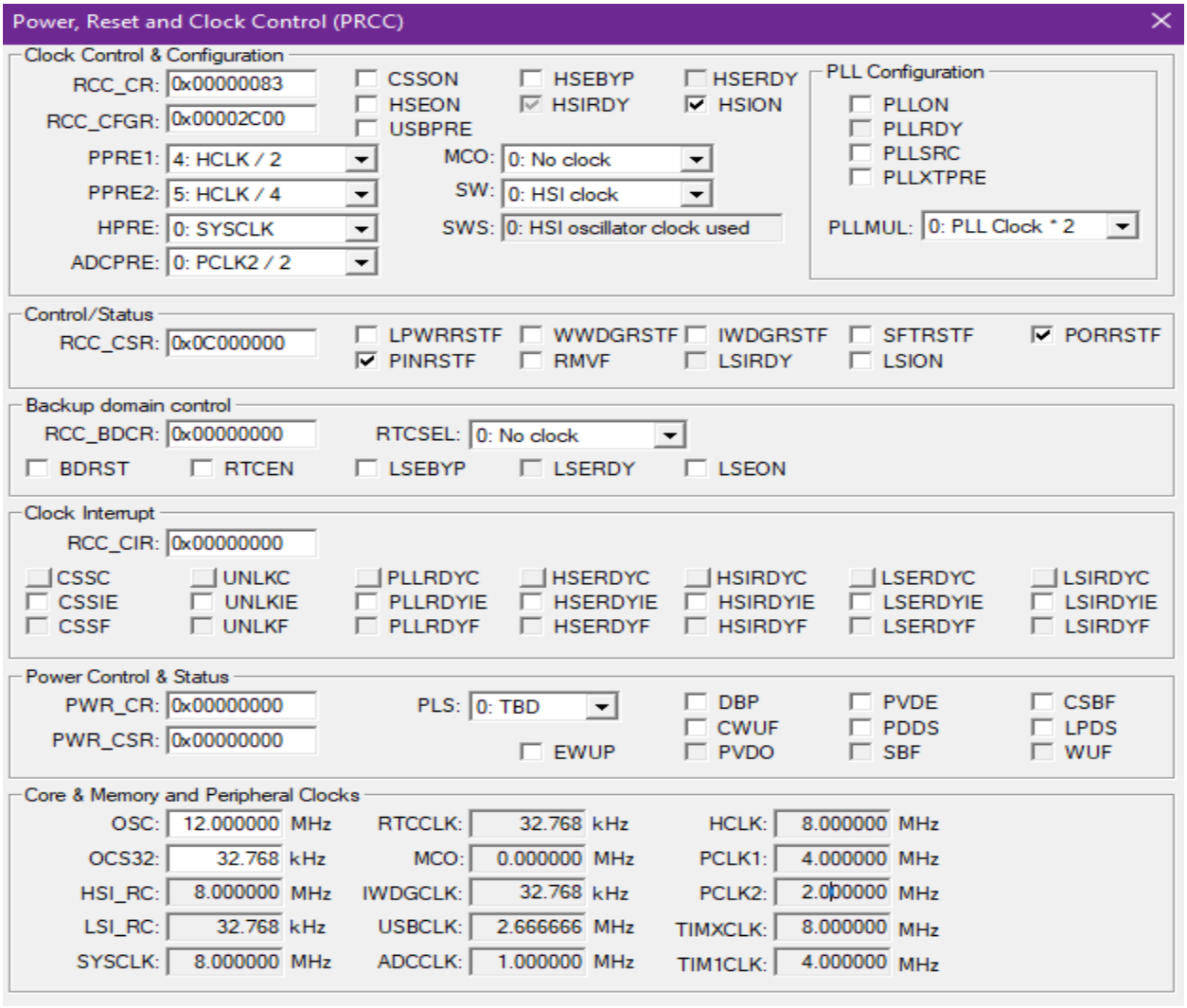
DBP, PVDE, CSBF, CWUF, PDDS, LPDS, EWUP, PVDO, SBF, WUF

Core & Memory and Peripheral Clocks

OSC:	12.000000 MHz	RTCCLK:	32.768 kHz	HCLK:	8.000000 MHz
OCS32:	32.768 kHz	MCO:	0.000000 MHz	PCLK1:	8.000000 MHz
HSI_RC:	8.000000 MHz	IWDGCLK:	32.768 kHz	PCLK2:	8.000000 MHz
LSI_RC:	32.768 kHz	USBCLK:	2.666666 MHz	TIMXCLK:	8.000000 MHz
SYSCLK:	8.000000 MHz	ADCCLK:	4.000000 MHz	TIM1CLK:	8.000000 MHz

Lab2

- Change the SYSCLK, HCLK, PCLK1, and PCLK2 with different frequencies
  - Configure Board to run with the following rates:
    - APB1 Bus Frequency 4MHz
    - APB2 Bus Frequency 2MHz
    - AHB Frequency 8MHz
    - SYSCLK 8MHz
    - Use only internal HIS_RC



Lab3

- Change the SYSCLK, HCLK, PCLK1, and PCLK2 with different frequencies
  - Configure Board to run with the following rates:
    - APB1 Bus Frequency 16MHz
    - APB2 Bus Frequency 8MHz
    - AHB Frequency 32MHz
    - SYSCLK 32MHz
    - Use only internal HIS_RC