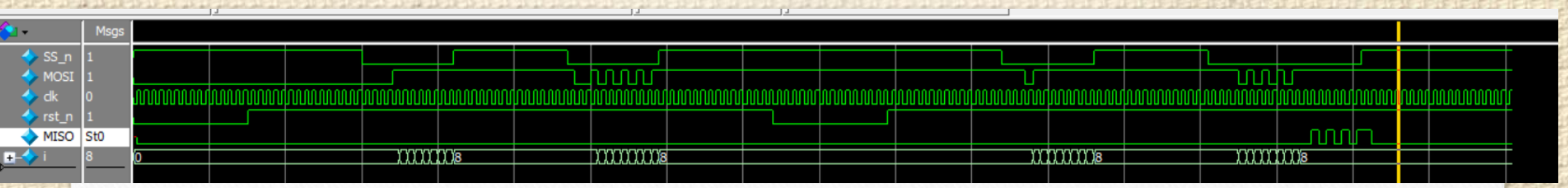
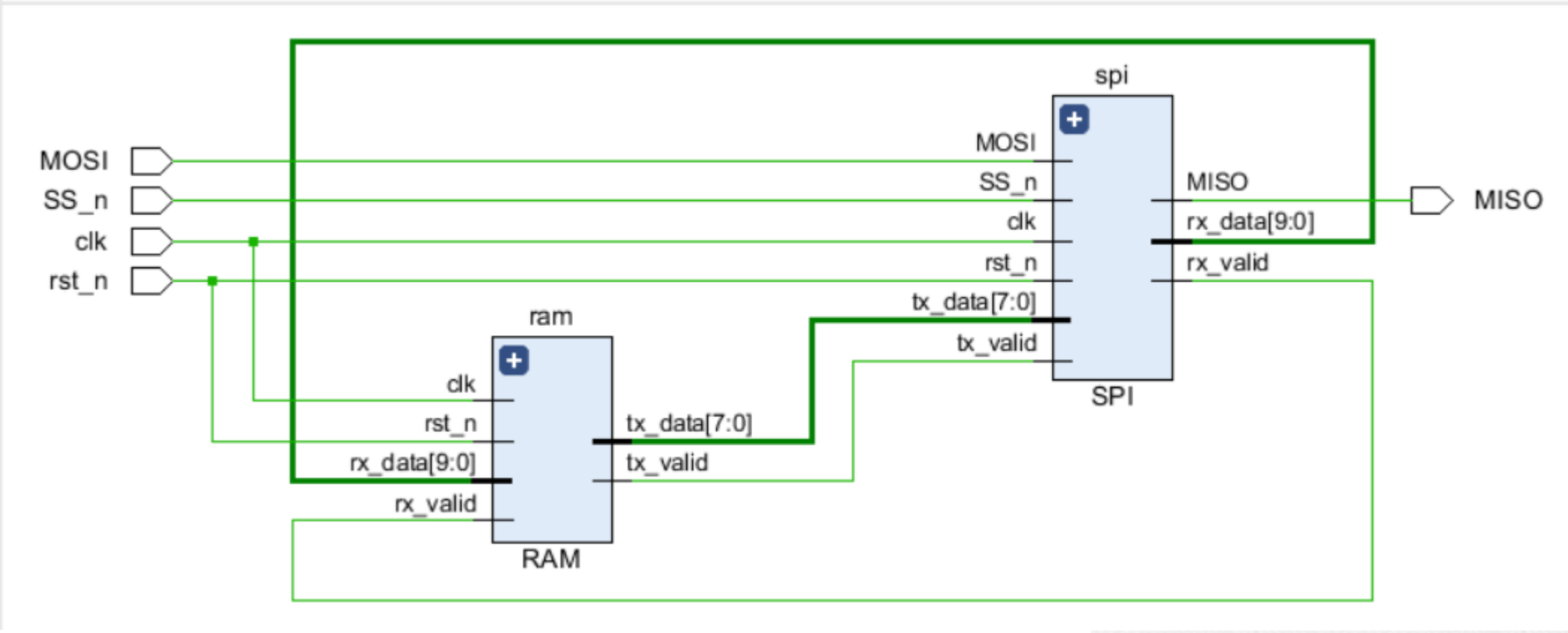
SPI PROJECT

Name : Mohamed Mostafa Mahmoud

WAVE FORM

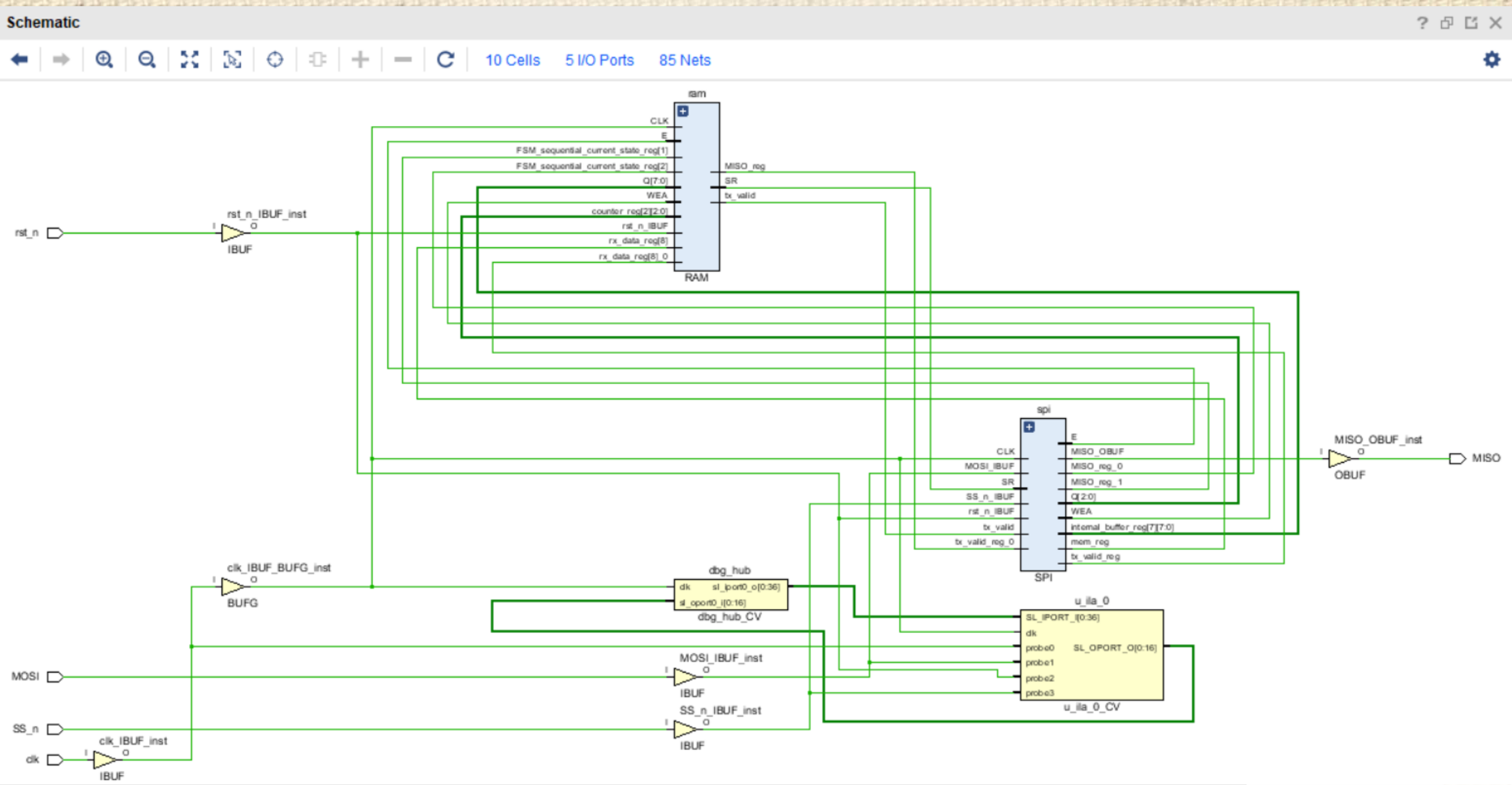


ELABORATION STAGE (ONE HOT ENCODING)



- Elaborated Design (13 infos)
  - General Messages (13 infos)
    - [Synth 8-6157] synthesizing module 'SPI_wrapper' [SPI_wrapper.v:1] (2 more like this)
    - [Synth 8-155] case statement is not full and has no default [SPI.v:20] (1 more like this)
    - [Synth 8-6155] done synthesizing module 'SPI' (1#1) [SPI.v:1] (2 more like this)
    - [Device 21-403] Loading part xc7a35ticpg236-1L
    - [Project 1-570] Preparing netlist for logic optimization

SYNTHESIS STAGE (ONE HOT ENCODING)



Design Timing Summary

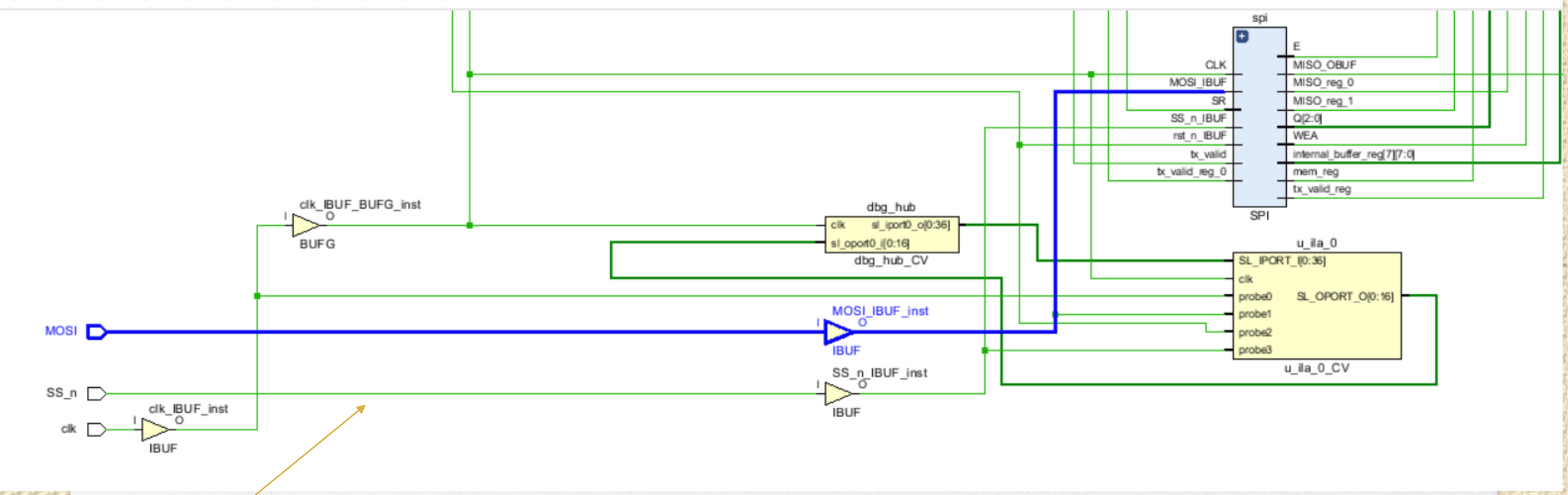
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.682 ns	Worst Hold Slack (WHS):	0.151 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	66	Total Number of Endpoints:	66	Total Number of Endpoints:	32

All user specified timing constraints are met.

- Synthesized Design (9 infos)
  - General Messages (9 infos)
    - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
    - [Timing 38-35] Done setting XDC timing constraints.
    - [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
    - [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

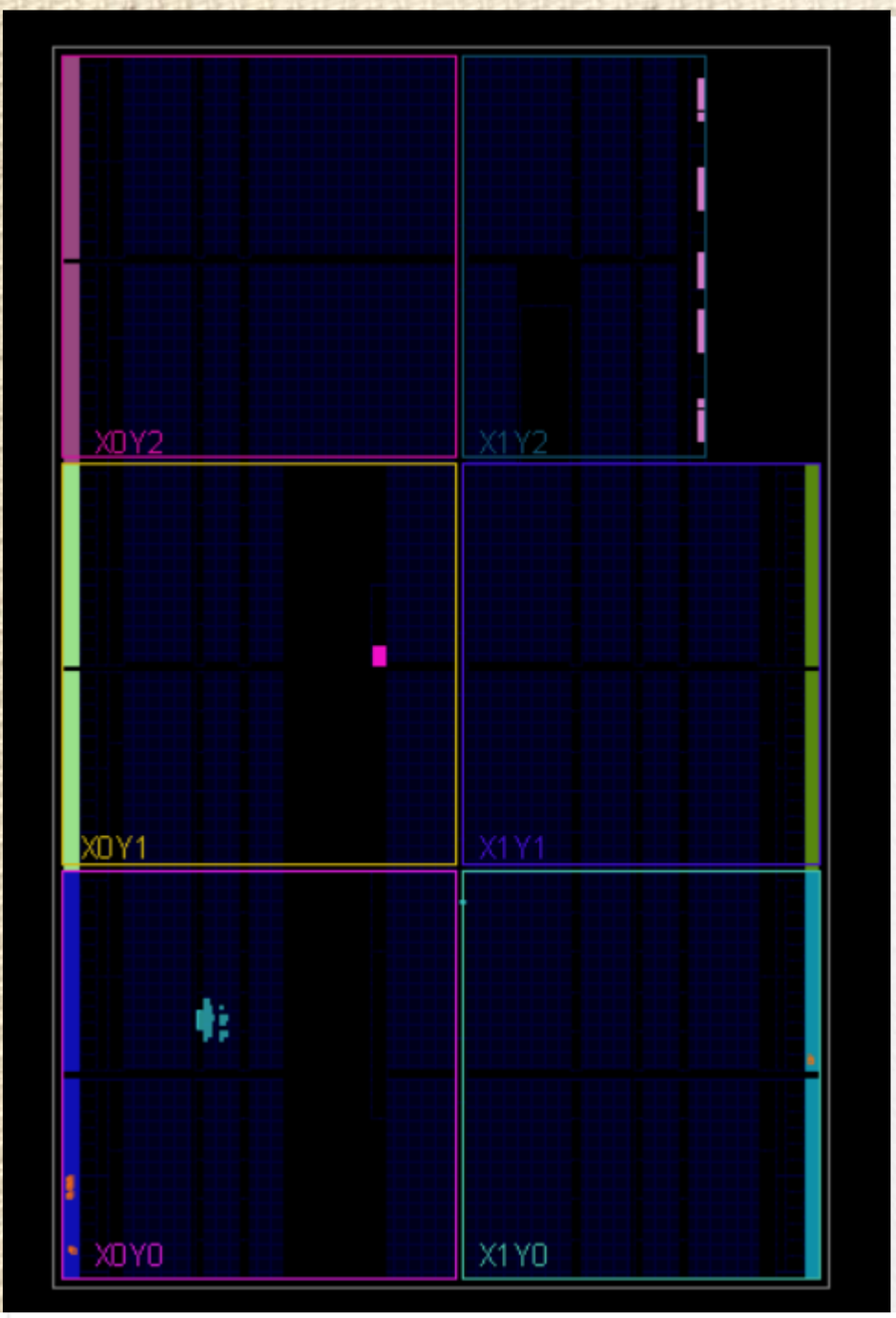
- Synthesis (4 warnings, 33 infos)
  - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
  - [Synth 8-6157] synthesizing module 'SPI_wrapper' [SPI_wrapper.v:1] (2 more like this)
  - [Synth 8-155] case statement is not full and has no default [SPI.v:20] (1 more like this)
  - [Synth 8-6155] done synthesizing module 'SPI' (1#1) [SPI.v:1] (2 more like this)
  - [Device 21-403] Loading part xc7a35ticpg236-1L
  - [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/digital_design_diploma/projects/SPI/basys_master.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/SPI_wrapper_propImpl.xdc].
    Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
  - [Synth 8-802] inferred FSM for state register 'current_state_reg' in module 'SPI'
  - [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (4) smaller than threshold (5) (5 more like this)
  - [Synth 8-327] inferring latch for variable 'FSM_sequential_next_state_reg' [SPI.v:22] (2 more like this)
  - [Synth 8-3354] encoded FSM with state register 'current_state_reg' using encoding 'sequential' in module 'SPI'
  - [Synth 8-4480] The timing for the instance i_0/ram/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
  - [Project 1-571] Translating synthesized netlist
  - [Netlist 29-17] Analyzing 8 Unisim elements for replacement
  - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  - [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  - [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed. (1 more like this)
  - [Common 17-83] Releasing license: Synthesis
  - [Constraints 18-5210] No constraint will be written out.
  - [Common 17-1381] The checkpoint 'D:/digital_design_diploma/projects/SPI/project_SPI_final/project_SPI_final.runs/synth_1/SPI_wrapper.dcp' has been generated.
  - [runtcl-4] Executing : report_utilization -file SPI_wrapper_utilization_synth.rpt -pb SPI_wrapper_utilization_synth.pb
  - [Common 17-206] Exiting Vivado at Tue Mar 12 03:15:31 2024...

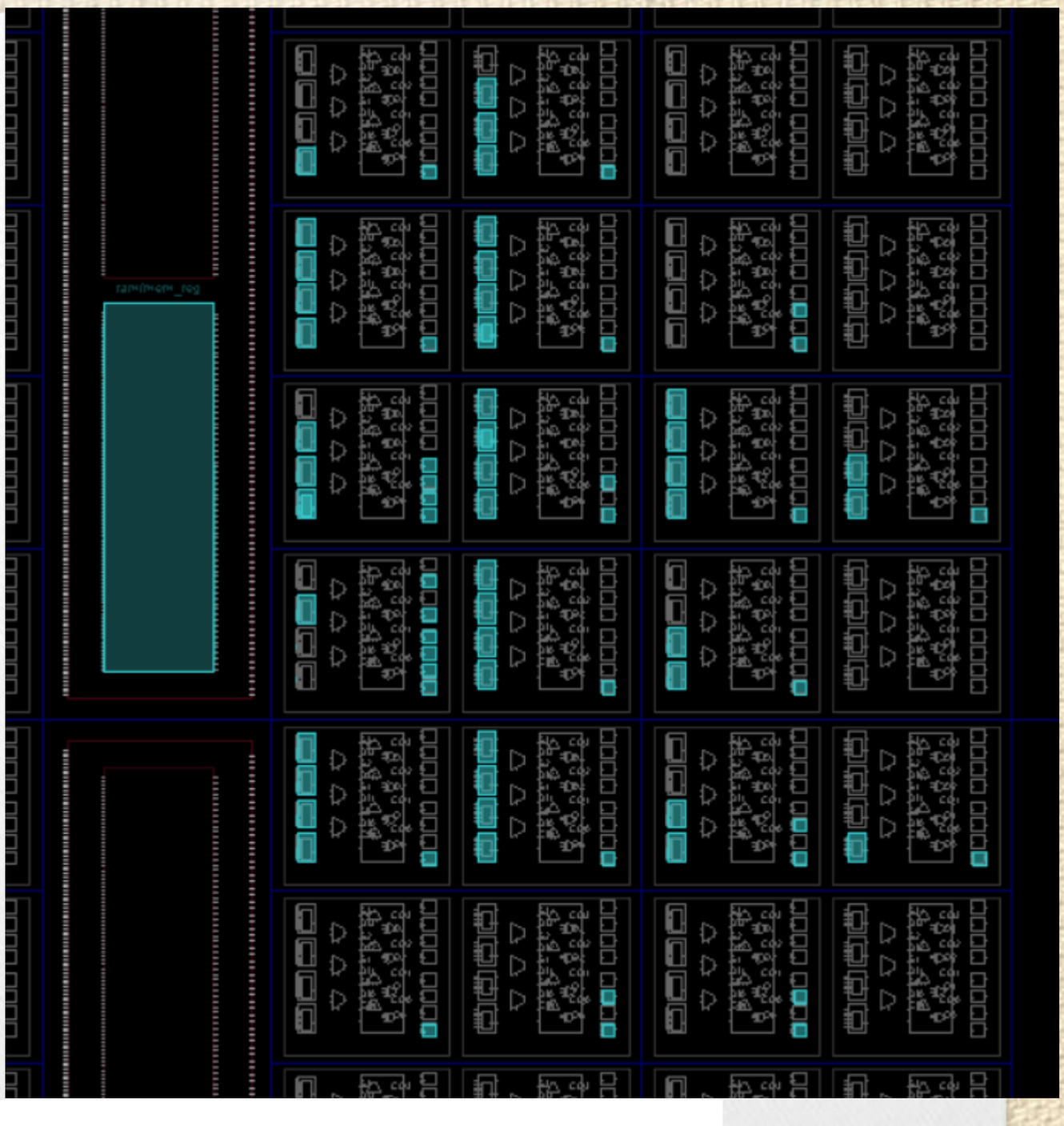
Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_wrapper	42	32	0.5	5	1
dbg_hub (dbg_hub_CV)	0	0	0	0	0
ram (RAM)	4	9	0.5	0	0
spi (SPI)	38	23	0	0	0
u_ila_0 (u_ila_0_CV)	0	0	0	0	0



CRITICAL PATH

IMPLEMENTION STAGE (ONE HOT ENCODING)





Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.066 ns	Worst Hold Slack (WHS):	0.084 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	67	Total Number of Endpoints:	67	Total Number of Endpoints:	32

All user specified timing constraints are met.

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_wrapper	43	32	19	43	5	0.5	5	1
ram (RAM)	5	9	7	5	0	0.5	0	0
spi (SPI)	38	23	18	38	4	0	0	0

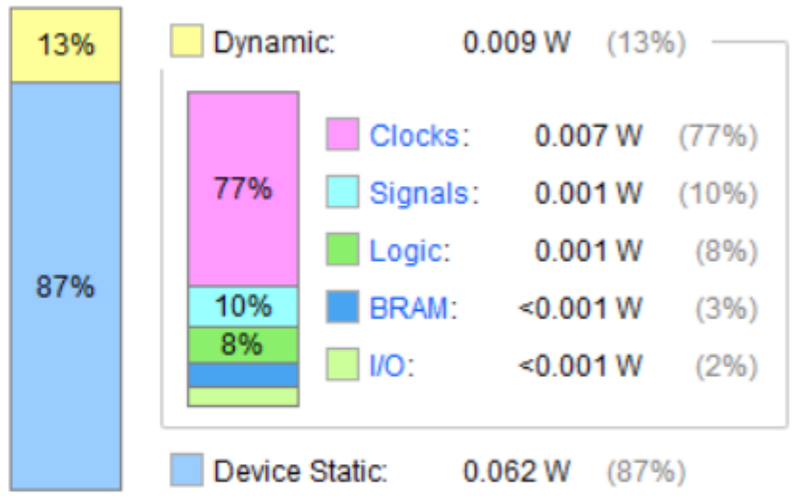
Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

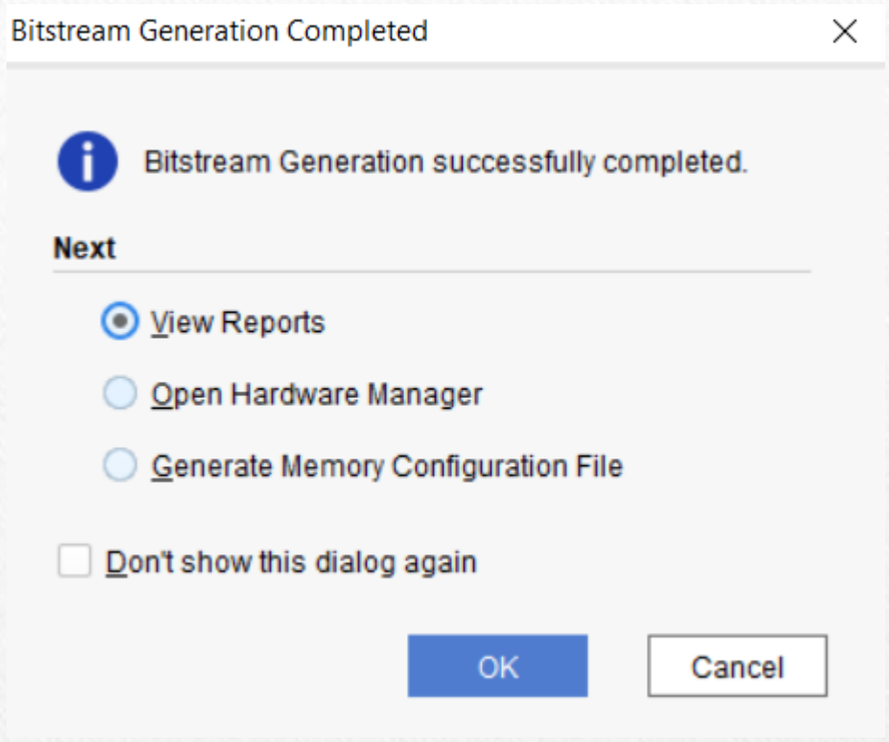
Total On-Chip Power:	**0.071 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.4°C**
Thermal Margin:	74.6°C (14.8 W)
Effective ϑJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

Launch Power Constraint Advisor to find and fix invalid switching activity

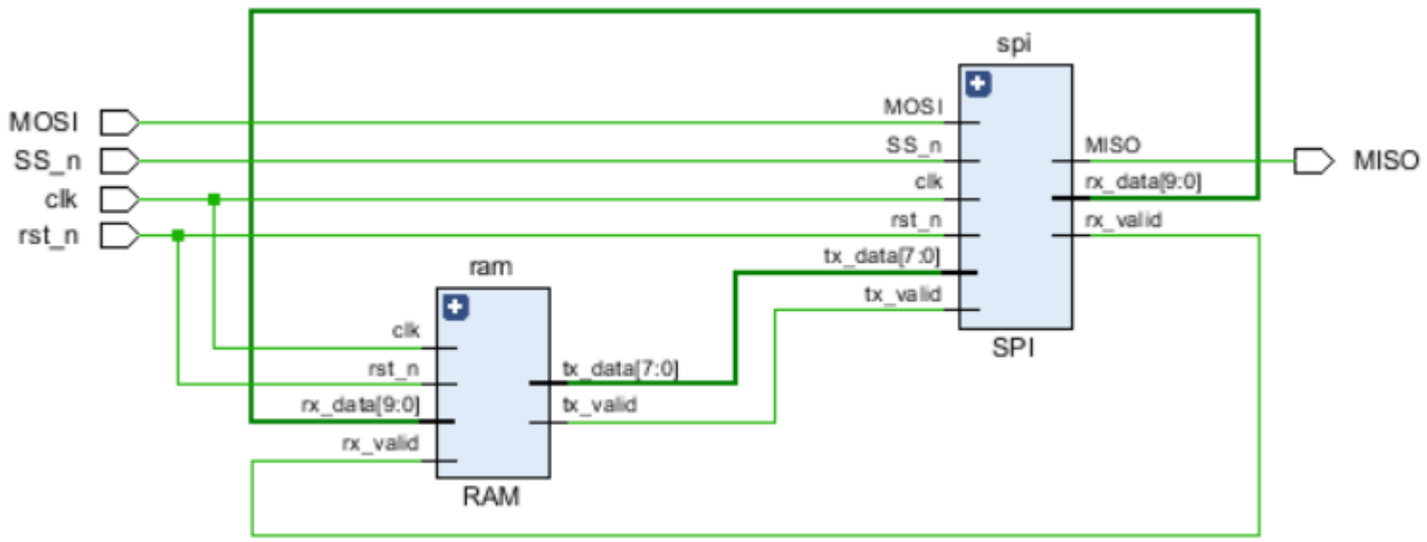
On-Chip Power



- Implementation (1 warning, 109 infos, 240 status messages)
  - Design Initialization (11 infos, 7 status messages)
    - Command: open_checkpoint D:/digital_design_diploma/projects/SPI/SPI_PROJECT/SPI_PROJECT.runs/impl_1/SPI_wrapper.dcp (6 more like this)
    - [Netlist 29-17] Analyzing 4 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Device 21-403] Loading part xc7a35ticpg236-1L
    - [Project 1-570] Preparing netlist for logic optimization
    - [Timing 38-478] Restoring timing data from binary archive.
    - [Timing 38-479] Binary timing data restore complete.
    - [Project 1-856] Restoring constraints from binary archive.
    - [Project 1-853] Binary constraint restore complete.
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
    - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  - Opt Design (36 infos, 54 status messages)
    - Command: opt_design (53 more like this)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
    - [Project 1-461] DRC finished with 0 Errors
    - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
    - [Chipscope 16-329] Generating Script for core instance : dbg_hub (1 more like this)
    - [IP_Flow 19-3806] Processing IP xilinx.com:ip:xsdbm:3.0 for cell dbg_hub_CV. (1 more like this)
    - [Chipscope 16-220] Re-using generated and synthesized IP, "xilinx.com:ip:xsdbm:3.0", from Vivado IP cache entry "9a650ad267bdd151". (1 more like this)
    - [Opt 31-49] Retargeted 0 cell(s).


Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel

ELABORATION STAGE (GRAY ENCODING)

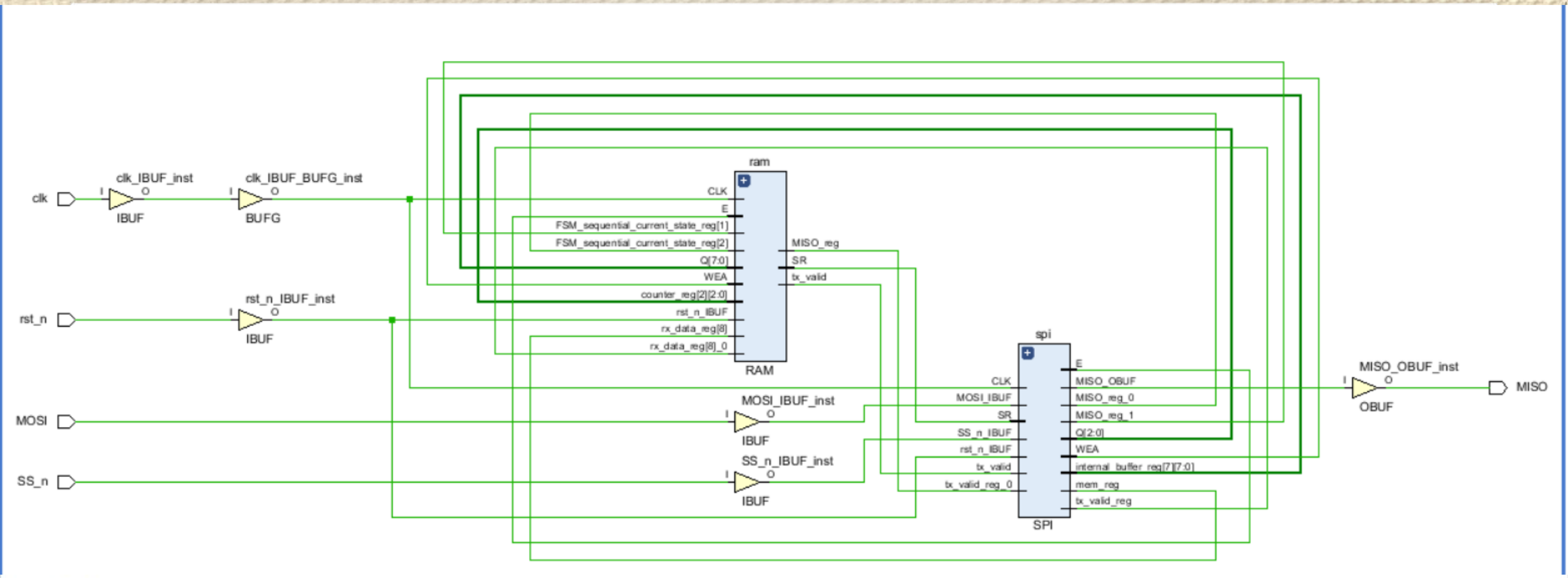


Elaborated Design (11 infos)

General Messages (11 infos)

- [Synth 8-6157] synthesizing module 'SPI_wrapper' [SPI_wrapper.v:1] (2 more like this)
- [Synth 8-155] case statement is not full and has no default [SPI.v:20] (1 more like this)
- [Synth 8-6155] done synthesizing module 'SPI' (1#1) [SPI.v:1] (2 more like this)
- [Project 1-570] Preparing netlist for logic optimization
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed.

SYNTHESIS STAGE (GRAY ENCODING)



Synthesis (4 warnings, 33 infos)

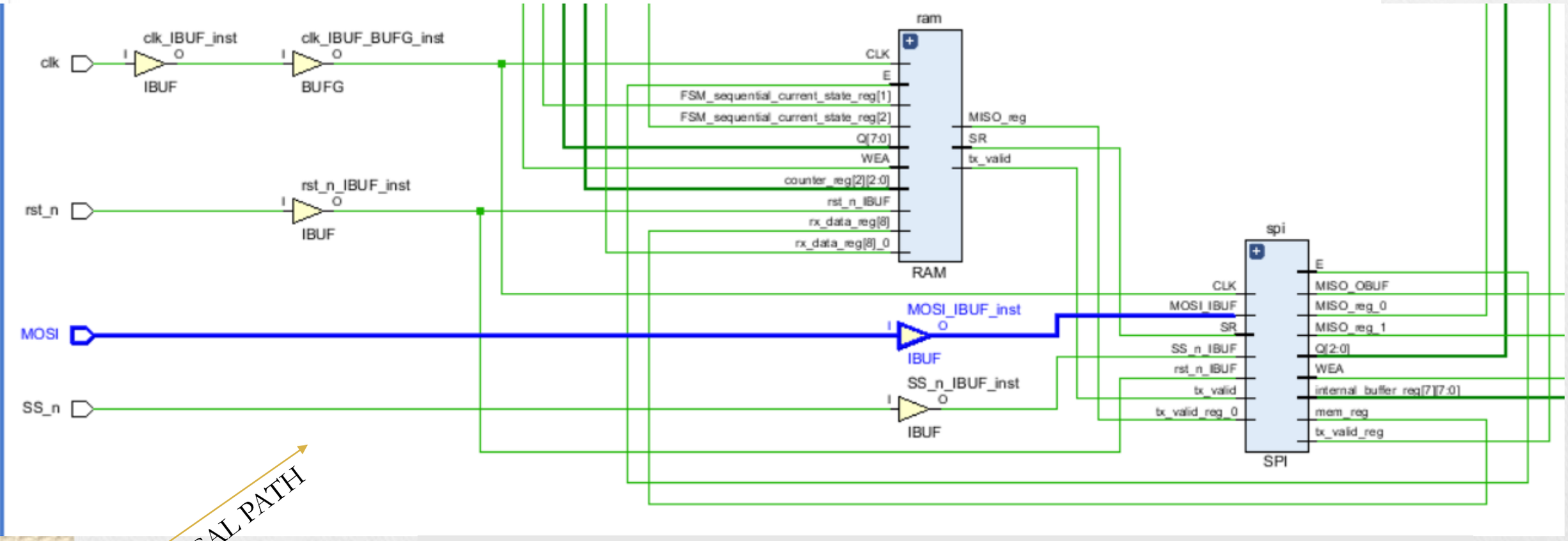
- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
- [Synth 8-6157] synthesizing module 'SPI_wrapper' [SPI_wrapper.v:1] (2 more like this)
- [Synth 8-155] case statement is not full and has no default [SPI.v:20] (1 more like this)
- [Synth 8-6155] done synthesizing module 'SPI' (1#1) [SPI.v:1] (2 more like this)
- [Device 21-403] Loading part xc7a35ticpg236-1L
- [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/digital_design_diploma/projects/SPI/basys_master - gray.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/SPI_wrapper_propImpl.xdc].
  Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- [Synth 8-802] inferred FSM for state register 'current_state_reg' in module 'SPI'
- [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (4) smaller than threshold (5) (5 more like this)
- [Synth 8-327] inferring latch for variable 'FSM_sequential_next_state_reg' [SPI.v:22] (2 more like this)
- [Synth 8-3354] encoded FSM with state register 'current_state_reg' using encoding 'sequential' in module 'SPI'
- [Synth 8-4480] The timing for the instance i_0/ram/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 8 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'D:/digital_design_diploma/projects/SPI/project_4/project_4.runs/synth_1/SPI_wrapper.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file SPI_wrapper_utilization_synth.rpt -pb SPI_wrapper_utilization_synth.pb

- Synthesized Design (6 infos)
  - General Messages (6 infos)
    - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.682 ns	Worst Hold Slack (WHS):	0.151 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	66	Total Number of Endpoints:	66	Total Number of Endpoints:	32

All user specified timing constraints are met.

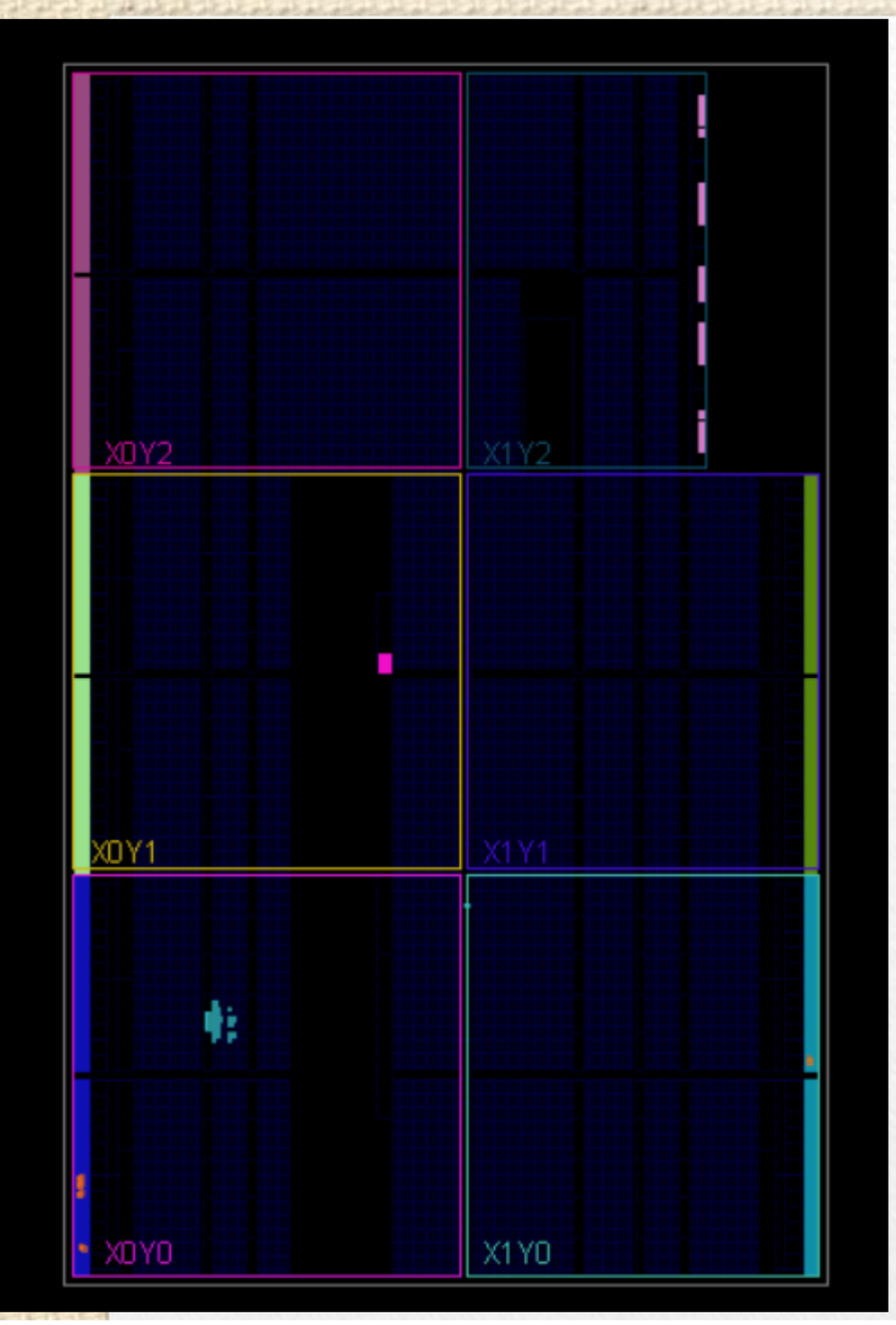


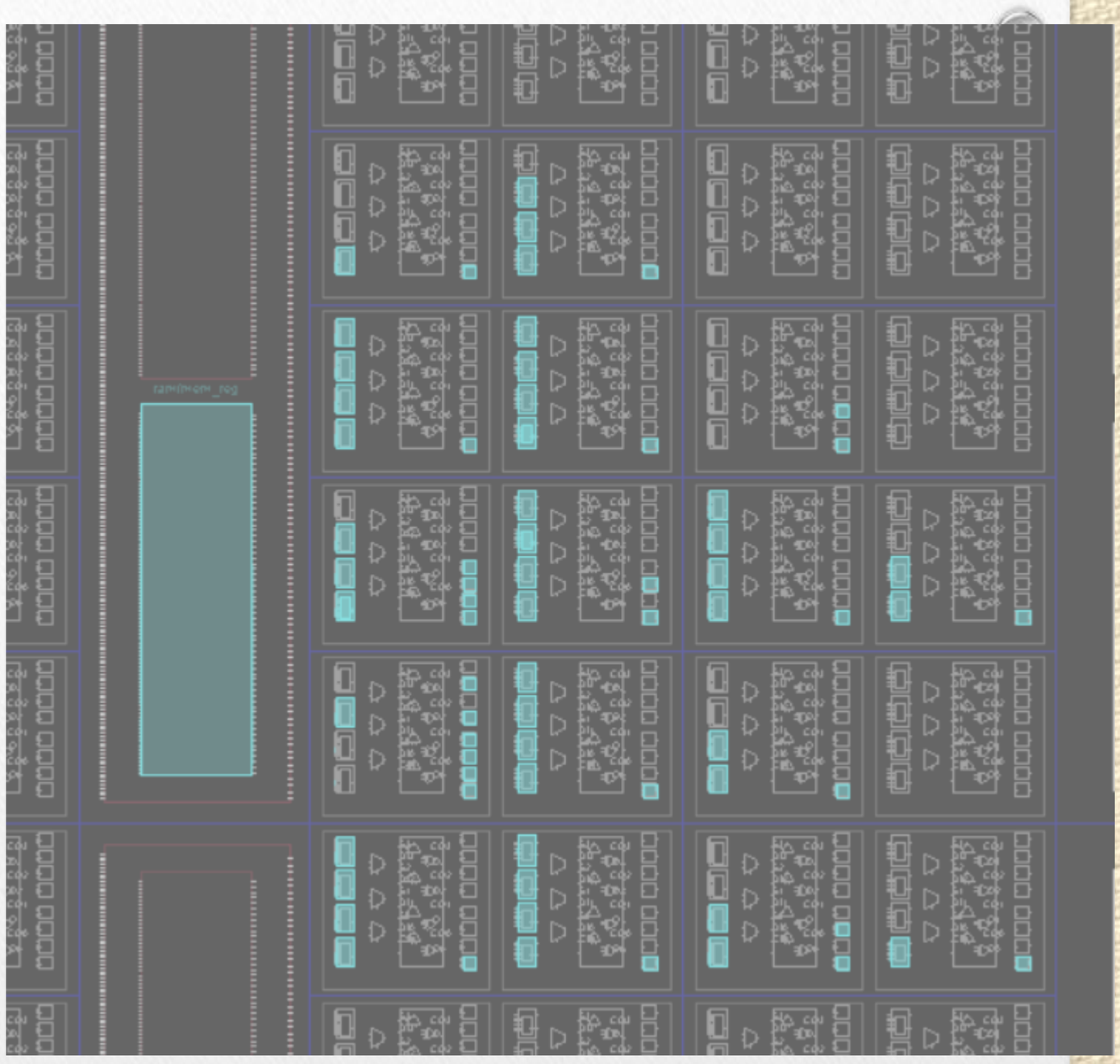
CRITICAL PATH

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_wrapper	42	32	0.5	5	1
ram (RAM)	4	9	0.5	0	0
spi (SPI)	38	23	0	0	0

IMPLEMENTION STAGE (GRAY ENCODING)





Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.066 ns	Worst Hold Slack (WHS):	0.084 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	67	Total Number of Endpoints:	67	Total Number of Endpoints:	32

All user specified timing constraints are met.

Hierarchy

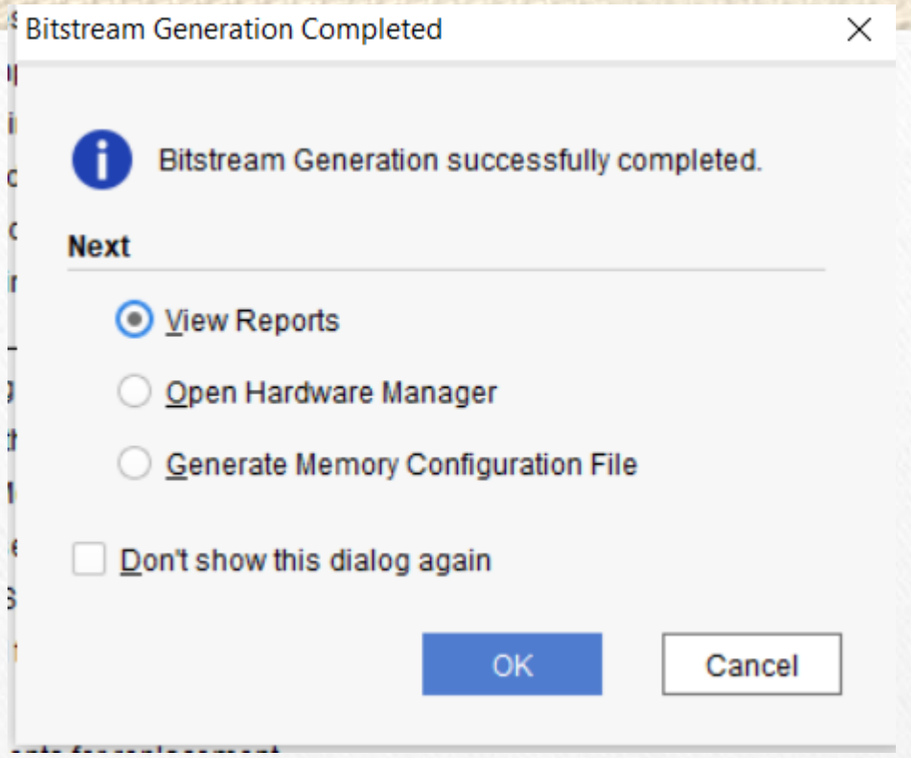
Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_wrapper	43	32	19	43	5	0.5	5	1
ram (RAM)	5	9	7	5	0	0.5	0	0
spi (SPI)	38	23	18	38	4	0	0	0

Design Initialization (11 infos)

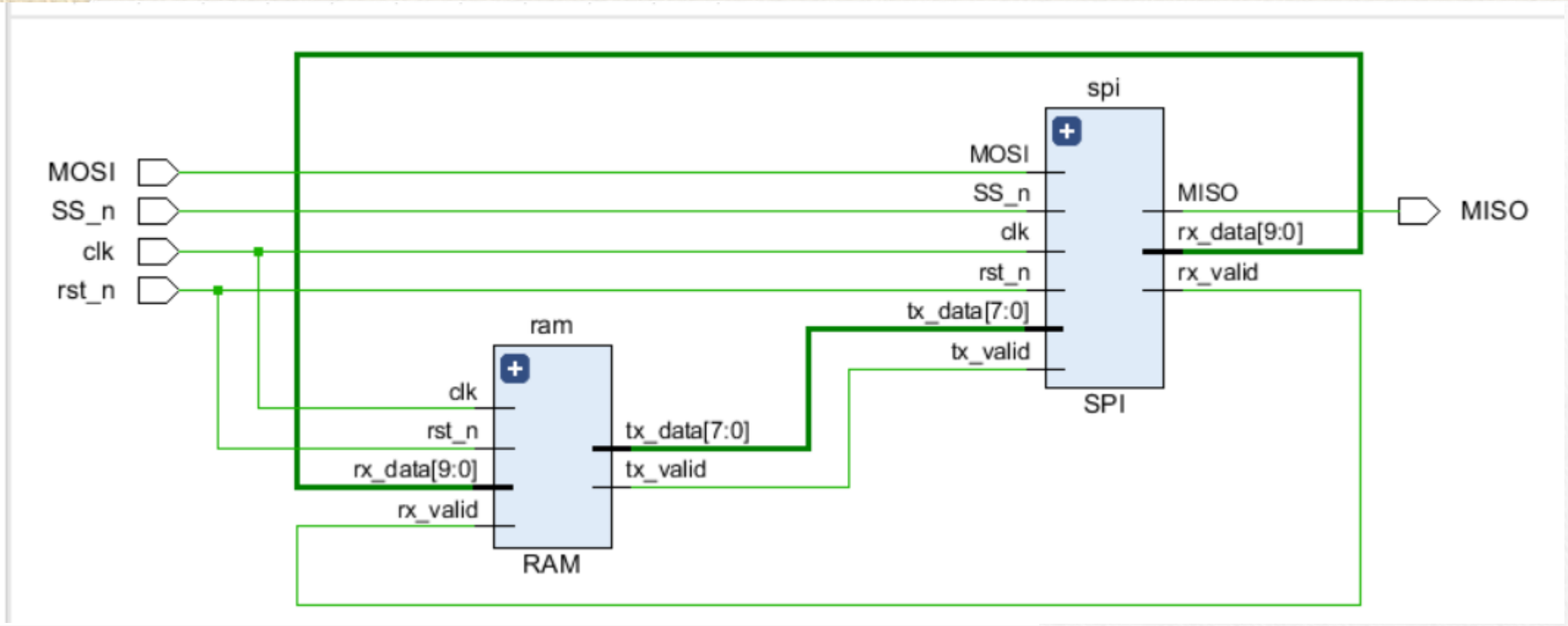
- [Netlist 29-17] Analyzing 5 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Device 21-403] Loading part xc7a35ticpg236-1L
- [Project 1-570] Preparing netlist for logic optimization
- [Timing 38-478] Restoring timing data from binary archive.
- [Timing 38-479] Binary timing data restore complete.
- [Project 1-856] Restoring constraints from binary archive.
- [Project 1-853] Binary constraint restore complete.
- [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed.
- [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

Opt Design (30 infos)

- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
- [Project 1-461] DRC finished with 0 Errors
- [Project 1-462] Please refer to the DRC report (report_drc) for more information.
- [Opt 31-49] Retargeted 0 cell(s).
- [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)
- [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
- [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
- [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
- [Pwropt 34-9] Applying IDT optimizations ...
- [Pwropt 34-10] Applying ODC optimizations ...
- [Physopt 32-619] Estimated Timing Summary | WNS=5.682 | TNS=0.000 |
- [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 1 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.
- [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports
- [Timing 38-35] Done setting XDC timing constraints. (1 more like this)

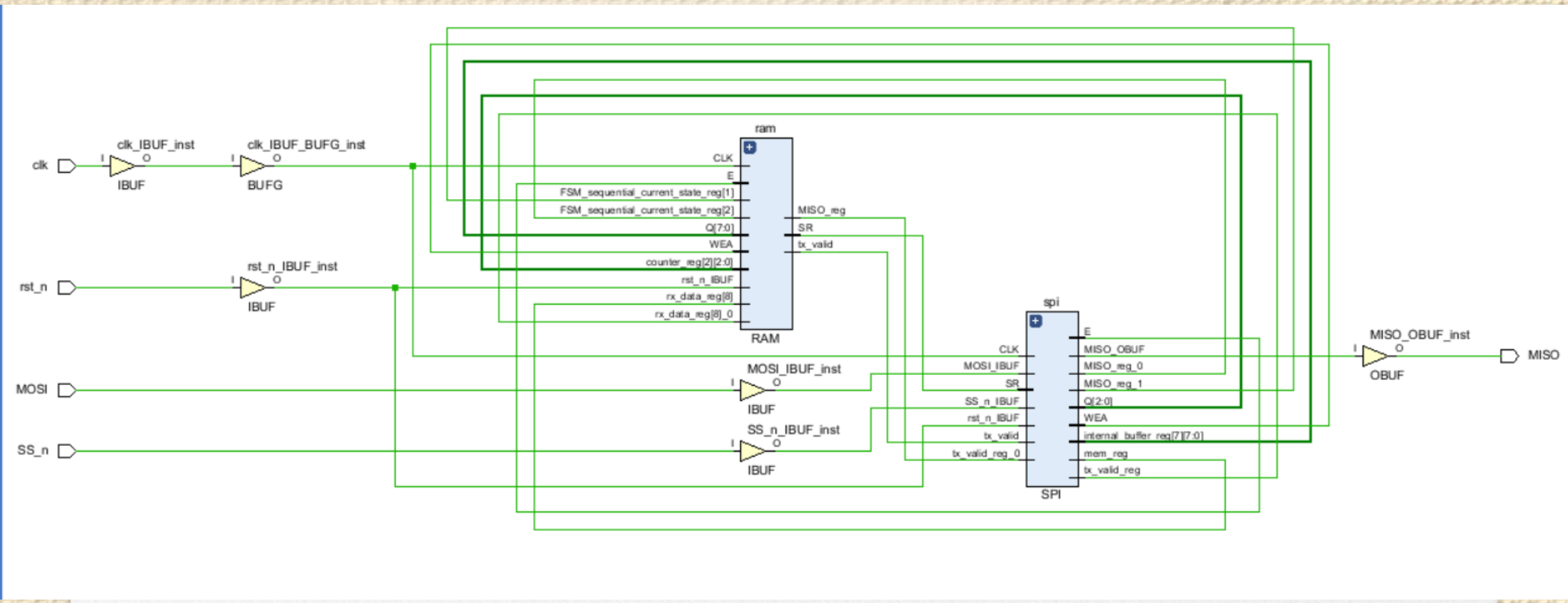

Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
View Reports
Open Hardware Manager
Generate Memory Configuration File
Don't show this dialog again
OK
Cancel

ELABORATION STAGE (SEQ ENCODING)



- Elaborated Design (11 infos)
  - General Messages (11 infos)
    - [Synth 8-6157] synthesizing module 'SPI_wrapper' [SPI_wrapper.v:1] (2 more like this)
    - [Synth 8-155] case statement is not full and has no default [SPI.v:20] (1 more like this)
    - [Synth 8-6155] done synthesizing module 'SPI' (1#1) [SPI.v:1] (2 more like this)
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.

SYNTHESIS STAGE (SEQ ENCODING)



Design Timing Summary

Setup

Worst Negative Slack (WNS):	5.682 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	66

Hold

Worst Hold Slack (WHS):	0.151 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	66

Pulse Width

Worst Pulse Width Slack (WPWS):	4.500 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	32

All user specified timing constraints are met.

Hierarchy

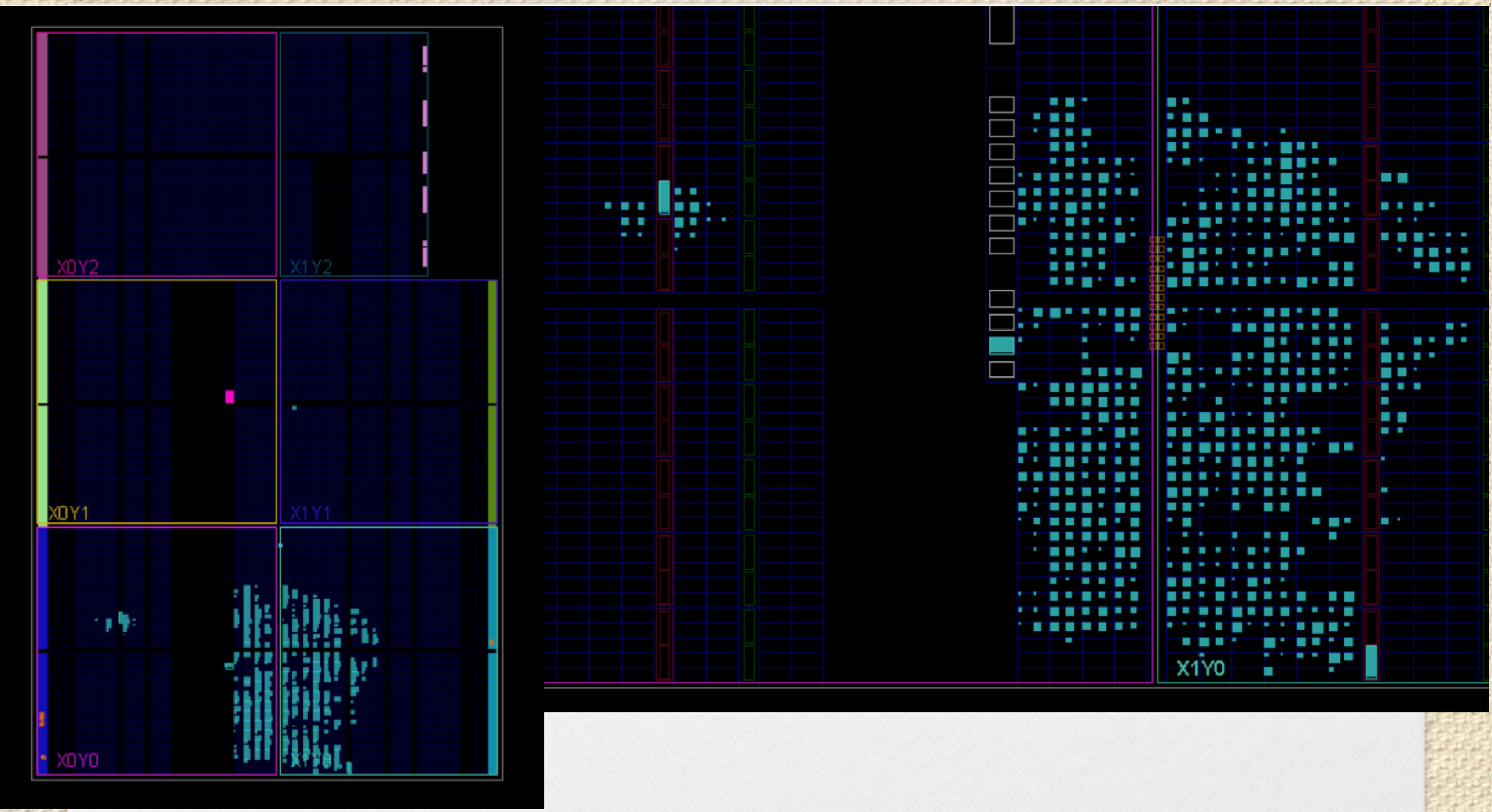
Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_wrapper	42	32	0.5	5	1
ram (RAM)	4	9	0.5	0	0
spi (SPI)	38	23	0	0	0

Synthesis (4 warnings, 33 infos)

- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
- [Synth 8-6157] synthesizing module 'SPI_wrapper' [SPI_wrapper.v:1] (2 more like this)
- [Synth 8-155] case statement is not full and has no default [SPI.v:20] (1 more like this)
- [Synth 8-6155] done synthesizing module 'SPI' (1#1) [SPI.v:1] (2 more like this)
- [Device 21-403] Loading part xc7a35ticpg236-1L
- [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/digital_design_diploma/projects/SPI/basys_master - seq.xdc]. These constraints w
  be used in implementation. Impacted constraints are listed in the file [.Xil/SPI_wrapper_propImpl.xdc].
  Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Pr
  elaboration/synthesis.
- [Synth 8-802] inferred FSM for state register 'current_state_reg' in module 'SPI'
- [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (4) smaller than threshold (5) (5 more like this)
- [Synth 8-327] inferring latch for variable 'FSM_sequential_next_state_reg' [SPI.v:22] (2 more like this)
- [Synth 8-3354] encoded FSM with state register 'current_state_reg' using encoding 'sequential' in module 'SPI'
- [Synth 8-4480] The timing for the instance i_0/ram/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ra
  register may help in improving timing. (1 more like this)
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 8 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'D:/digital_design_diploma/projects/SPI/project_seq_coding/project_seq_coding.runs/synth_1/SPI_wrapper.dcp' has been generated.

- Synthesized Design (9 infos)
  - General Messages (9 infos)
    - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
    - [Timing 38-35] Done setting XDC timing constraints.
    - [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.
    - [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

IMPLEMENTION STAGE (SEQ ENCODING)



- Implementation (1 warning, 105 infos)
  - Design Initialization (7 infos)
    - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Device 21-403] Loading part xc7a35ticpg236-1L
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
  - Opt Design (37 infos)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
    - [Project 1-461] DRC finished with 0 Errors
    - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
    - [Chipscope 16-329] Generating Script for core instance : dbg_hub (1 more like this)
    - [IP_Flow 19-3806] Processing IP xilinx.com:ip:xsdbm:3.0 for cell dbg_hub_CV. (1 more like this)
    - [Chipscope 16-220] Re-using generated and synthesized IP, "xilinx.com:ip:xsdbm:3.0", from Vivado IP cache entry "9a650ad267bdd151". (1 more like this)
    - [Opt 31-49] Retargeted 0 cell(s).
    - [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)
    - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
    - [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
- Place Design (24 infos)
  - [Chipscope 16-240] Debug cores have already been implemented
  - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
  - [DRC 23-27] Running DRC with 2 threads (1 more like this)
  - [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
  - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
  - [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
  - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
  - [Physopt 32-65] No nets found for high-fanout optimization.
  - [Physopt 32-232] Optimized 0 net. Created 0 new instance.
  - [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
  - [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
  - [Place 30-746] Post Placement Timing Summary WNS=4.827. For the most accurate timing information please run report_timing.
  - [Common 17-83] Releasing license: Implementation
  - [Timing 38-480] Writing timing data to binary archive.
  - [Common 17-1381] The checkpoint 'D:/digital_design_diploma/projects/SPI/project_seq_coding/project_seq_coding.runs/impl_1/SPI_wrapper_placed.dcp' has been generated.

Design Timing Summary

Setup

Worst Negative Slack (WNS):	2.548 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	3756

Hold

Worst Hold Slack (WHS):	0.034 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	3740

Pulse Width

Worst Pulse Width Slack (WPWS):	3.750 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	2068

All user specified timing constraints are met.

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
SPI_wrapper	1232	1894	8	616	1129	103	697	1	5	2	1
dbg_hub (dbg_hub)	476	727	0	244	452	24	304	0	0	1	1
ram (RAM)	4	9	0	5	4	0	0	0.5	0	0	0
spi (SPI)	38	23	0	17	38	0	5	0	0	0	0
u_ila_0 (u_ila_0)	714	1135	8	362	635	79	386	0.5	0	0	0

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

- View Reports
- Open Hardware Manager
- Generate Memory Configuration File

Don't show this dialog again

OK Cancel

THANK YOU