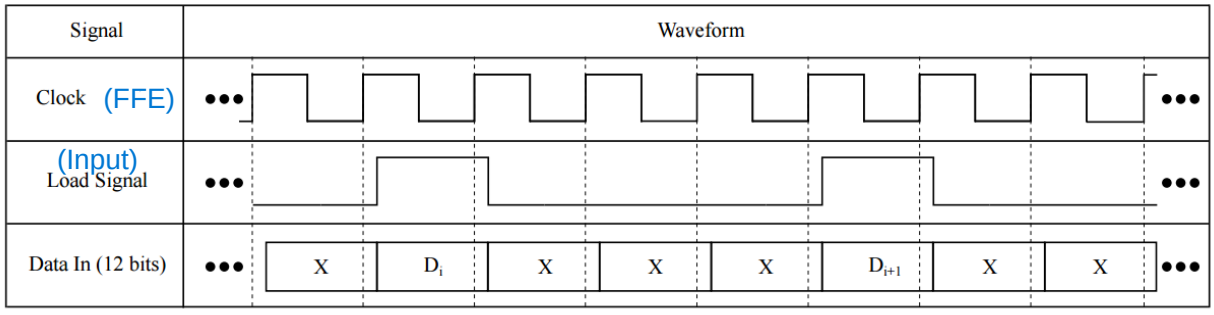
FFE EQUALIZER

- In this project we need to have more practice on practical usage of VHDL or Verilog and all topics which are covered through the course.
- You are supposed to implement 4 taps FFE equalizer using VHDL or Verilog and go through the digital flow in any tool which you want.
- First you need to read the following slide to know what is the FFE and what is its usage (https://people.engr.tamu.edu/spalermo/ecen689/lecture8_ee720_rx_adaptive_eq.pdf) you will find its name RX FIR in the last slides .
  After reading the slides, u should understand the following topics (not in deep)
  - Why we need equalization
  - What is the FFE
  - Equation of FFE

- **For our project**:

The FIR filter taps values (hi) are given as follows: h_0 = 0.5, h_1 = −0.25, h_2 = 0.15625, h_3 = −0.0625. The input data (D_i) is signed and 12-bit wide, and its range is given as follows: $D_i \in (-2^{11}, 2^{11})$. The output data ($Y_i$) has the following relation with input data and the FIR filter taps: $\boldsymbol{Y_i = \sum_{j=0}^{j=3} h_j D_{i-j}}$

- **Note that the input date frequency is 4MHz and the FFE clock is 1MHz!**
- here is a timing diagram for the system:



- **You are supposed to get an output data of 12's signed bit width.**

- **Constrains:**
  - Assume that you will have only **one multiplier and one adder** so you need to use time sharing.
    - ❖ If any one use more than one adder of multiplier will lose marks.

- **General notes:**
  - Try to Keep all signals width to be 12bit so that your code will be simple
  - Every 4 clock cycles of the FFE you are supposed to take only 4 inputs and then any input is don't care
  - After 4 cycles of the FFE, the output should be available
  - Try to think how to store the input data although it is coming from different clock domain

- **Submission:**
  - Every team need to submit the following
    - Paper hardware design for the FFE block
    - pseudo code for this design
    - VERILOG or VHDL code to implement this design (**bonus**)
  - The submission will be at the google class room
  - You can work in teams of 4-6 students, for any exceptions please ask Dr/Karim Osama or Eng/Mahmoud Yehia.
  - Project due date is until 30/5/2023.

Grading:

  - a meeting will be scheduled to discuss every team work.