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| Course Code: | ELC 4801 | Course Title: | Project (1) |

Cairo University

Faculty of Engineering

Electronics and Communications Engineering Department – 4th Year

Sponsored by Si-Vision

**Graduation Project:  
Digital Verification of OpenHMC Controller IP**

*Submitted to: Dr. Ibrahim Qamar*

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# Abstract

In our project, we start by creating a verification plan after reading the documentations of the design and list all its features and functionality. Perform functional verification by using self-checking testbenches for all different scenarios then report the coverage. The Universal Verification Methodology (UVM) is a standardized methodology for verifying integrated circuit designs. It’s derived mainly from the Open Verification Methodology (OVM). We will build a UVM testing environment architecture using SystemVerilog HVL language going through development and debugging phases till we achieve complete coverage. Hence our project is implementing a UVM environment of the OpenHMC (Hybrid Memory Cube) Controller.

# Project Phases

1. Learning required skills
2. Studying the design
3. Building the UVM test environment
4. Collecting Coverage
5. Write Thesis
6. Final Presentation

During the first semester we only covered half of the learning phase.

# Learning Phase

Before starting working on the project, we have to learn the skills needed first. Which are

1. SystemVerilog
2. UVM

we covered the training course of SystemVerilog. Then, after mid-year final exams we will start the UVM training.

## SystemVerilog Training

The team of engineers assigned by Si-Vision company have held meetings with us and prepared many helpful materials.

1. SystemVerilog full training provided by Si-Vision Academy
2. Software OOP full training provided by Si-Vision Academy
3. Reference books (SystemVerilog for Verification by Chris Spear)
4. Recommending best websites (chipverify, Testbench.in)

These materials helped us to learn and master the SystemVerilog HVL language

### SystemVerilog main topics

1. Introduction to Verification Flow and the verification engineer mindset
2. Data Types
3. Functions, Loops and Processes
4. Basics of Object-Oriented Programming
5. Randomization
6. Line and Functional Coverage
7. Assertions