Applied Learning Project: Designing PID Controller for 2nd Order System (RC Circuit) Using Root Locus Method

Objective:
Design a Proportional-Integral-Derivative (PID) controller for a second-order system represented by an RC circuit. The goal is to achieve specific performance requirements, including an overshoot of less than 15%, a 5% steady-state error, and a settling time of less than 3 seconds.

System Description:
An RC circuit models the second-order system under consideration.

Methodology:
1. Determine System Parameters: Obtain the values of resistors R_1, R_2, and capacitors C_1, C_2 from the circuit specifications.
2. Performance Requirements: Define the performance requirements, including overshoot, steady-state error, and settling time.
3. Root Locus Analysis: Implement the Root Locus method on the Arduino platform to analyze the system's closed-loop response and design the PID controller to meet the performance requirements.
4. PID Controller Design: Design the PID controller using the parameters obtained from the Root Locus analysis.
5. Hardware Implementation: Implement the PID controller on the Arduino platform to regulate the second-order RC circuit system in real time.
6. Testing and Validation: Verify the performance of the hardware-based PID controller by conducting experiments and analyzing the closed-loop system response.
7. Fine-tuning: Fine-tune the PID controller parameters to optimize the system's performance.

Deliverables:
1. Analysis report detailing the system parameters, performance requirements, and PID controller design methodology.

2. Arduino code implementing the Root Locus analysis and PID controller design.

3. Experimental results demonstrating the real-time regulation of the second-order RC circuit system using the hardware-based PID controller.

Expected Outcome:
The hardware-based PID controller implemented on the Arduino platform should effectively regulate the second-order RC circuit system, ensuring that the performance requirements, including overshoot, steady-state error, and settling time, are met within acceptable limits.