Project description

Design a 32-point FFT in RTL using the Cooley-Tukey FFT algorithm. The butterfly diagram for this is shown below:

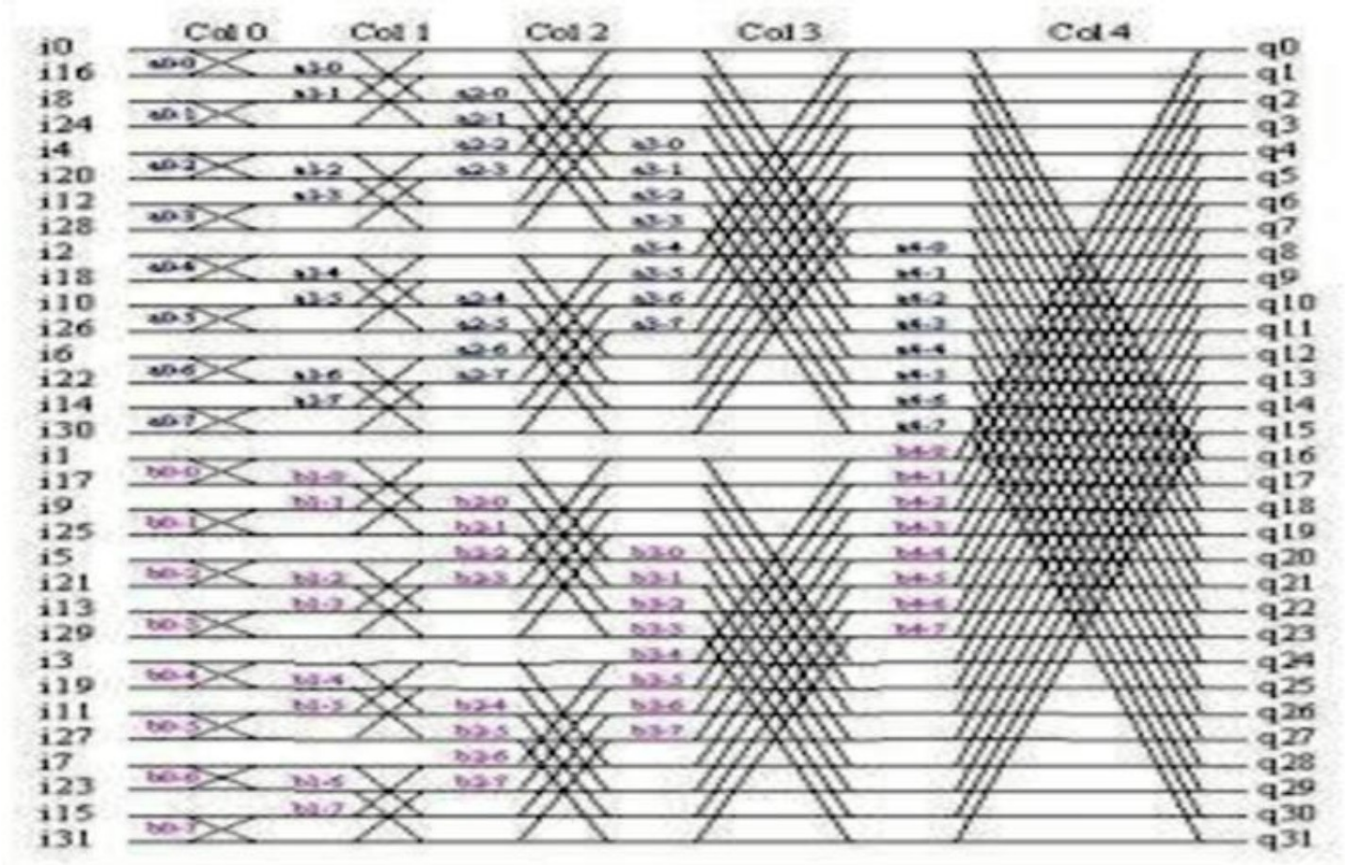

Figure 1 32-FFT butterfly diagram

Assumptions:

1-Inputs are 8 bits: 7 bits for integer number and 1 bit for sign.
2-Inputs go through a block which converts inputs to 24 bits by zero padding.
3-24 bits are divided to 10 bits for fraction and 13 bits for integer number and 1 bit for sign.

Design schematic

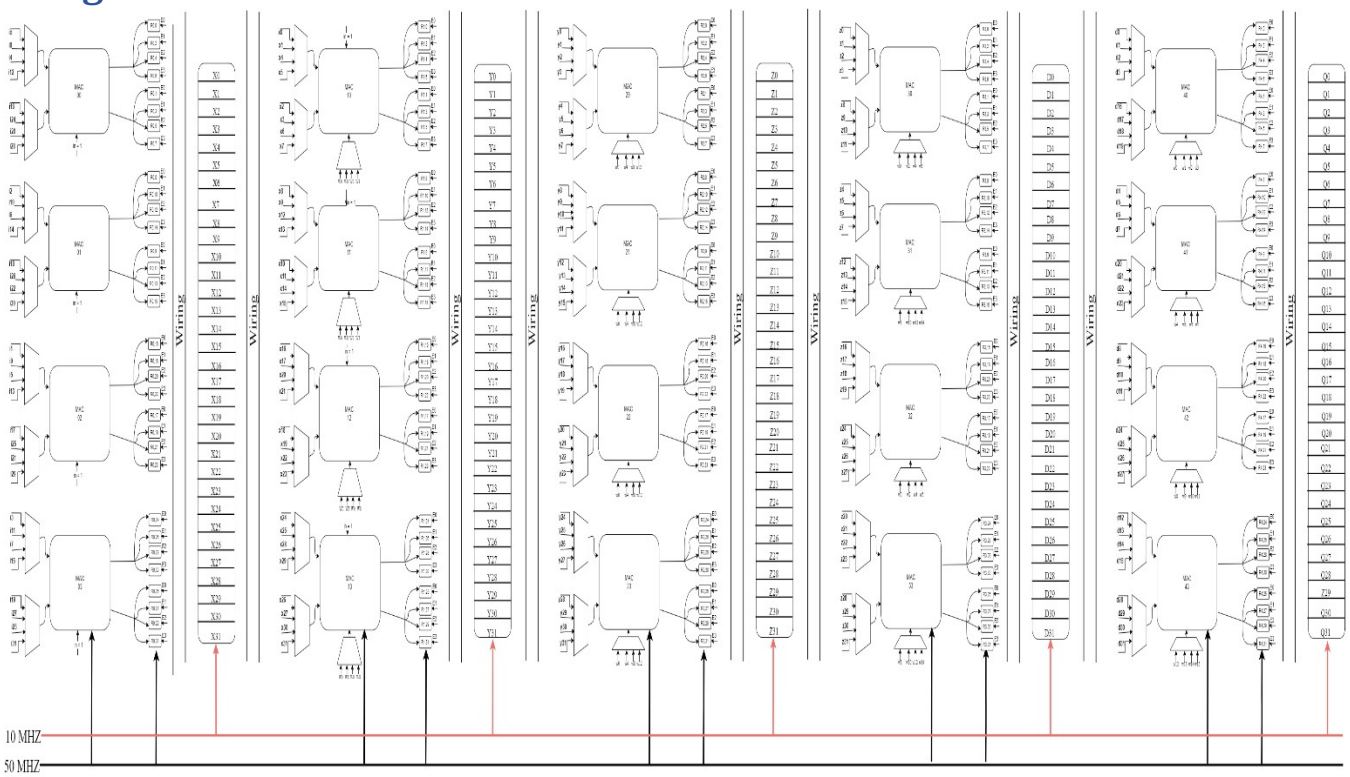

Figure 2 32-FFT design

For a better quality of design diagram:
https://drive.google.com/file/d/1dkkCorC0PDUxmRcLzsYQztOjM95RdZcE/view?usp=sharing

The throughput of FFT block is 10 MHZ and the throughput of MAC (multiply and accumulate) is 50 MHZ. We use time sharing concept in each column to decrease the hardware used in the FFT block.

Each MAC has 8 inputs and 8 outputs which means that in each column we use $\frac{32}{8}$=4 MACs. Using controller (MUXs, counter and decoder) we can control the flow of inputs and outputs then store outputs in latches with clock 50 MHZ after MAC and finally forwarding outputs to the next column through registers with clock 10 MHZ. The main function of registers with clock 10 MHZ is the pipelining between every 2 columns and here we get latency of 500 nsec.

Butterfly

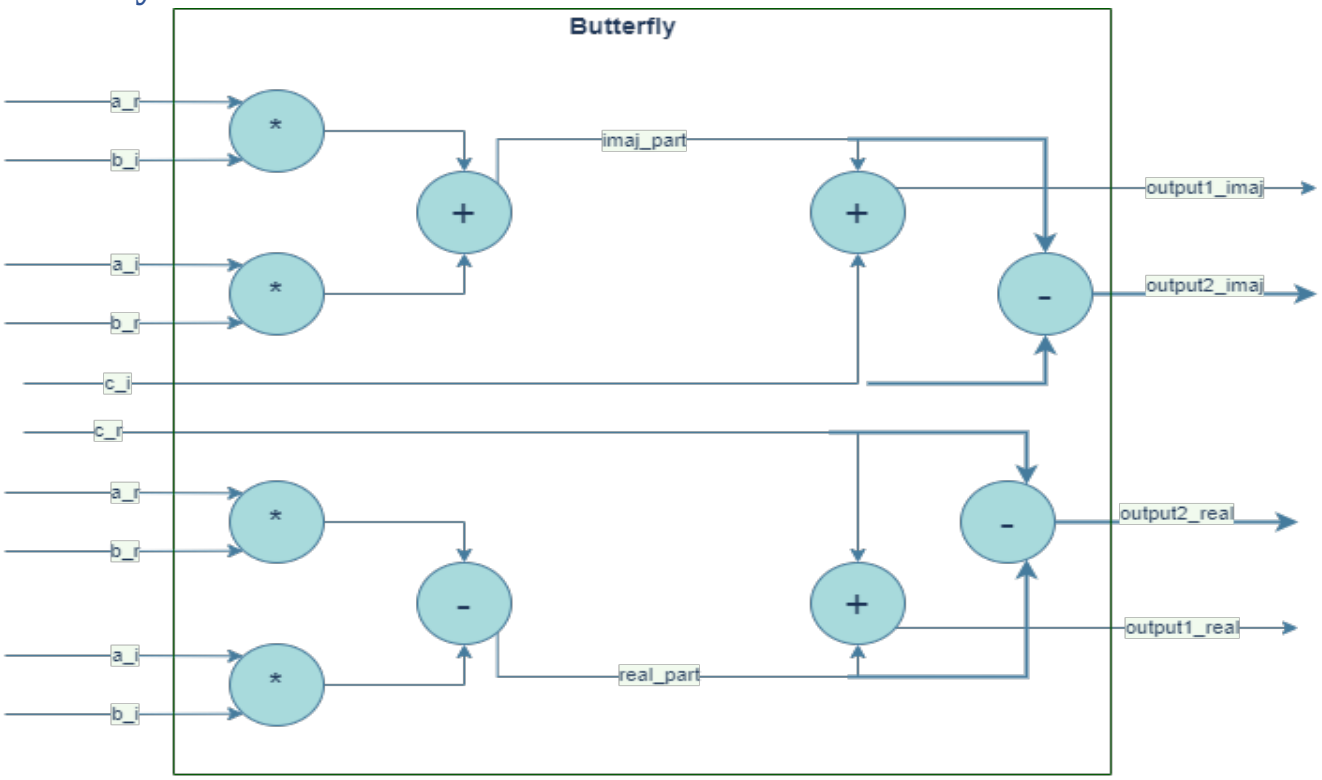

Figure 3 Butterfly implementation

Every input has real and imaginary values which go through MAC with twiddle factor where:
a: first input, b: twiddle factor, c: second input.

This MAC has 4 outputs (2 for real and 2 for imaginary):
Output1_real =c_r+(a_r*b_r-a_i*b_i) , Output2_real =c_r-(a_r*b_r-a_i*b_i).

Instead of using 4 multipliers to get output 1 and another 4 multipliers to get output 2, we concluded that the multiplier inputs are common so we reduced the number of multipliers to half, so we get the result of both output1 and output2 using same 4 multipliers.

Controller

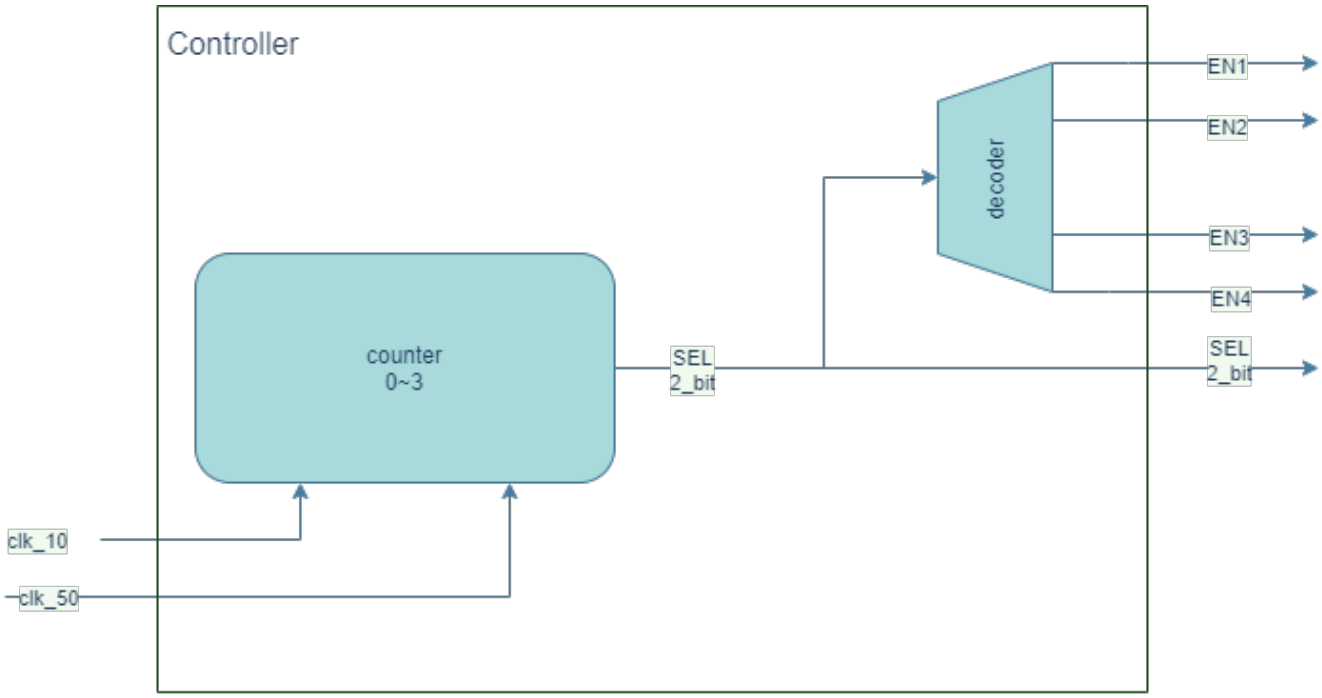

Figure 4 Controller implementation

This is controller consists of 2-bit counter and 2-to-4-bit decoder. Inputs for counter are 10-MHZ and 50-MHZ clocks where we use 50-MHZ clock for increment the counter and the 10-MHZ clock to reset the counter. Outputs of counter are selection lines of MUXs to select the proper inputs to MACs. Also, outputs of counter are the inputs of decoder which has 4 enables to open latches in the proper time to store outputs of MAC.

Results

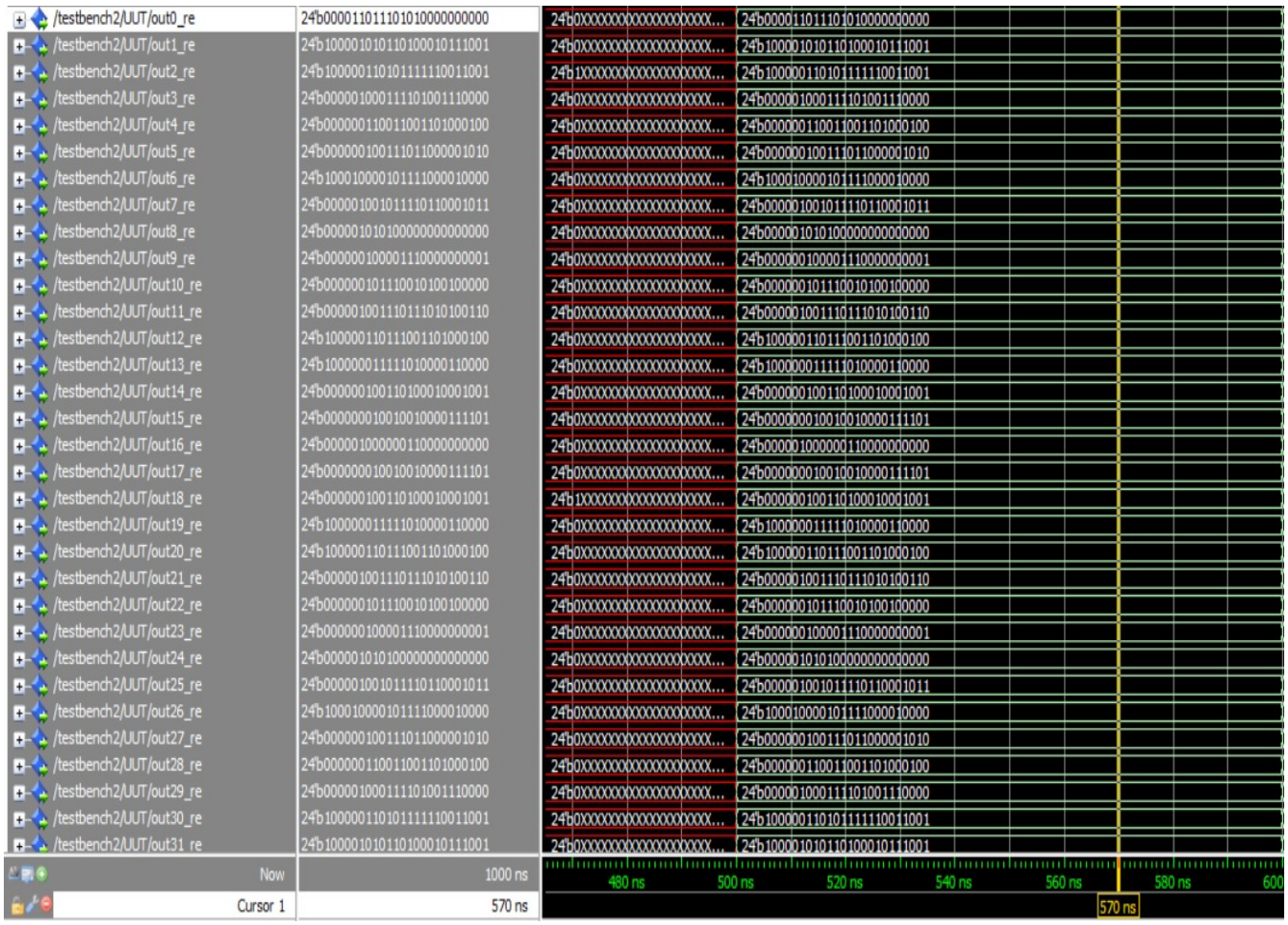

Figure 5 Real part of first 32 outputs (from 500 to 600 ns)

The expected outputs are:

Out0_re=885	000011011101010000000000
Out1_re=-346.28	100001010110100100011110
Out2_re=-216.09	100000110110000001011100
Out3_re=286.84	000001000111101101011100
Out4_re=204.84	000000110011001101011100
Out5_re=157.5	000000100111011000000000
Out6_re=-535.43	100010000101110110111000
Out7_re=303.4	000001001011110110011001
Out8_re=336	000001010100000000000000
Out9_re=134.62	000000100001101001111010
Out10_re=185.18	000000101110010010111000
Out11_re=315.75	000001001110111100000000
Out12_re=-220.84	100000110111001101011100
Out13_re=-125.33	100000011111010101010001

Out14_re=154.34	00000010011010010101100
Out15_re=73.497	00000001001001011111100
Out16_re=259	00000100000011000000000
Out17_re=73.497	00000001001001011111100
Out18_re=154.34	00000010011010010101100
Out19_re=-125.33	10000001111101010101001
Out20_re=-220.84	10000011011100110101100
Out21_re=315.75	00000100111011110000000
Out22_re=185.18	00000010111001001011000
Out23_re=134.62	00000010000110100111010
Out24_re=336	00000101010000000000000
Out25_re=303.4	00000100101111011001001
Out26_re=-535.43	10001000010111011011000
Out27_re=157.5	00000010011101100000000
Out28_re=204.84	00000011001100110101100
Out29_re=286.84	00000100011110110101100
Out30_re=-216.09	10000011011000000101100
Out31_re=-346.28	10000101011010010001110

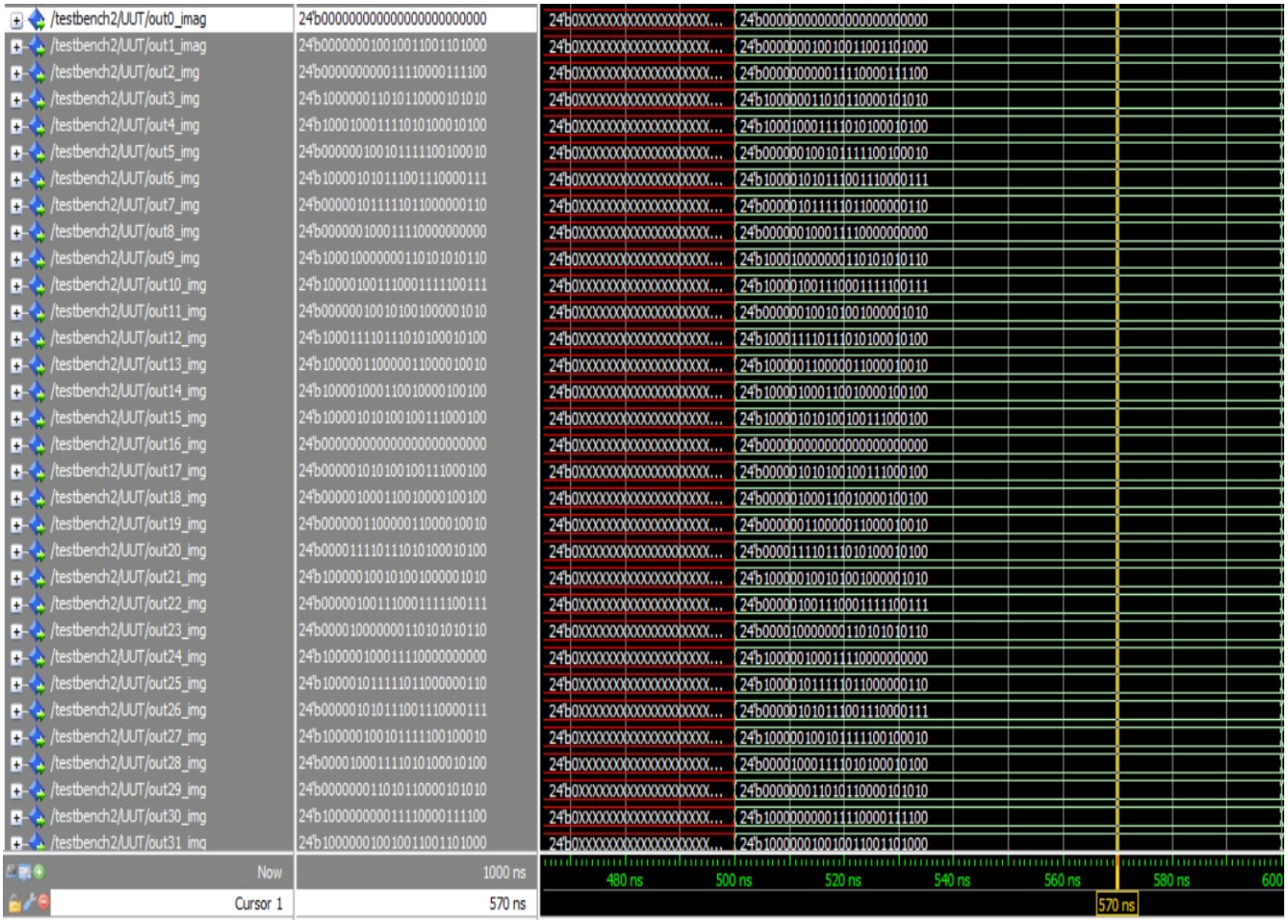

Figure 6 imaginary part of first 32 outputs (from 500 to 600 ns)

The expected outputs are:

Out0_img=0	000000000000000000000000
Out1_img=74.05	000000010010100000110011
Out2_img=15.131	000000000011110010000110
Out3_img=-107.26	100000011010110100001010
Out4_img=-573.35	100010001111010101100110
Out5_img=151.97	000000100101111111100001
Out6_img=-349.3	100001010111010100110011
Out7_img=381.74	000001011111011011110101
Out8_img=143	000000100011110000000000
Out9_img=-515.65	100010000000111010011001
Out10_img=-313.41	100001001110010110100011
Out11_img=148.81	000000100101001100111101
Out12_img=-989.35	100011110111010101100110
Out13_img=-193.61	100000110000011001110000
Out14_img=-280.98	100001000110001111101011
Out15_img=-338.53	100001010100101000011110

Out16_img=0	000000000000000000000000
Out17_img=338.53	000001010100101000011110
Out18_img=280.98	000001000110001111101011
Out19_img=193.61	000000110000011001110000
Out20_img=989.35	000011110111010101100110
Out21_img=-148.81	100000100101001100111101
Out22_img=313.41	000001001110010110100011
Out23_img=515.65	000010000000111010011001
Out24_img=-143	100000100011110000000000
Out25_img=-381.74	100001011111011011110101
Out26_img=349.3	000001010111010100110011
Out27_img=-151.97	100000100101111111100001
Out28_img=573.35	000010001111010101100110
Out29_img=107.26	000000011010110100001010
Out30_img=-15.131	100000000011110010000110
Out31_img=-74.05	100000100101000000110011

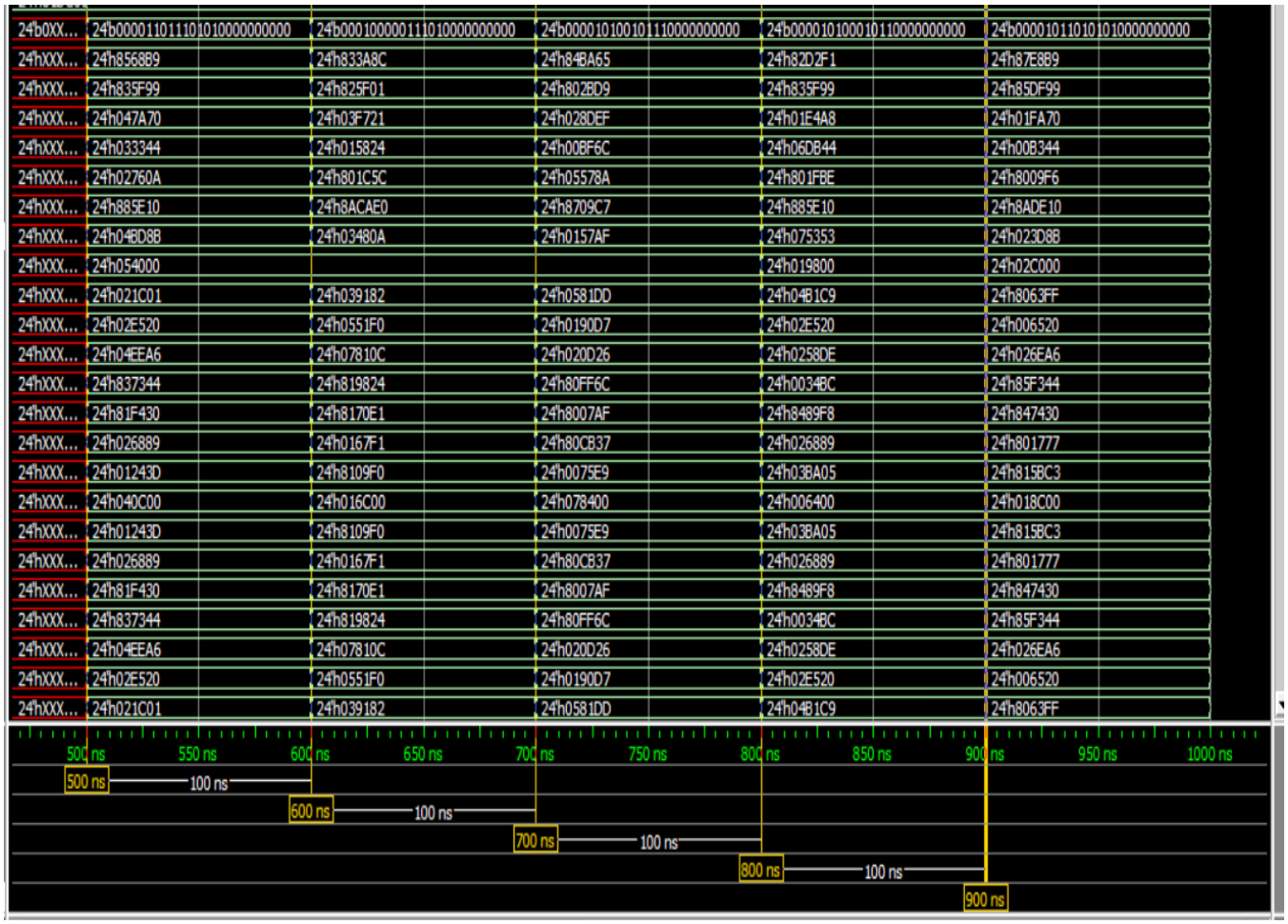

Figure 7 Outputs of 5 inputs

Here we find that throughput of FFT is 10 MHZ since every output come out after 100 ns from the previous output.

Synthesis Results

Timing Constraints

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.378 ns	Worst Hold Slack (WHS):	0.157 ns	Worst Pulse Width Slack (WPWS):	9.650 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	40032	Total Number of Endpoints:	40032	Total Number of Endpoints:	15408

All user specified timing constraints are met.

Figure 8 Timing Constraints

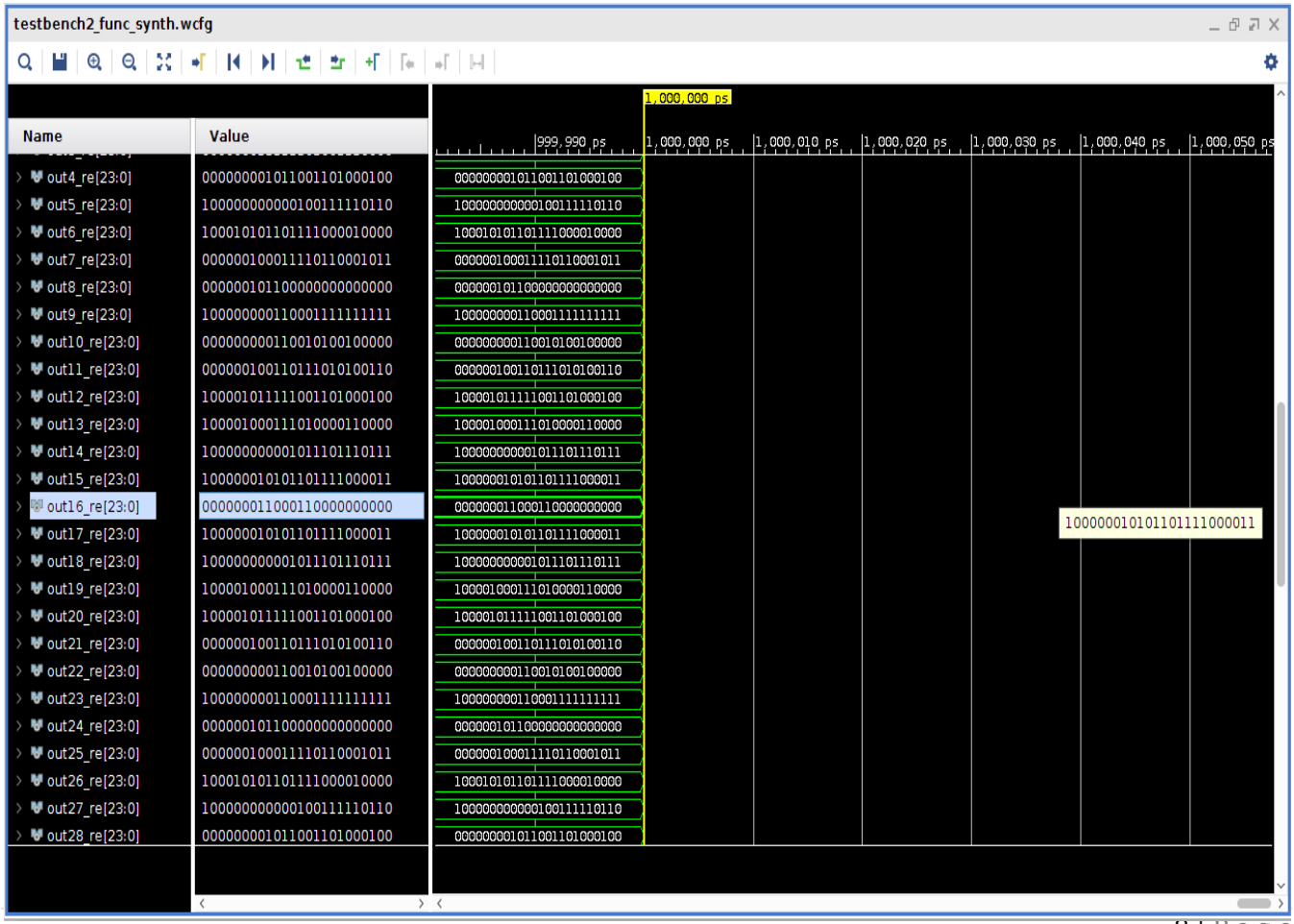

Figure 9 Post synthesis simulation real part of last 32 outputs (from 900 to 1000 ns)

Post Synthesis Simulation:

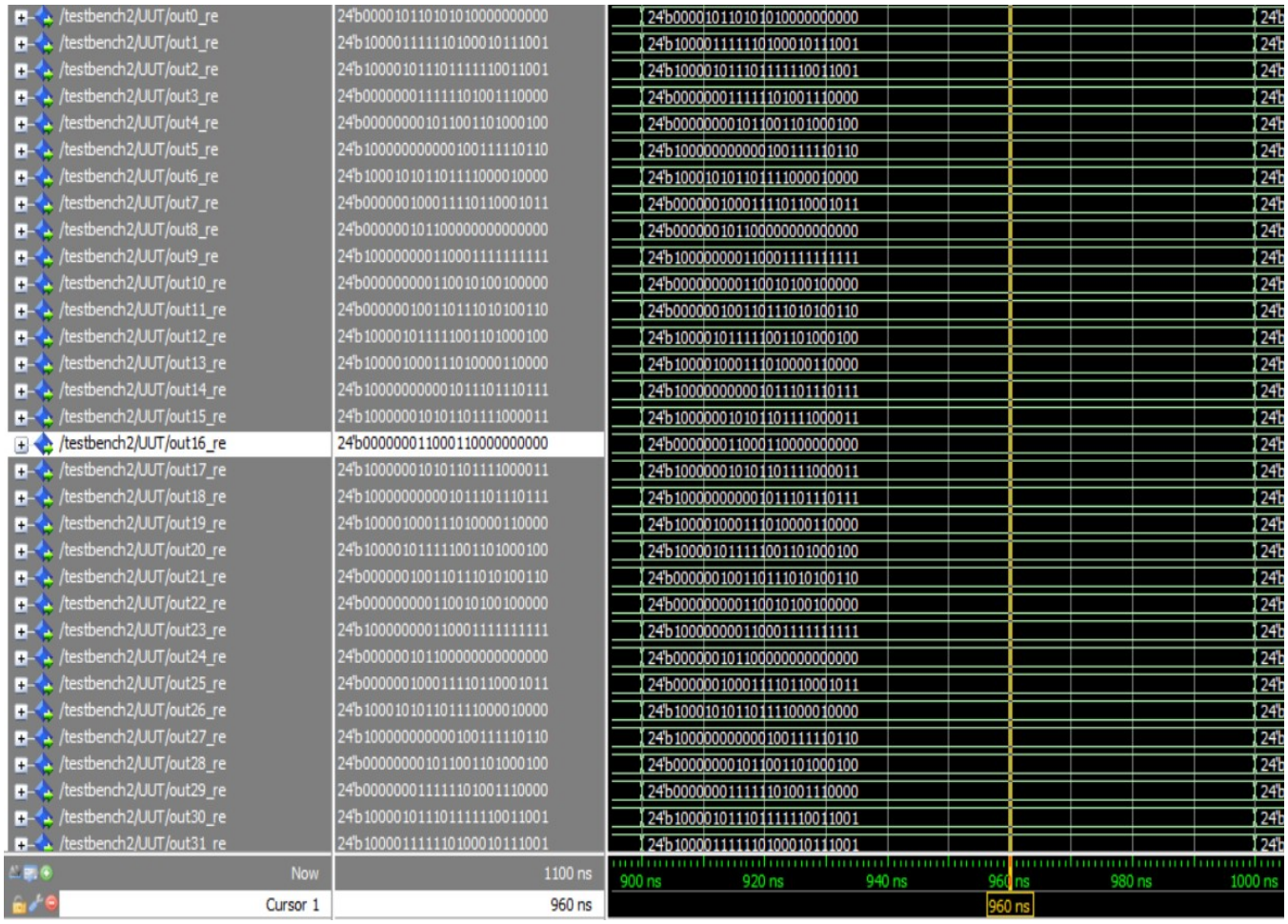

Figure 10 before synthesis simulation real part of last 32 outputs (from 900 to 1000 ns)

- From figure 9 post synthesis and figure 10 before synthesis show that the function still valid and output value are still the same before synthesis.

Resource usage and report of utilization

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	8595	0	433200	1.98
LUT as Logic	8595	0	433200	1.98
LUT as Memory	0	0	174200	0.00
Slice Registers	15408	0	866400	1.78
Register as Flip Flop	15408	0	866400	1.78
Register as Latch	0	0	866400	0.00
F7 Muxes	10	0	216600	<0.01
F8 Muxes	0	0	108300	0.00

Figure 11 resource usage and report of utilization