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| --- |
| Electronics project  2018 |
|  |
| **represented by**  Huda Ehab El\_Sayed  Nourhan Mohammad Fahmy  Marwa Ibrahim Fathy  Shahd Mahmoud  Mohamed Gendy Mohammed  Mohammed Shaban Mohammed   |  |  |  | | --- | --- | --- | | **ID** | **SEC** | **Name** | | 9230974 | 4 | هدى ايهاب السيد ابراهيم | | 9230966 | 4 | نورهان محمد فهمي | | 9230856 | 4 | مروة ابراهيم فتحي | | 9230485 | 2 | شهد محمود | | 9230755 | 3 | محمد جندي محمد | | 9230775 | 3 | محمد شعبان محمد | |

**Supervised by**

**Eng. Mahmoud Yahya**

**Problem 1**

**Circuit Schematics:**

A screenshot of a computer screen

Description automatically generated

Figure 1

**a.** Run DC with VCM=1.5V

i. Show the DC voltages of all points and validate it using hand calculations

**hand analysis:**

Due to symmetry in Q1 and Q2 , we can see this is a current mirror circuit so:

Now we can see that Q2 works as current source to the differential pair Q3 and Q4 which are clearly symmetric so the current will be divided equally in each transistor

Assume all transistors are in saturation mode :

Check saturation:

For M4:

Correct Assumption

For M0 and M1:

Correct Assumption

## Simulation:

1\_open ADL

2\_DC analysis->save dc operating point

3\_Run

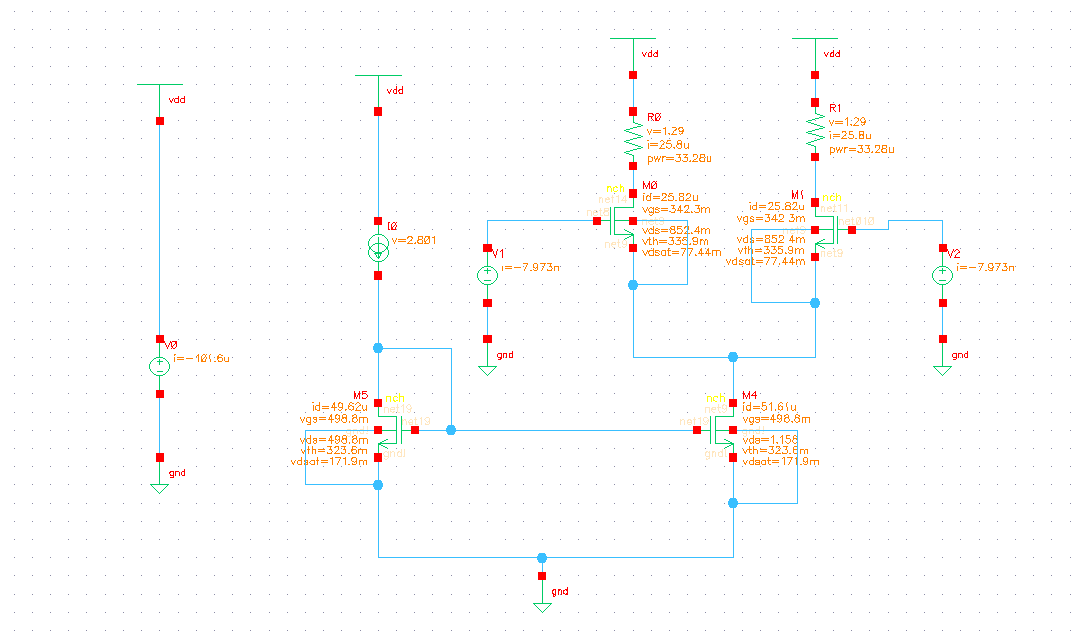
**DC operating point from simulation:**

Figure 2

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| VDD | VD5 | VG5 | VD4 | VG 4 | VS1,2 | VD0,1 | VG 0,1 | VS 0,1 |
| 3.3 V | 498.8 mV | 498.8 mv | 1.158 V | 498.8mv | grounded | 2.01 V | 1.5 V | 1.158 V |

**ii. Show the operating point of all transistors and make sure that they are in SAT (region 2)**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Mosfet | Drain current | | Vgs | | Vds | |
|  | calculated | measured | calculated | measured | calculated | measured |
| M\_0 | 25 | 25.8 | 342.3 mv | 342.3 mV |  | 852.3 mV |
| M\_1 | 25 | 25.8 | 342.3 mv | 342.3mv |  | 852.3 mV |
| M\_4 | 50 | 51.61 | 498.8 mv | 498.8 mV |  | 1.158V |
| M\_5 | 50 | 49.62 | 498.8 mv | 498.8mv | 498.8 mv | 498.8 mV |

iii. Show the power consumption

|  |  |
| --- | --- |
| Hand Analysis:          Simulation: . | C:\Users\dell\Desktop\diff_amp_12png.png  Figure 3 |

**Calculated Power dissipated in transistors :**

In M0,M1:

In M4:

In M5:

**Power dissipated in transistors from simulation:**

In M0,M1:

In M4:

In M5:

b. Run transient simulations (show the equation for every requirement ,how you get the results in cadence and the simulation setup)

**Transiant analysis:**

1-open Adl. 2- analysis. 3- choose tran. 4-set certain output

i. Show the current of VOUT+ & VOUT- across time

|  |  |
| --- | --- |
| **Equation in cadence calculator:**  **IT(“/M1/D”)** | **Hand equation** |

**Output from simulation** :Current of Vout+

A graph of a diagram

Description automatically generated

Figure 4

|  |  |
| --- | --- |
| **Equation in cadence calculator:**  **IT(“/M0/D”)** | **Hand equation** |

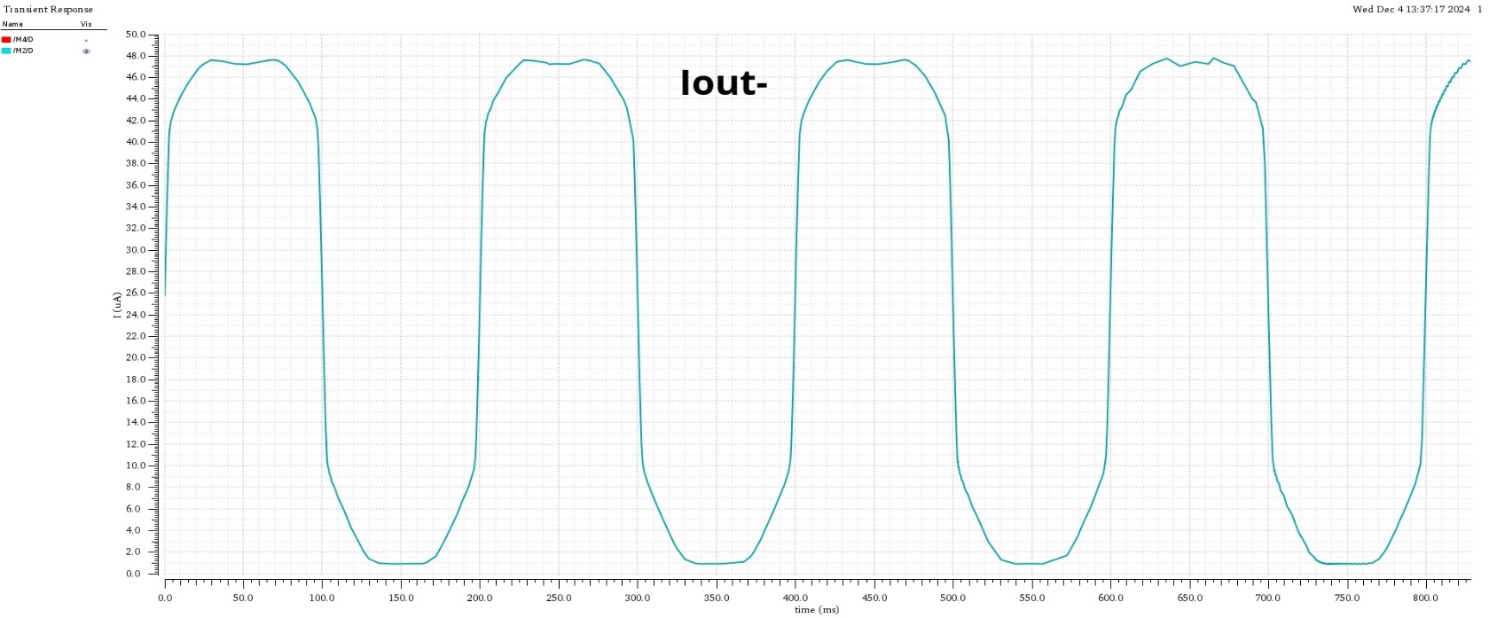
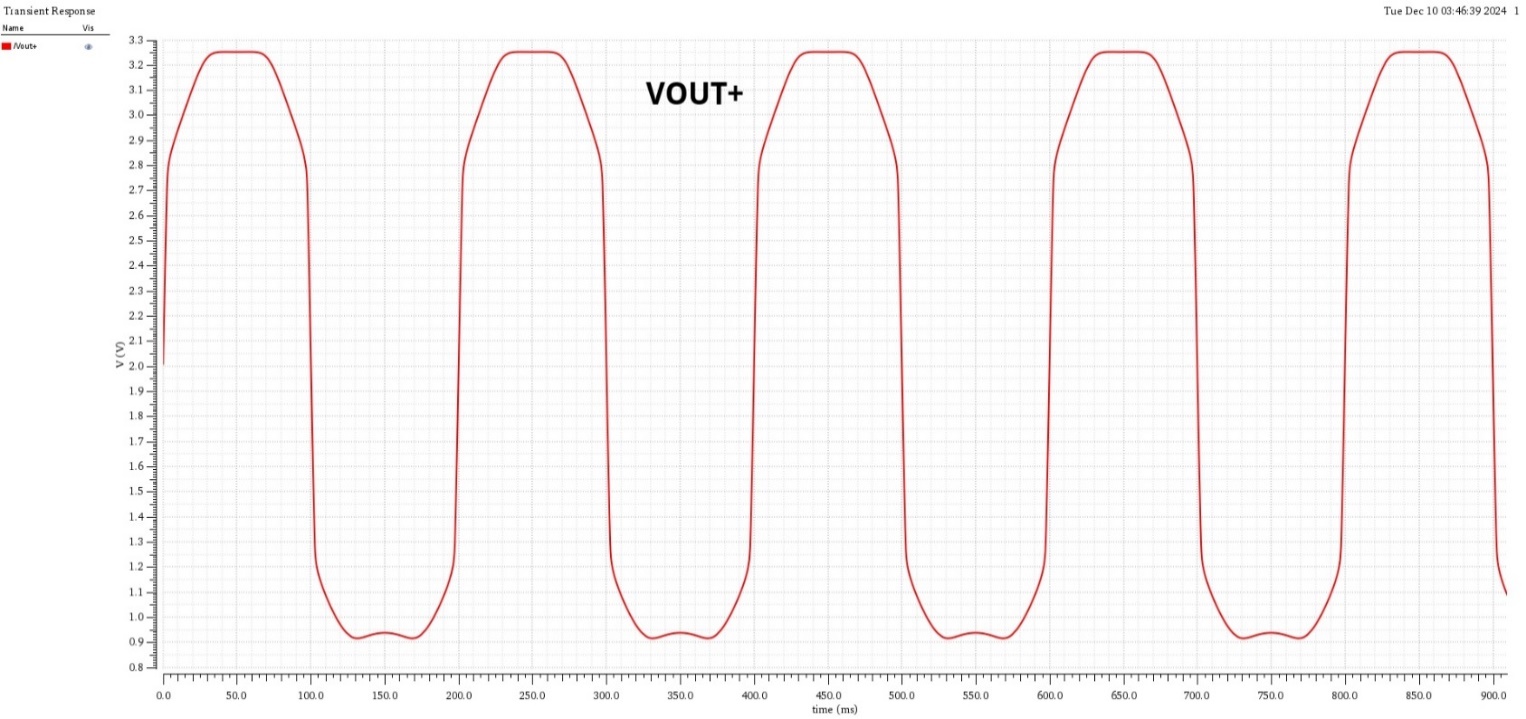
**Output from simulation** :current of Vout-

Figure 5

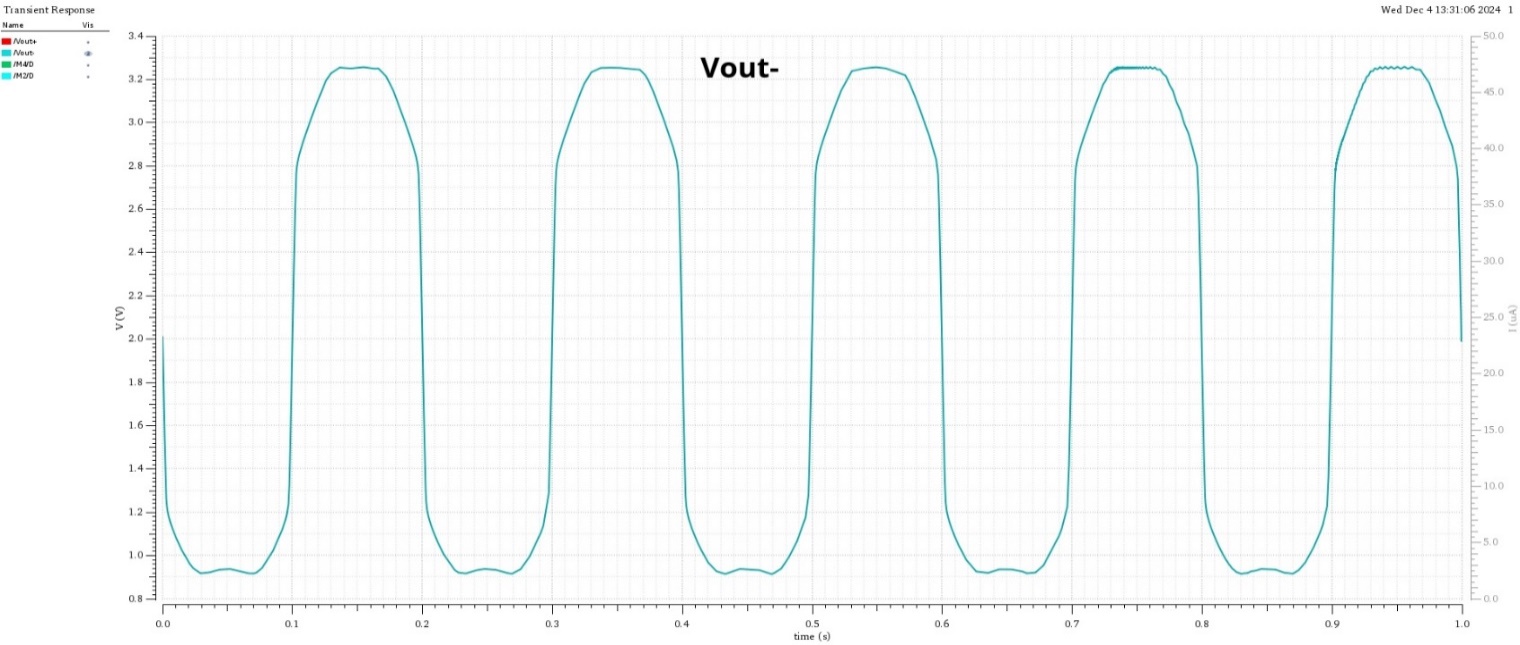
ii. Show the voltage of VOUT+&VOUT- across time

|  |  |
| --- | --- |
| **Equations in cadence calculator:**  **VT(“/Vout+”)**  **VT(“/Vout-”)** | **Hand equations** |

**Equation in cadence calculator:** VOLTAGE VOUT+

**Output from simulation** 

**Output from simulation** VOLTAGE VOUT-



iii. Show the voltage of VOUT differential across time

|  |  |
| --- | --- |
| **Equations in cadence calculator:**  **VT(“/Vout+”) - VT(“/Vout-”)** | **Hand equations** |

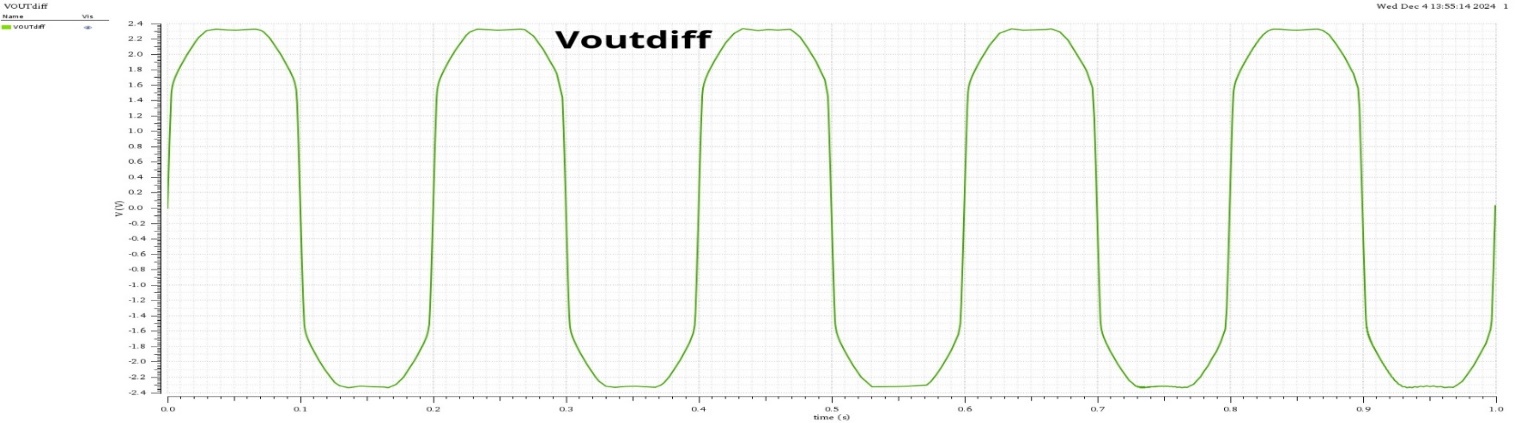
**Output from simulation** :Voutdiff

Figure 8

iv. Calculate the output swing

|  |  |
| --- | --- |
| **Equations in cadence calculator:**  **ymax(VT(“/Vout+”) - VT(“/Vout-”)) - ymin(VT(“/Vout+”) - VT(“/Vout-”))** | **Hand equations** |

**Output from simulation**

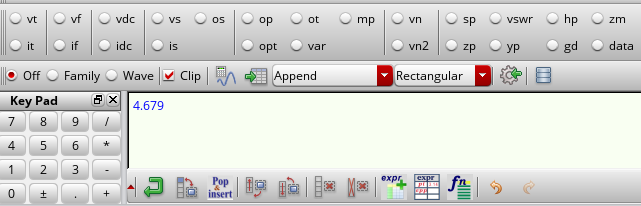


Figure 9

c. Run AC simulations (show equation for every requirement,how you get the results in cadence and the simulation setup)

**Hand Analysis** of this part are doneby applying **half circuit concept.**

**A diagram of a circuit

Description automatically generated**

Figure 10

**Let**

**&**

**Values taken from simulation**

By applying half circuit concept

By adding the source resistance in consideration so it converted to 2 common source amplifiers with source resistance degeneration but because of odd symmetry a virtual ground in parallel with so it will be cancelled

so

The same in the case of the Common mode input voltage signal but here is an even symmetry and not equal zero so will be taken in consideration

1-Get 𝐴𝑑𝑖𝑓𝑓−𝑑𝑖𝑓𝑓

|  |  |
| --- | --- |
| **A screenshot of a computer  Description automatically generatedEquation in cadence calculator:**  Figure 11 | **Hand equations:** |

A graph with a red line

Description automatically generated**Output from simulation:**

Figure 12

2- Get 𝐴𝑑𝑖𝑓𝑓−𝐶𝑀

|  |  |
| --- | --- |
| **A screenshot of a computer  Description automatically generatedEquation in cadence calculator:** | **Hand equations** |

**A graph with a red line

Description automatically generatedOutput from simulation:**

Figure 13

3-Get 𝐴𝐶𝑀−𝐶𝑀

|  |  |
| --- | --- |
| A screenshot of a computer  Description automatically generated**Equation in cadence calculator:**  Figure 14 |  |

A graph with a red line

Description automatically generated**Output from simulation**

Figure 15

4. Get 𝐴𝐶𝑀−𝑑𝑖𝑓.

|  |  |
| --- | --- |
| A screenshot of a computer  Description automatically generated**Equation in cadence calculator:**  Figure | **Hand equations** |

**A graph showing a number of numbers

Description automatically generated with medium confidenceOutput from simulation:**

Figure 17

**5-CMRR**

6-𝑅𝑂𝑈𝑇−𝑑𝑖𝑓𝑓

|  |  |
| --- | --- |
| **Equation in cadence calculator:**  A screenshot of a computer  Description automatically generated  Figure 18 | **Hand equations** |

* Output resistance ( )is defined as:

=

* ​ is the differential-mode output voltage, which in this case is approximated by (the voltage difference across the two outputs).
* is the differential-mode output current, which flows through the DC source, represented by .
* We used the following expression in the Cadence Calculator:
* Here's what each term represents:
  + =
  + :
  + : The current flowing through the DC voltage source .
* The expression calculates the ratio of the voltage difference across the two output nodes to the current through the DC source, **differential output resistance** ​.

**Output from simulation:**

A graph with numbers and lines

Description automatically generated

Figure 19

7-𝑅𝑂𝑈𝑇−𝐶*M*

|  |  |
| --- | --- |
| **Equation in cadence calculator:**  Figure  A screenshot of a computer  Description automatically generated | **Hand equations** |

= 24.9699 kΩ

* Output resistance ( )is defined as:
* Since the AC magnitude of the current source is 1 A, the voltage at the output node ()is numerically equal to ()​ directly:

Note: VF("/net14")=

* We used VF("/net14"), which calculates the voltage at the output node net14

1. Because the AC current source is set to 1 A, VF("/net14")directly gives the small-signal **common-mode resistance**  ​.

* The plot shows how behaves across frequencies, starting flat at low frequencies (~25 kΩ) and decreasing at higher frequencies due to parasitic effects.

**Output from simulation:**

A graph with text on it

Description automatically generated

**Problem2** Current mirror.

**Simulator Circuit:**

A computer screen shot of a diagram

Description automatically generated

Figure 22

**Part1**

**Hand analysis:**

A diagram of a circuit

Description automatically generated**As D1 & G1 are connected so Q1 will be**

**In saturation**

**V**

**From the concept of current mirroring**

**Neglecting channel length modulation**

**Figure 23**

**As Q2 is in saturation**

**As  *&***

**\* 100**

**From hand analysis:**

**From simulation:**

**Part2**

1.

**Output from simulation:**

A graph with a red line

Description automatically generated

Figure 23

**Observation:**

Slight increasing in output voltage () will set initially in triode region such as the transistor reacts as a resistor so output current () has a linear relation with output voltage ()), then after a specific voltage known as overdrive voltage gets in saturation such as current is kept constant while increasing voltage but as a result of channel length modulation there is a small increase in output current, And with the increase of the output voltage the transistor fall in break down region in which it lose its characteristics.

2.

**Output from simulation:**

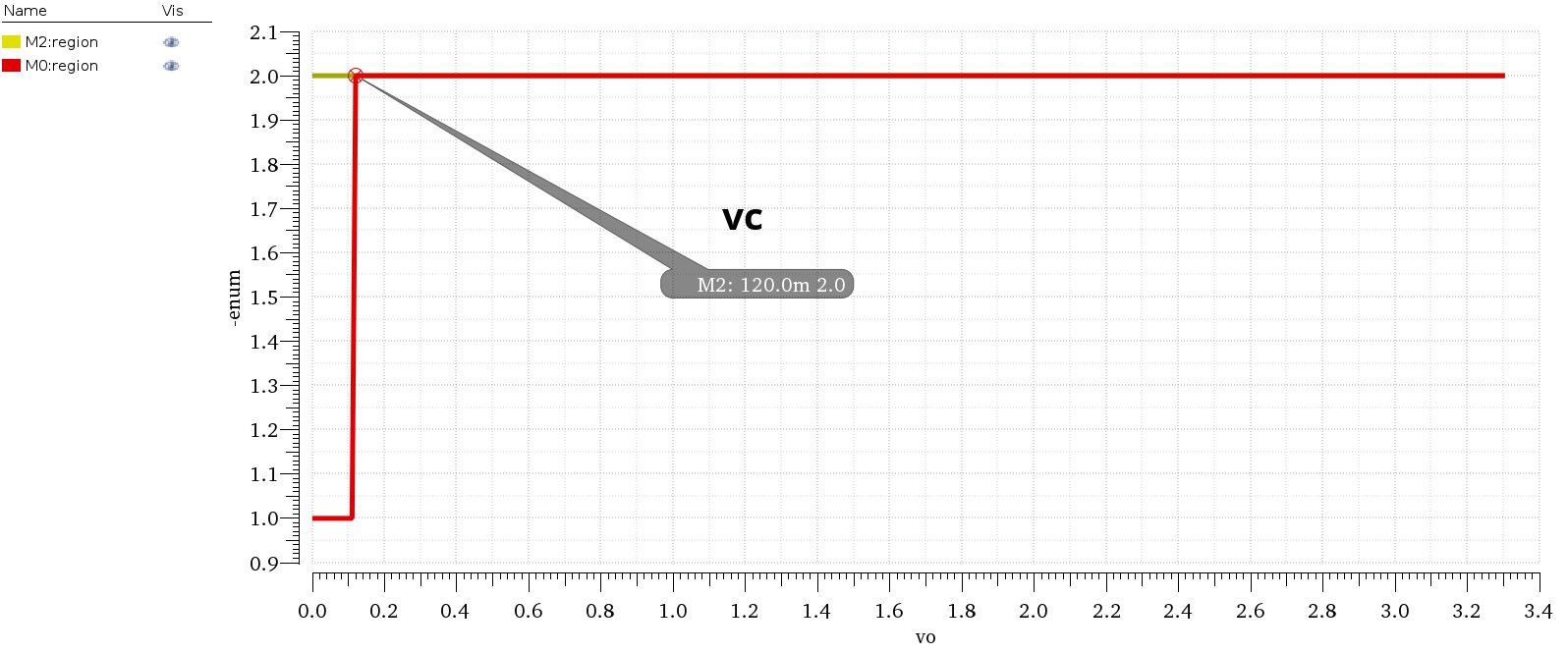


Figure 24

**Comments:**

Compliance voltage from its definition is the minimum voltage to derive the current mirror in a right way which gives approximately a constant current.

From simulation we found that

**compliance voltage=120m V**

, after this value the transistor  will be in saturation and work as ideal current mirror

3.

The overdrive voltage is the minimum voltage that makes saturation.

We neglect Q1 as its drain and gate are connected so any small voltage will set it in saturation.

Which calculated before from part1

**4.**

**Output from simulation:**

**A graph showing the current error

Description automatically generated**

Figure 25

So, it has the Same variation as , but with a different slope and shifted.

5.

**Output from simulation:**

**A graph with a red line

Description automatically generated**

Figure 26

**Comment:**

At low values, ​ starts low and increases steadily. This could correspond to the saturation of the transistor or the mirror's inability to sustain higher resistance at low output, a maximum value at an intermediate , indicating optimal operation of the current mirror at this point. This is where the circuit might achieve the highest output impedance, After the peak, begins to drop with further increases in This suggests the circuit enters a region where it can no longer maintain a high impedance, likely due to the transistor moving out of its active region.

**Output from simulation:**

A graph with a red line

Description automatically generated

Figure 27

At

We perform a frequency sweep of ​ to identify the frequency at which the influence of the internal capacitance of the transistor becomes significant. This analysis highlights the point where the capacitive effects begin to dominate, impacting the impedance and altering the circuit's performance.

**Part3**

**1\_Plot output current vs L :**

**Output from simulation:**

**A graph with a red line

Description automatically generated**

Figure 28

**3\_Comment on the results:**

**Comments:**

So, if we neglected as it too small compared to we get that the inverse relation between L and  **,**asdirect proportional to and asL increases, decreases

And because it is not an exact linear relation the decreasing in the graph is a curve.

Note that the variation in L is the same so is the same in the 2 transistors.

**2\_Use calculator to get relative error :**

**Output from simulation:**

**A graph showing the current error

Description automatically generated with medium confidence**

Figure29

**3\_comment on the result:**

**Comment:**

As L increases the channel length modulation effect decreases so that ,the relative current error decreases as it easy to know where it could be neglected,And the output current only depends on the input current and there dimensions ( W & L ) .