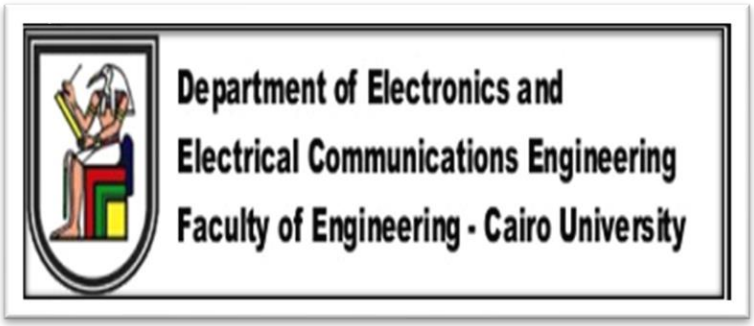
Electronics project



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Problem 1

Circuit Schematics:

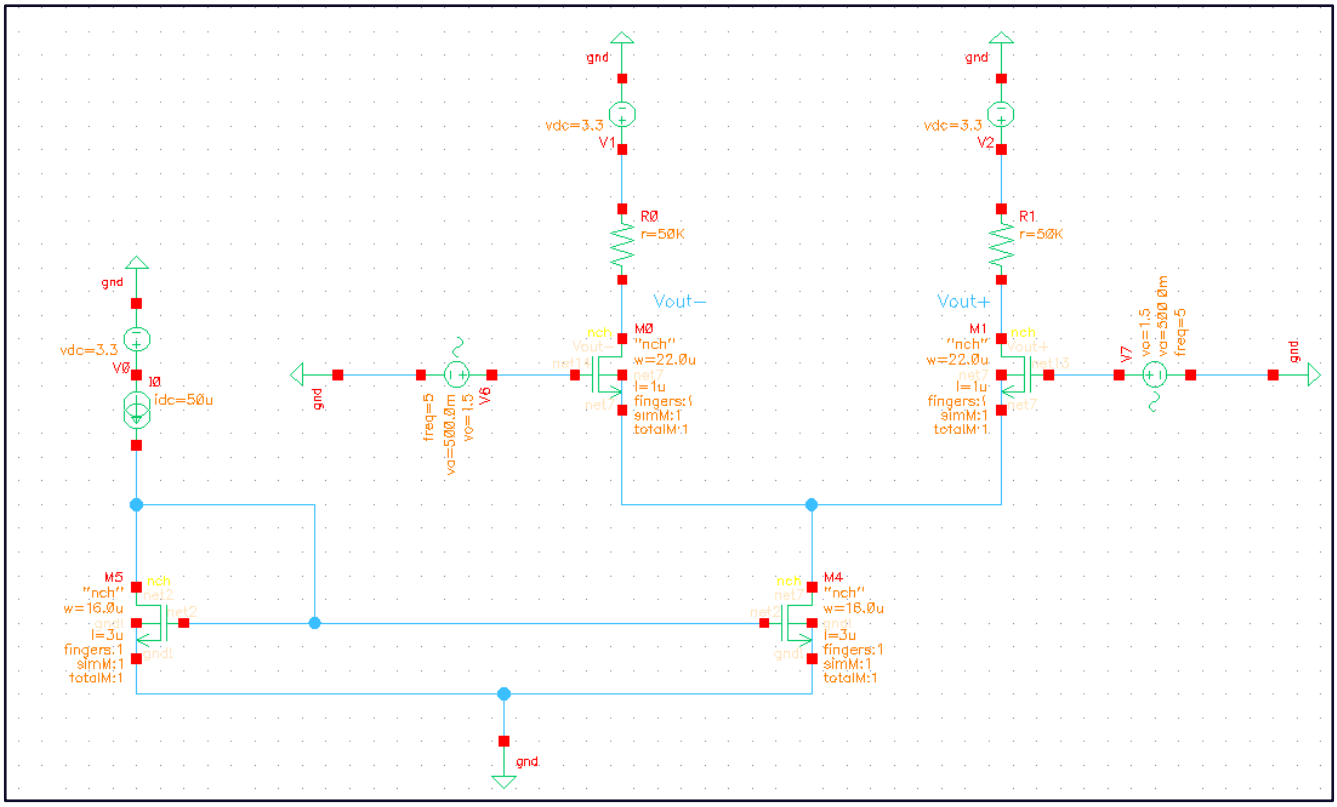


Figure 1: Problem 1 circuit

a. Run DC with VCM=1.5V

i. Show the DC voltages of all points and validate it using hand calculations

hand analysis:

Due to symmetry in **Q1** and **Q2** , we can see this is a current mirror circuit so:

$$I_{DS3} = I_{DS2} = 50\ \mu A$$

Now we can see that **Q2** works as a current source to the differential pair **Q3** and **Q4** which are clearly symmetric so the current will be divided equally in each transistor

$$I_{DS0} = I_{DS1} = 25\ \mu A$$

$$V_{out} -= V_{out} +$$
$$= V_{DD} - R \times i_{ds1} = 3.3 - 50 \times 10^{3} \times 25 \times 10^{-6} = 2.05\ V$$

$$V_{GS0} = V_{GS\,M1} = 342.3mV\ from\ simulation\ dc\ analysis$$

$$V_{S0,1} = V_{CM} - V_{GS} = 1.5 - 342.3 \times 10^{-3} = 1.1577\ V$$

Assume all transistors are in saturation mode :

$$V_{SO,1} = V_{CM} - V_{GS} = 1.5 - 0.3423 = 1.1577\ V$$

Check saturation:

For **M4**:

$$V_{DS\,M4} > V_{GS\,M4} - V_{TH}$$
$$V_{DS\,M4} = V_{S\,M0,M1} = 1.158\ V$$
$$V_{GS\,M4} - V_{TH} = 498.8 - 323.8 = 175mV$$

✓ **Correct Assumption**

For **M0** and **M1**:

$$V_{DS\,M0,M1} > V_{GS\,M0,M1} - V_{TH\,M0,M1}$$
$$V_{DS\,M0,M1} = 2.05 - 1.158 = 0.892\ V$$
$$V_{GS\,M0,M1} - V_{TH\,MO,M1} = 0.3423 - O.3359 = 6.4\ mV$$

✓ **Correct Assumption**

Simulation:

1- open ADL
2- DC analysis → save dc operating point
3- Run

DC operating point from simulation:

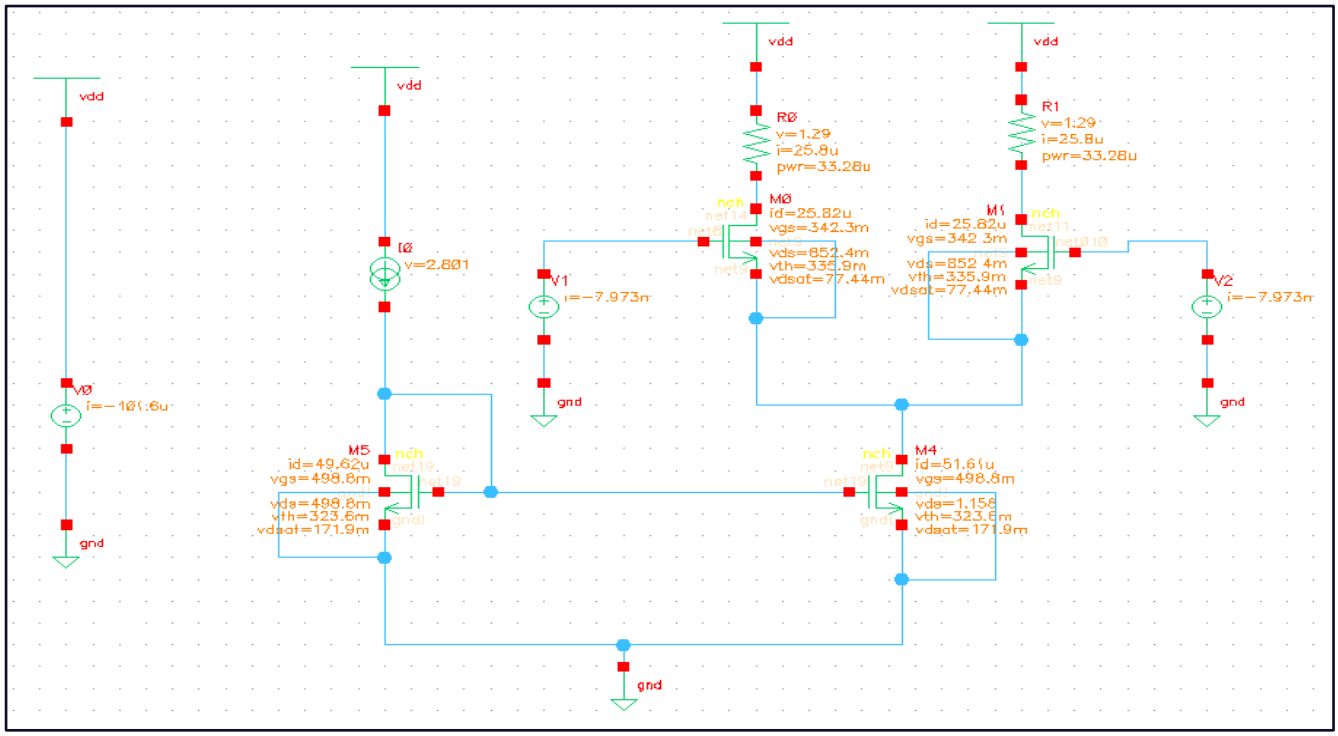


Figure 2: DC operating point from simulation

V_{DD}	V_{D5}	V_{G5}	V_{D4}	V_{G4}	$V_{S1,2}$	$V_{D0,1}$	$V_{G0,1}$	$V_{S0,1}$
3.3 V	**498.8 mV**	**498.8 mv**	**1.158 V**	**498.8mv**	**grounded**	**2.01 V**	**1.5 V**	**1.158 V**

ii. Show the operating point of all transistors and make sure that they are in SAT (region 2)

Mosfet	Drain current		V_{GS}	V_{DS}	
	calculated	measured	measured	calculated	measured
M_0	$25\ \mu A$	$25.8\ \mu A$	$342.3\ mV$	$0.892\ V$	$852.3\ mV$
M_1	$25\ \mu A$	$25.8\ \mu A$	$342.3\ mV$	$0.892\ V$	$852.3\ mV$
M_4	$50\ \mu A$	$51.61\ \mu A$	$498.8\ mV$	$0.175\ V$	$171.9\ mV$
M_5	$50\ \mu A$	$49.62\ \mu A$	$498.8\ mV$	—	$498.8\ mV$

iii. Show the power consumption

Hand Analysis:

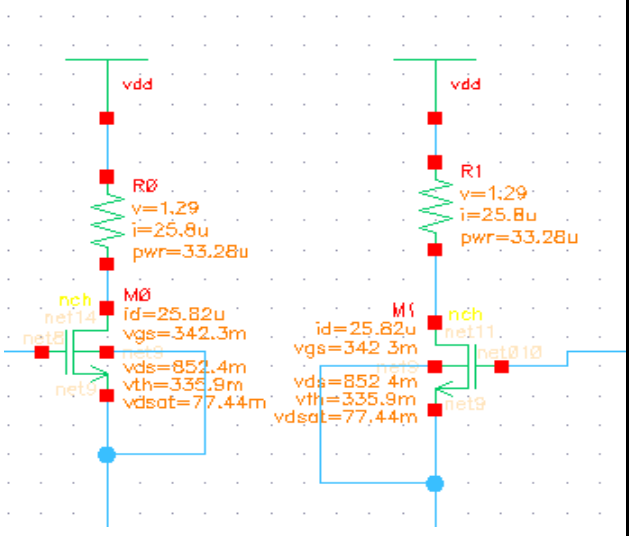
$$P = I^2 \times R$$
$$I = 25\,\mu A\ ,\ \ R = 50K\ ohm$$
$$P = (25 \times 10^{-6})^2 \times 50 \times 10^3$$

$$P\ in\ r1 = 3.125 \times 10^{-5}\ Watt$$
$$total\ power = 2 \times P\ in\ r$$

$$P\ total = 6.25 \times 10^{-5}\ Watt$$

Simulation:

$$power\ in\ simulation = 33.28\ \mu Watt$$
$$total\ power = 66.56\ \mu Watt$$



Calculated Power dissipated in transistors :

In **M₀,M₁**:

$$Power = I_{D1} \times V_{DS1} = 25 \times 10^{-6} \times 0.894 = 22.3\ \mu watt$$

In **M₄**:

$$Power = I_{D4} \times V_{DS4} = 50 \times 10^{-6} \times 1.158\ = 57.9\ \mu watt$$

In **M₅**:

$$Power = I_{D5} \times V_{DS5} = 50 \times 10^{-6} \times 498.8 \times 10^{-3} = 24.94\ \mu watt$$

Power dissipated in transistors from simulation:

In **M₀,M₁**:

$$Power = I_D \times V_{DS} = 22\mu watt$$

In **M₄**:

$$Power = I_D \times V_{DS} = 59.76\ \mu watt$$

In **M₅**:

$$Power = I_D \times V_{DS} = 24.75\ \mu watt$$

b. Run transient simulations (show the equation for every requirement ,how you get the results in cadence and the simulation setup)

Transient analysis:

1- open Adl.
2- analysis.
3- choose tran.
4- set certain output.

(APPLY INPUT TO M_2 1 AMPLUTIDE AND PHASE 0 AND , INPUT M_4 1 AMPLITUDE AND 180 DEGREE PHASE)

i. Show the current of VOUT+ & VOUT- across time.

Equation in cadence calculator: IT("/M1/D")	$I_{out+} = \frac{V_{DD} - V_{out+}}{R_1}$

Output from simulation :Current of Vout+

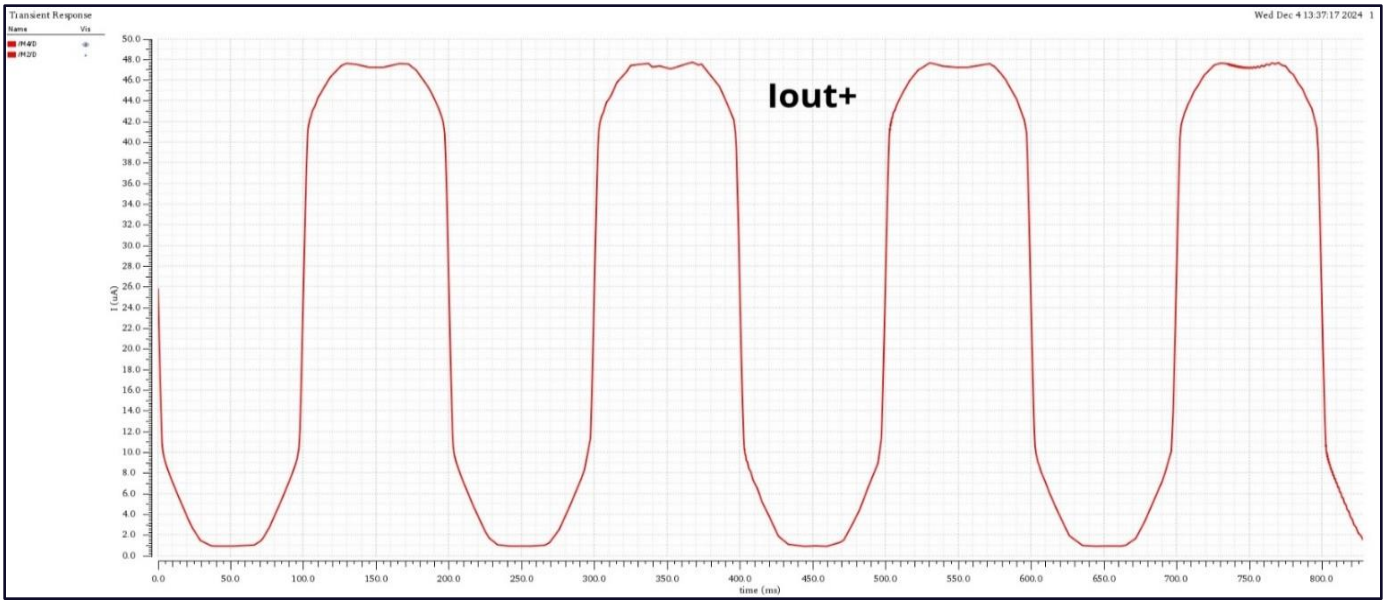


Figure 3: Output from simulation , Current of $V_{out}+$

Equation in cadence calculator: IT("/M0/D")	$I_{out-} = \frac{V_{DD} - V_{out-}}{R_0}$

Output from simulation :current of Vout-

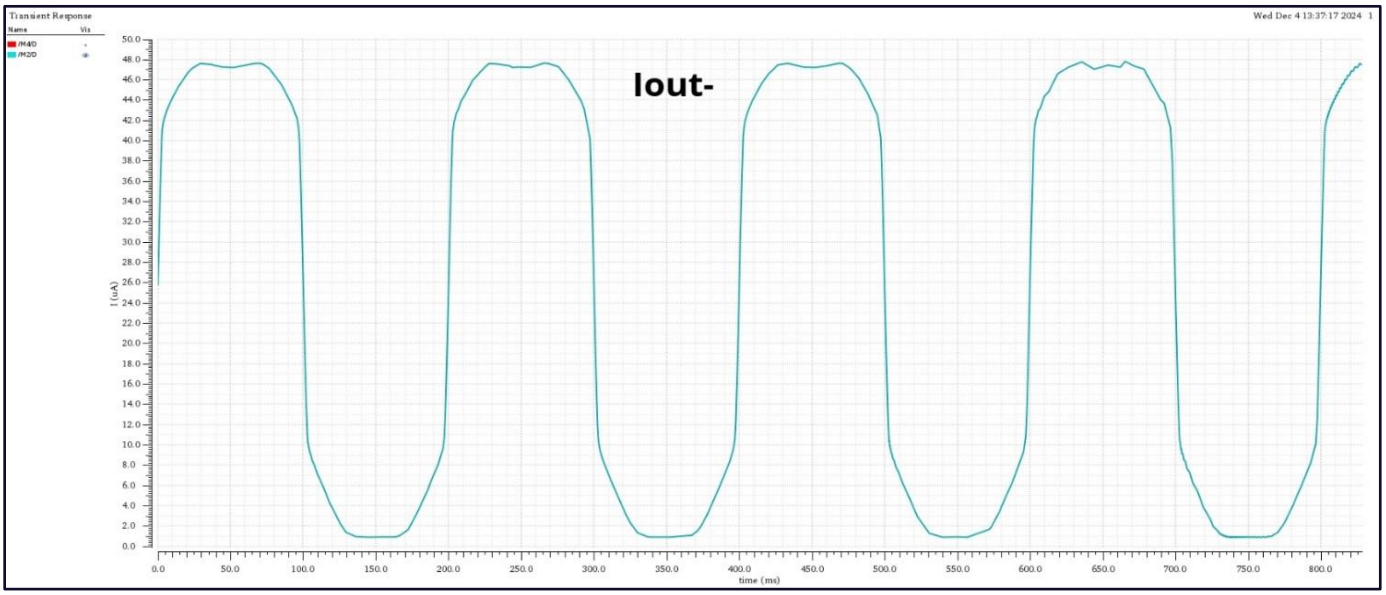


Figure 4: Output from simulation , Current of V_{out} -

ii. Show the voltage of $\mathbf{V_{OUT+}}$**&**$\mathbf{V_{OUT-}}$ across time

Equations in cadence calculator:	$V_{OUT+} = V_{CM} + \Delta v_{(-)}$ $V_{OUT-} = V_{CM} + \Delta v_{(+)}$
VT("/Vout+") **VT("/Vout-")**	

Equation in cadence calculator: VOLTAGE V_{OUT+}

Output from simulation

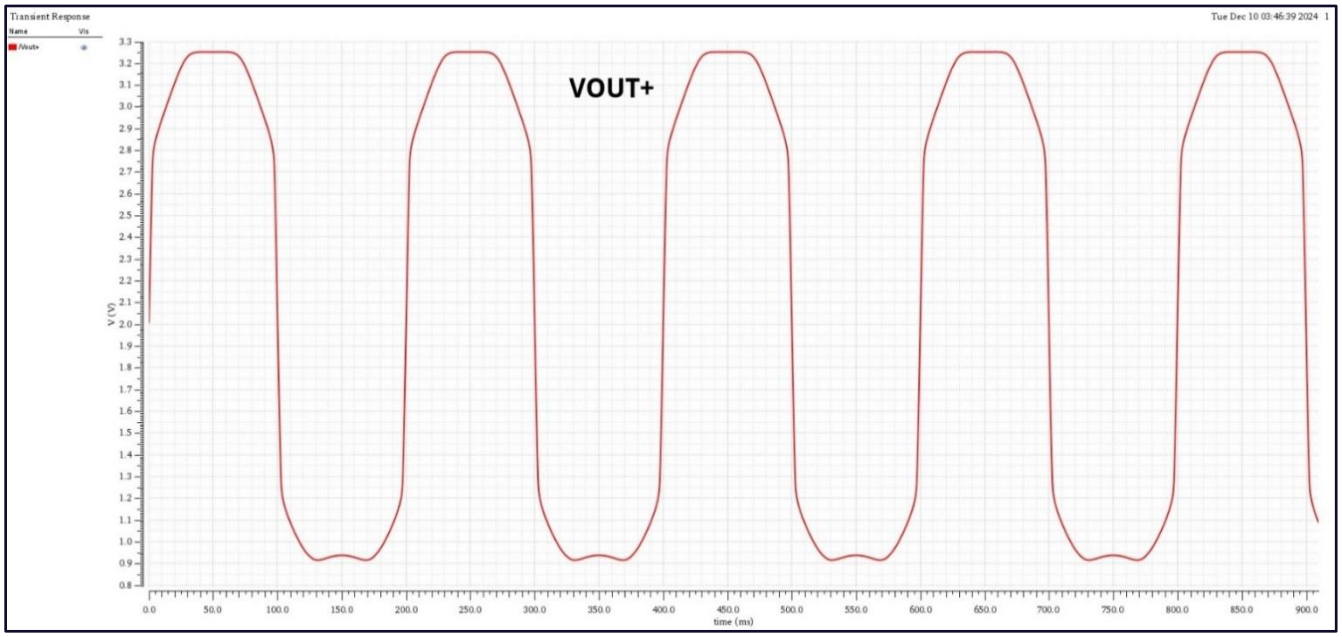


Figure 5: Output from simulation , Voltage of V_{out}+

Output from simulation VOLTAGE V_{OUT-}

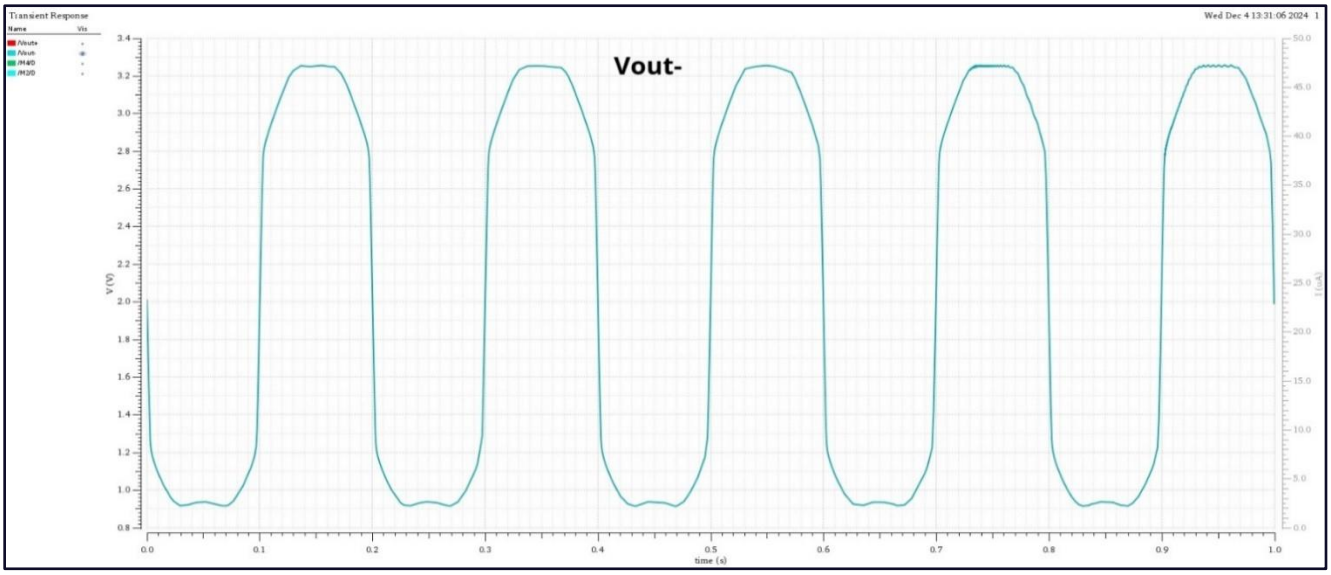


Figure 6: Output from simulation , Current of V_{out} -

iii. Show the voltage of **V_{out}** differential across time

Equations in cadence calculator: VT("/Vout+") - VT("/Vout-")	$V_{outdiff} = V_{out+} - V_{out-}$

Output from simulation :$V_{outdiff}$

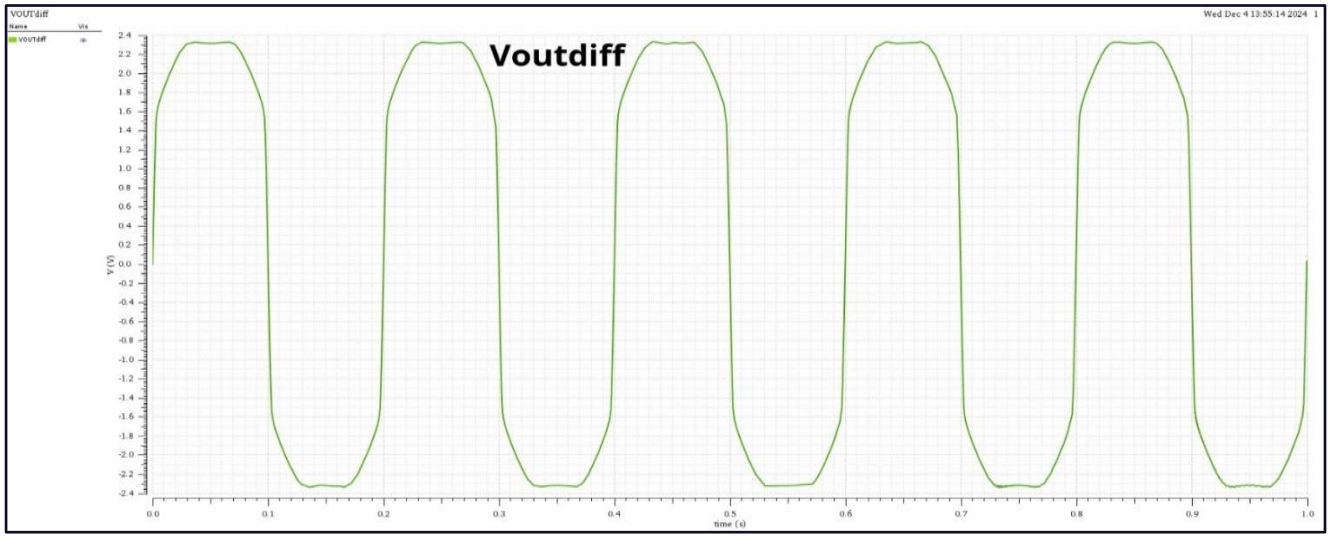


Figure 7: $V_{outdiff}$ from simulation

iv. Calculate the output swing

Equations in cadence calculator: ymax(VT("/Vout+") - VT("/Vout-")) - ymin(VT("/Vout+") - VT("/Vout-"))	$OUTPUT\ SWING = MAX\ PEAK\ (V_{outdiff}) - MIN\ PEAK(V_{outdiff})$ $OUTPUT\ SWING = 4.679\ V$

Hand solution: Max Swing $=2 * (V_{cm\_max} - V_{cm\_min})$, $V_{cm\_max} = VDD = 3.3\ V$

$$V_{cm\_min} = V_{cm} - V_{th} = 1.5 - 0.3359 = 1.164\ V$$

$$\text{Max Swing} = 2 * (3.3 - 1.16) = 4.3\ V$$

Output from simulation

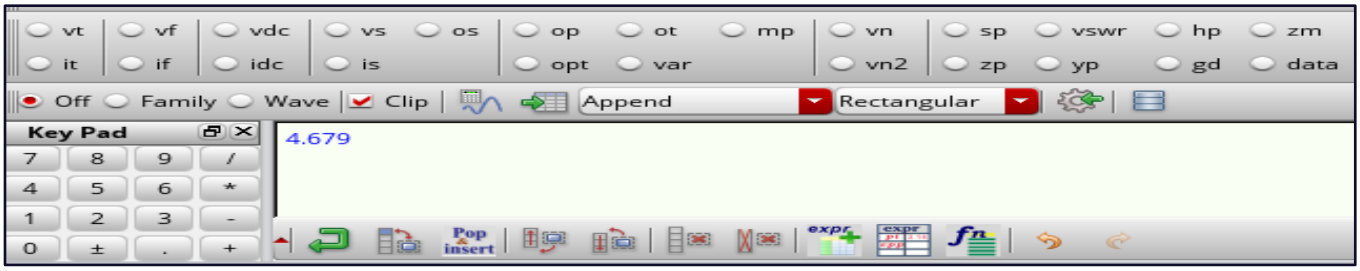


Figure 8: output swing from simulation

c. Run AC simulations (show equation for every requirement , how you get the results in cadence and the simulation setup)

Hand Analysis of this part are done by applying **half circuit concept.**

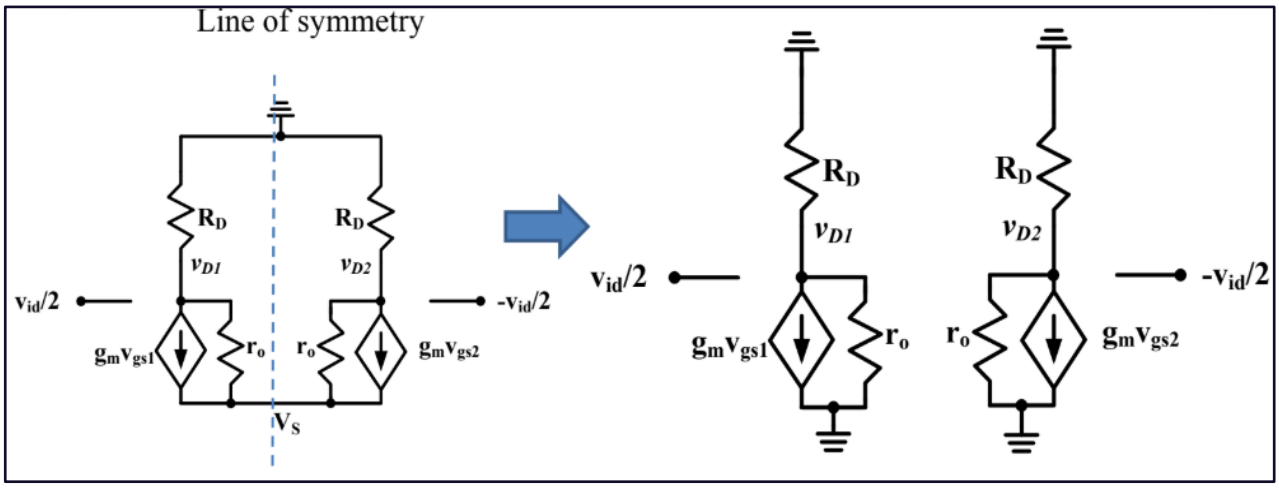


Figure 9: half circuit concept

Let

$$V_{d1} = V_{out-} \;\&\; V_{d2} = V_{out+}$$

Values taken from simulation

$$g_m = 0.00046\ A/V$$
$$r_{o1} = 294.655\ Kohm$$
$$r_{os} = 722.482\ Kohm$$

By applying half circuit concept

$$V_{d1} = V_{out-} = g_m * (R_D \,\backslash\backslash\, r_{o1}) * \frac{v_{id}}{2} = 9.83\ volt$$
$$V_{d2} = V_{out+} = g_m * (R_D \,\backslash\backslash\, r_{o1}) * \frac{-v_{id}}{2} = -9.83 volt$$

By adding the source resistance in consideration so it converted to 2 common source amplifiers with source resistance degeneration but because of odd symmetry $\boldsymbol{V_S = 0}$ a virtual ground in parallel with $\boldsymbol{R_{SS}}$ so it will be cancelled so

$$\mathbf{A_{diff-diff}} = \frac{\boldsymbol{V_{out-} - V_{out+}}}{\boldsymbol{v_{id}}} = \frac{\mathbf{9.83\ -(-9.83\ )}}{\mathbf{1}} = \mathbf{19.66}$$

$$\mathbf{A_{diff\ -CM}} = \frac{\frac{\boldsymbol{V_{out-}+V_{out+}}}{\mathbf{2}}}{\boldsymbol{v_{id}}} = \frac{\boldsymbol{-g_m(R_D \setminus\setminus\ r_{o1}) + g_m(R_D \setminus\setminus\ r_{o1})}}{\mathbf{2 * 1}} = \mathbf{0}$$

The same in the case of the Common mode input voltage signal but here is an even symmetry and $\boldsymbol{V_S}$ not equal zero so $\boldsymbol{R_{SS}}$ will be taken in consideration

$$\boldsymbol{R_{SS} = r_{os} =\ 722.482\ Kohm}$$

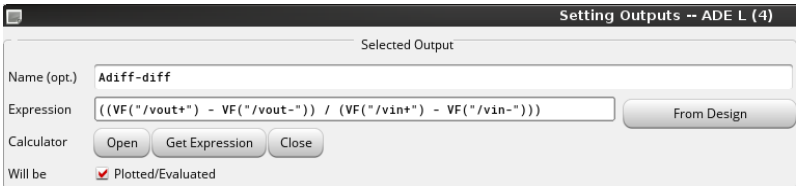
$$\boldsymbol{V_{d1} = V_{d2} = V_{out-} = V_{out+} = \frac{g_m(R_D \setminus\setminus\ r_{o1})}{1 + 2g_mR_{ss}} * V_{CM}}$$

$$\boldsymbol{= 0.0298\ volts}$$

$$\mathbf{A_{CM-diff}} = \frac{\boldsymbol{V_{out-} - V_{out+}}}{\boldsymbol{v_{CM}}} = \frac{\boldsymbol{g_m(R_D \setminus\setminus\ r_{o1})}}{\boldsymbol{1 + 2g_mR_{ss}}} - \frac{\boldsymbol{g_m(R_D \setminus\setminus\ r_{o1})}}{\boldsymbol{1 + 2g_mR_{ss}}} = \mathbf{0}$$

$$\mathbf{A_{CM-CM}} = \frac{\frac{\boldsymbol{V_{out-}+V_{out+}}}{\mathbf{2}}}{\boldsymbol{v_{CM}}} = \frac{\boldsymbol{V_{out+}}}{\mathbf{1}} = \mathbf{29.8\ m}$$

1-Get $\boldsymbol{A_{diff-diff}}$

Equation in cadence calculator:	
	$\mathbf{A_{diff-diff}} = \frac{\boldsymbol{V_{out+} - V_{out-}}}{\boldsymbol{V_{in+} - V_{in-}}} = \mathbf{19.64}$

Output from simulation:

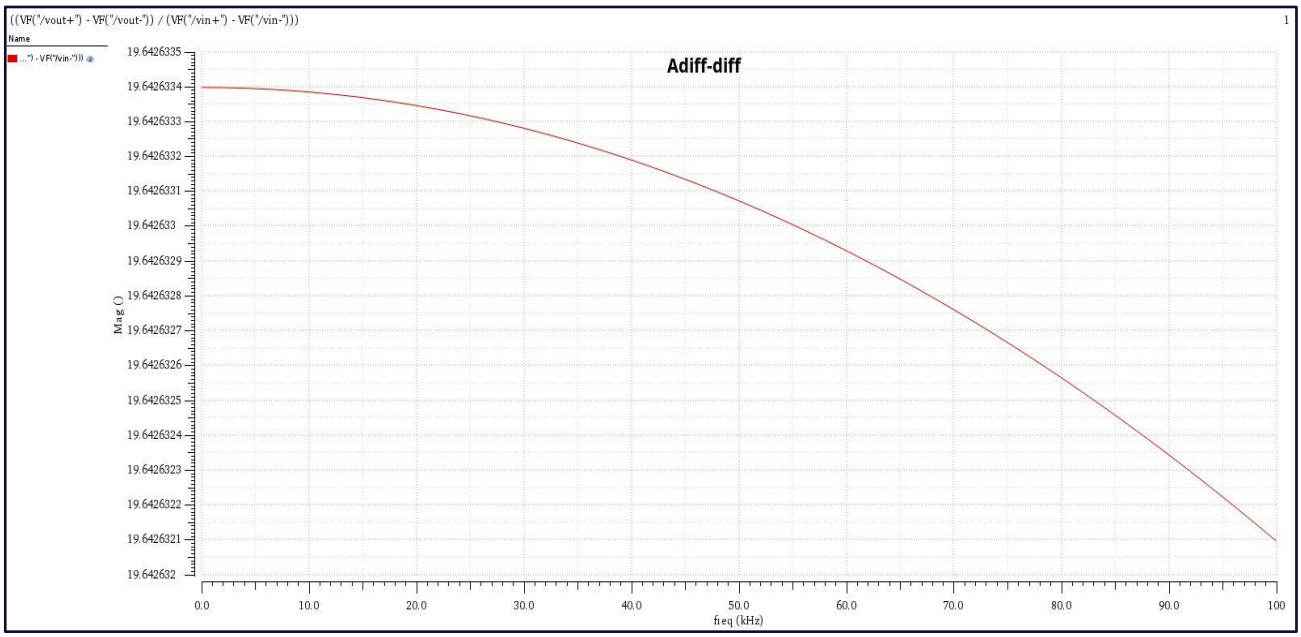
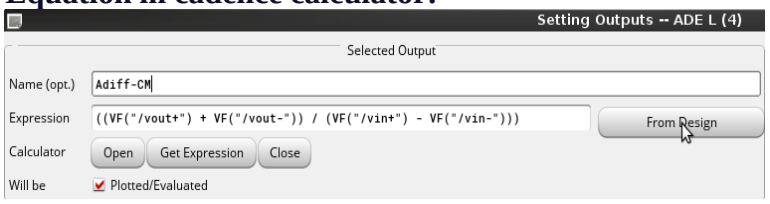


Figure 10: $A_{diff-diff}$ from simulation

2- Get $A_{diff-CM}$

Equation in cadence calculator:



$$A_{diff-CM} = \frac{V_{out+} + V_{out-}}{2 \cdot (V_{in+} - V_{in-})} = 0$$

Output from simulation:

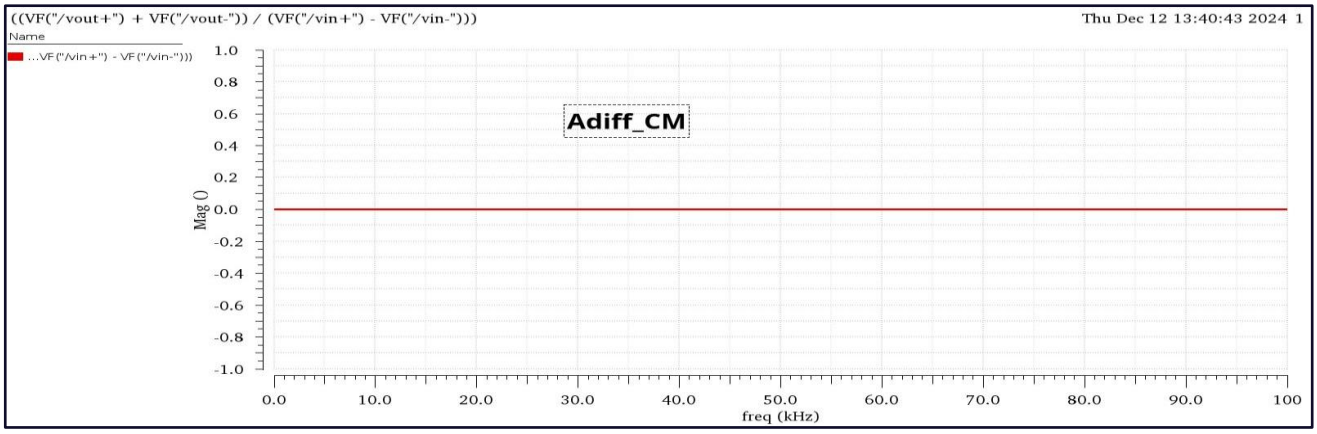
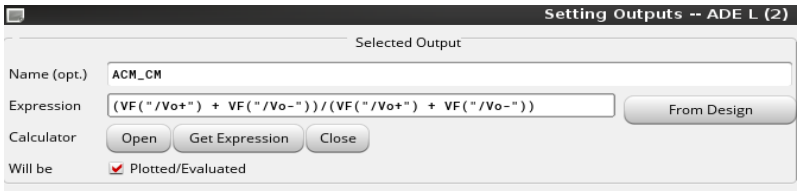


Figure 11: $A_{diff-CM}$ from simulation

3-Get A_{CM-CM}

Equation in cadence calculator:



$$A_{CM-CM} = \frac{V_{out1} + V_{out2}}{V_{in1} - V_{in2}} = 34.36m$$

Output from simulation

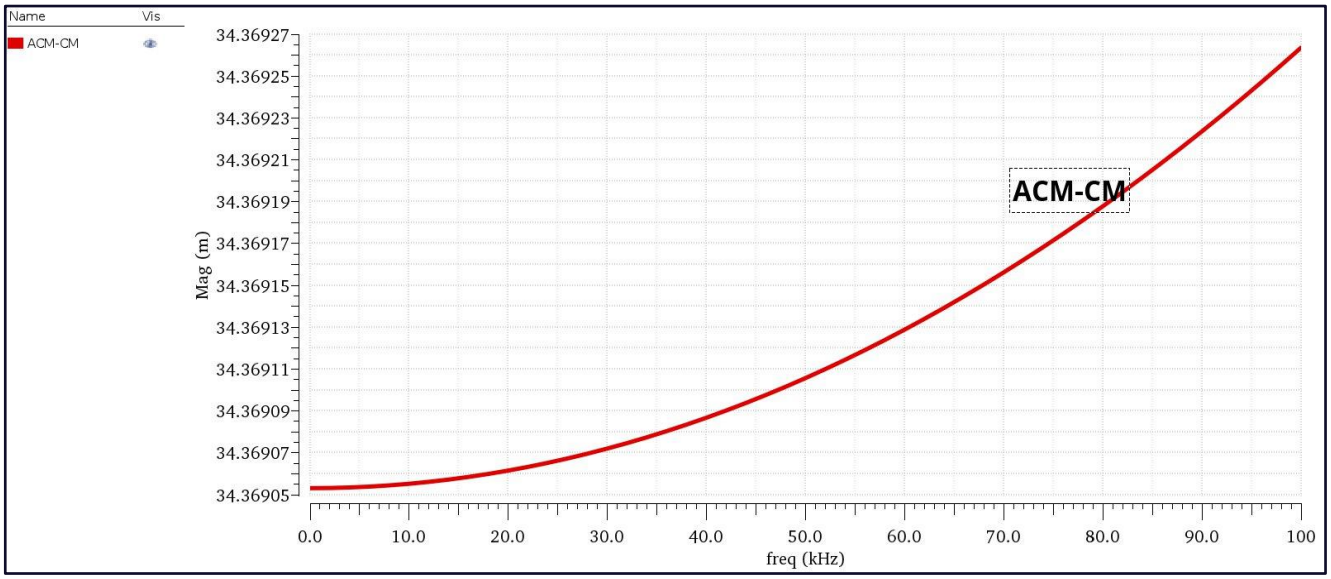
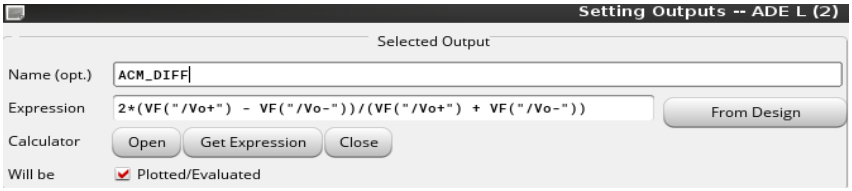


Figure 12: A_{CM-CM} from simulation

4. Get $A_{CM-diff}$.

Equation in cadence calculator:



$$A_{CM-diff} = \frac{V_{out1} - V_{out2}}{V_{in1} + V_{in2}} = 0$$

Output from simulation:

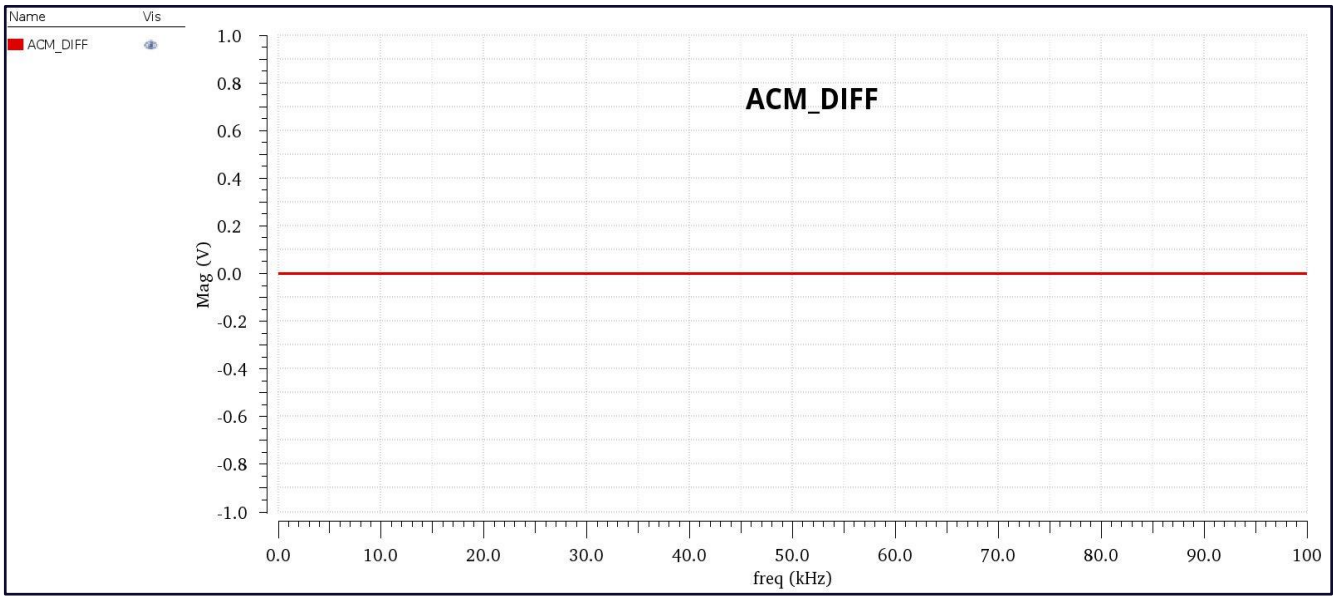
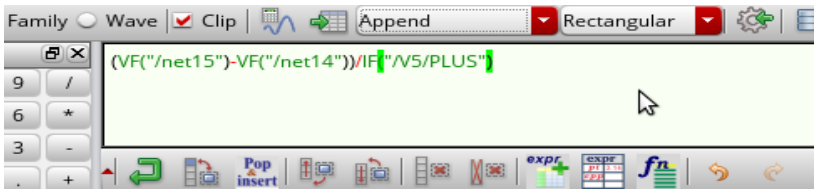


Figure 13: $A_{CM-diff}$ from simulation

5-CMRR

$$CMRR = \frac{Adiff\_diff}{Acm\_diff} \approx \infty$$

6-$R_{OUT-diff}$:

Equation in cadence calculator:	
	$R_{out-diff} = \frac{V_{out-diff}}{I_{out-diff}} = 85.43k\Omega$

- Output resistance (R_{out})is defined as:

$$Rout\_diff = (Vout\_diff)/(Iout\_diff) = 85.43k\Omega$$

- $Vout\_diff$ is the differential-mode output voltage, which in this case is approximated by $VF("/net15") - VF("/net14")$ (the voltage difference across the two outputs).
- $Iout\_CM$ is the differential-mode output current, which flows through the DC source $V5$, represented by $IF("/V5/PLUS")$.
- We used the following expression in the Cadence Calculator:

$$(VF("/net15") - VF("/net14"))/(IF("/V5/PLUS"))$$

- Here's what each term represents:
  - $VF("/net15")$: $+Vout$
  - $VF("/net14")$: $-Vout$
  - $IF("/V5/PLUS")$: The current flowing through the DC voltage source $V5(V_{out})$.
- The expression calculates the ratio of the voltage difference across the two output nodes to the current through the DC source, **differential output resistance** $R_{out-diff}$.

Output from simulation:

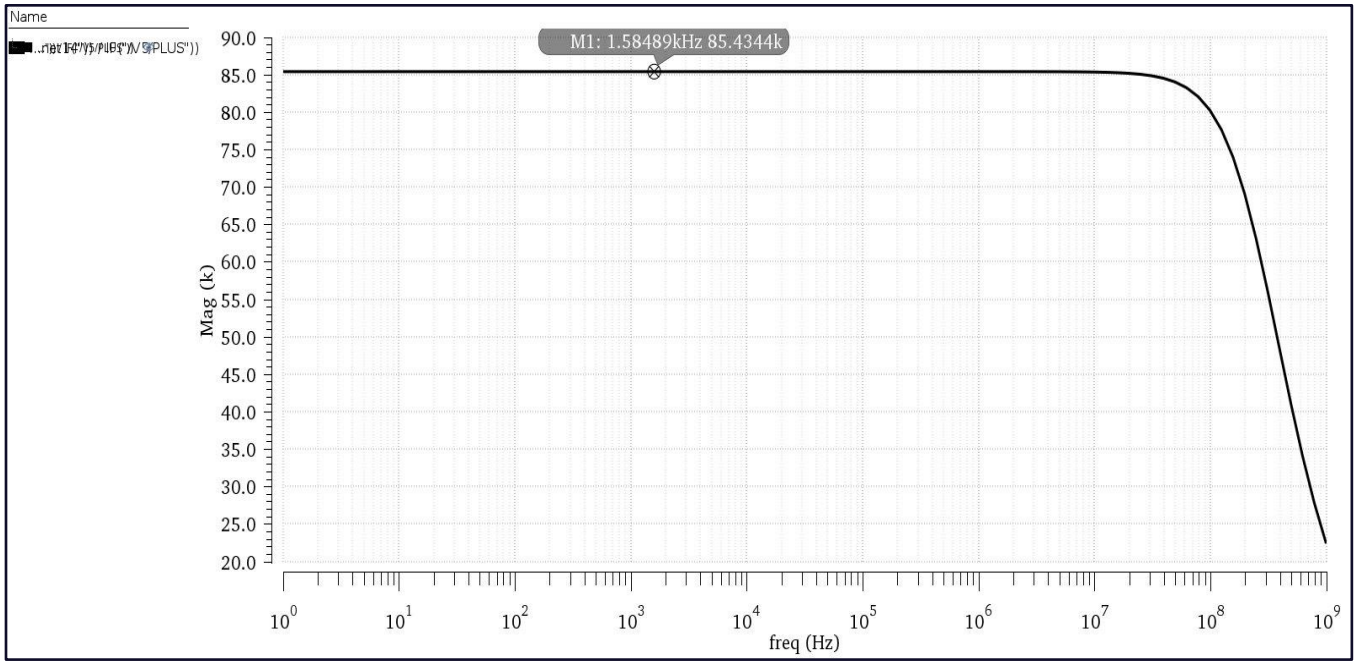
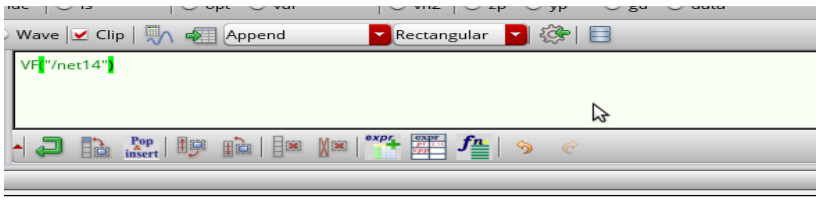


Figure 14: $R_{OUT-diff}$ from simulation

7-R_{OUT-CM}

Equation in cadence calculator:	
	$R_{out-CM} = \frac{V_{out-CM}}{I_{out-CM}} \approx \frac{R_1}{2} = 24.9699k\Omega$

$$R_{out-CM} = 24.9699\ k\Omega$$

- Output resistance ($Rout$)is defined as:

$$R_{out-CM} = \frac{V_{out-CM}}{I_{out-CM}}$$

- Since the AC magnitude of the current source is 1 A, the voltage at the output node (V_{out})is numerically equal to ($Rout$) directly:

$$R_{out-CM} = V_{out-CM}$$

Note: VF("/net14")= V_{out}

- We used VF("/net14"), which calculates the voltage at the output node net14

1. Because the AC current source is set to 1 A, VF("/net14")directly gives the small-signal **common-mode resistance R_{out-CM}** .

- The plot shows how R_{out-CM}behaves across frequencies, starting flat at low frequencies (~25 kΩ) and decreasing at higher frequencies due to parasitic effects.

Output from simulation:

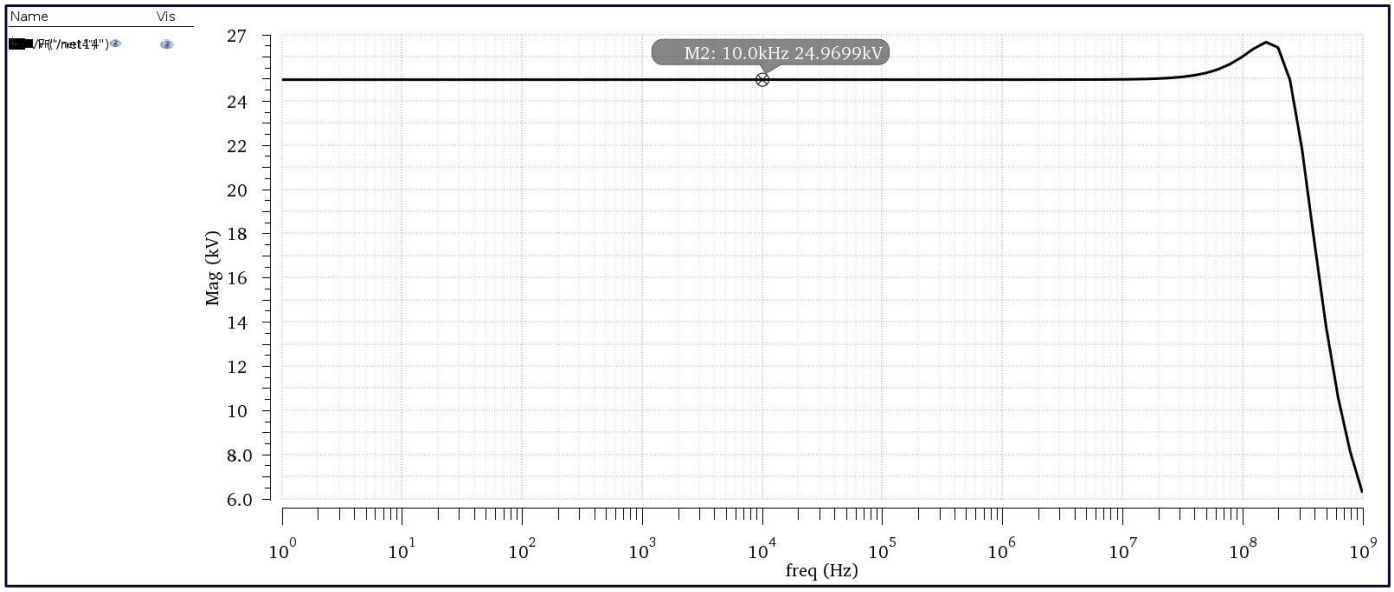


Figure 15: R_{OUT-CM} from simulation

Problem2 Current mirror.

Simulator Circuit:

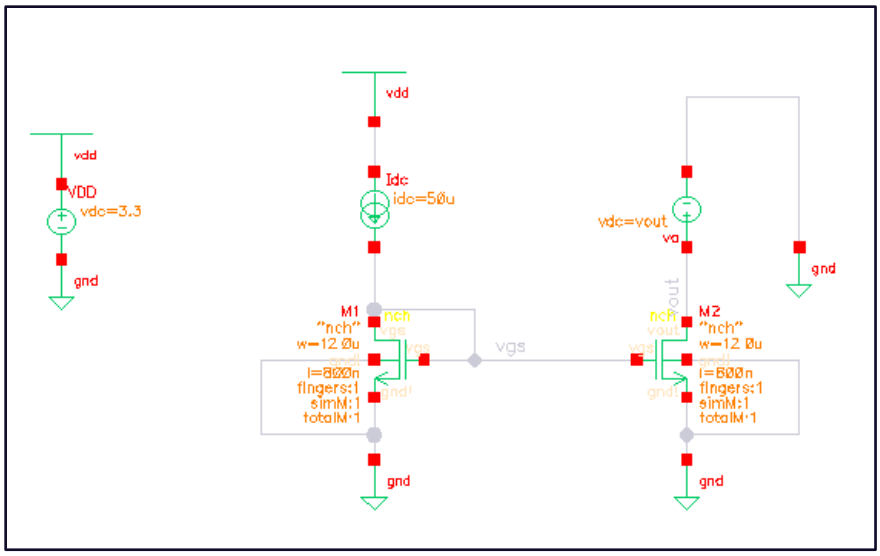


Figure 16: Problem 2 circuit

Part1

Hand analysis:

As D_1 & G_1 are connected so Q_1 will be
In saturation

$$I_{D1} = 0.5 * K_n * (V_{GS1} - V_T)$$

$$V_{GS1} = V_{DS1} = 0.4187\ V$$

$$V_{DSAT} = V_{GS1} - V_T = 0.4187 - 0.3397 = 0.079\ V$$

$$V_{GS1} = V_{GS2}$$

From the concept of current mirroring
Neglecting channel length modulation

$$\frac{I_{OUT}}{I_{REF}} = \frac{\frac{W1}{L1}}{\frac{W2}{L2}} = 1\ ,\ SO\ I_{OUT} = I_{REF} = I_{DC} = 50\ uAmp$$

$$V_{DS2} = V_{OUT} = 2.6\ V$$

As $V_{GS2} > V_T$ And $V_{DS2} > V_{GS2} - V_T$ Q_2 is in saturation
As $V_{GS1} = V_{GS2}$ And $V_{T1} = V_{T2}$

$$V_{DSAT1} = V_{DSAT2} = 0.079\ V$$

$$Relative\ Current\ Error = \frac{I_{OUT} - I_{REF}}{I_{REF}} \times 100$$

From hand analysis:

$$\boldsymbol{Relative\ Current\ Error = 0}$$

From simulation:

$$\boldsymbol{V_{GS1} = V_{DS1} = V_{GS2} = 0.4187}$$
$$\boldsymbol{V_{DSAT1} = V_{DSAT2} = 0.1187\ V}$$
$$\boldsymbol{V_{DS2} = 2.6\ V}$$
$$\boldsymbol{I_{OUT} = 59.69\ uA}$$
$$\boldsymbol{I_{REF} = 50.2\ uA}$$

$$\boldsymbol{Relative\ Current\ Error = \frac{59.69 - 50.2}{50.2} \times 100 = 18.9\%}$$

Part2

1)

Output from simulation:

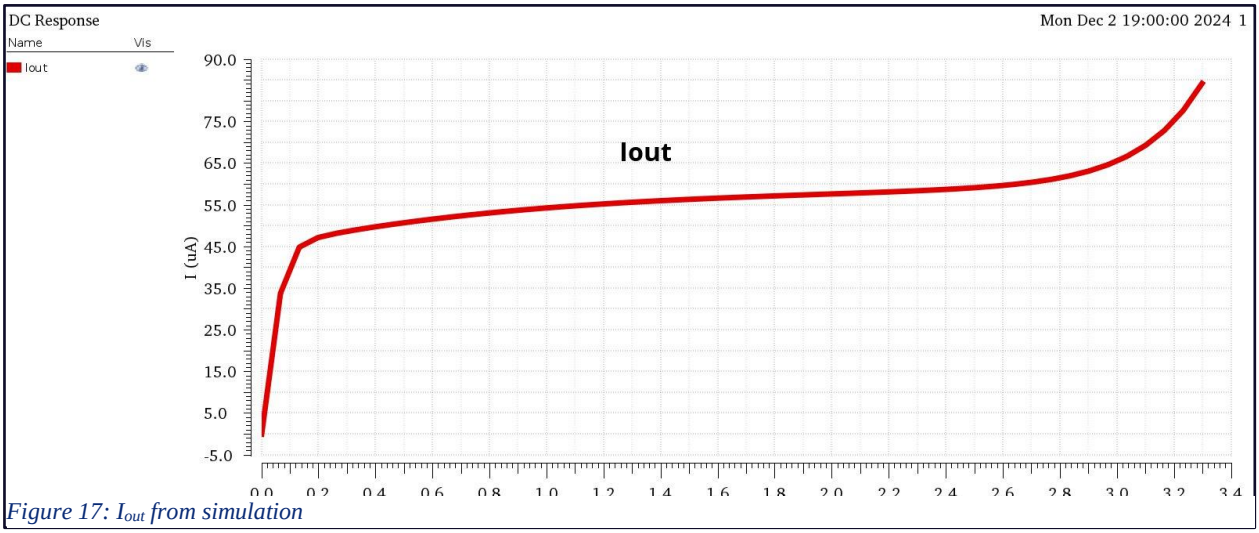


Figure 17: I_{out} from simulation

Observation:

Slight increasing in output voltage (V_{out}) will set Q_2 initially in triode region such as the transistor reacts as a resistor so output current (I_{out}) has a linear relation with output voltage (I_{out})), then after a specific voltage known as overdrive voltage Q_2 gets in saturation such as current is kept constant while increasing voltage but as a result of channel length modulation there is a small increase in output current, And with the increase of the output voltage the transistor fall in break down region in which it lose its characteristics.

2)

Output from simulation:

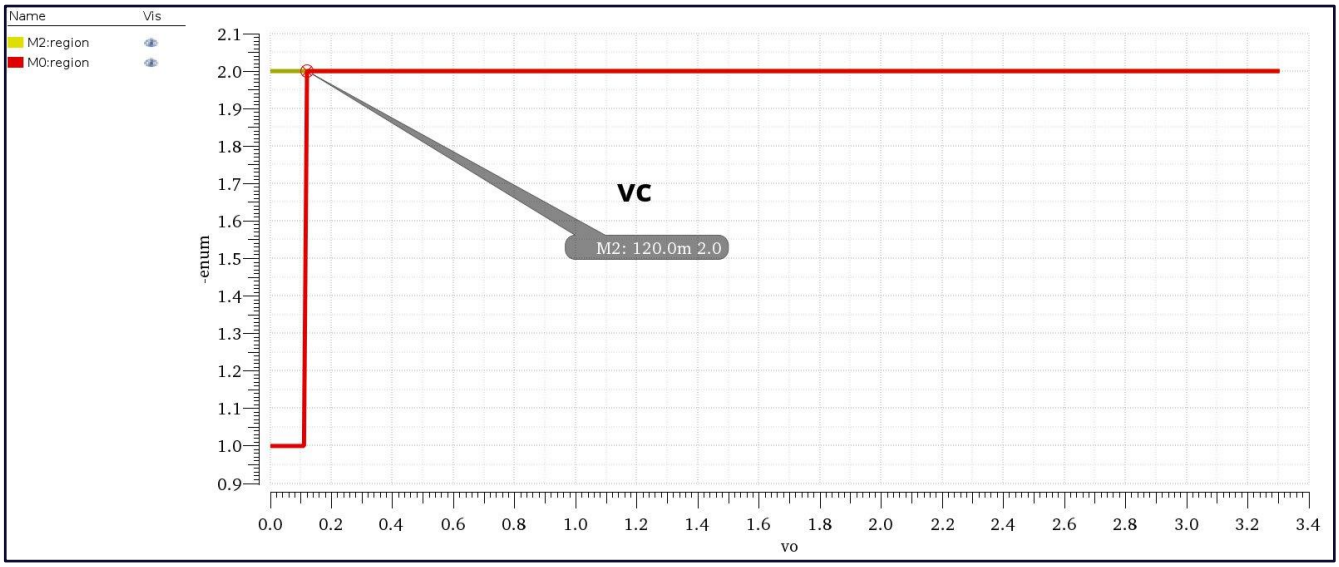


Figure 18: V_c from simulation

Comments:

Compliance voltage from its definition is the minimum voltage to derive the current mirror in a right way which gives approximately a constant current.

From simulation we found that

compliance voltage = 120m V

, after this value the transistor $\boldsymbol{Q_2}$ will be in saturation and work as ideal current mirror

3)

The overdrive voltage is the minimum voltage that makes $\boldsymbol{Q_2}$ saturation.

We neglect $\mathbf{Q_1}$ as its drain and gate are connected so any small voltage will set it in saturation.

Which calculated before from part1

$$\boldsymbol{V_{DSAT}\ from\ dc\ operating\ point = 118\ mV}$$

4)

Output from simulation:

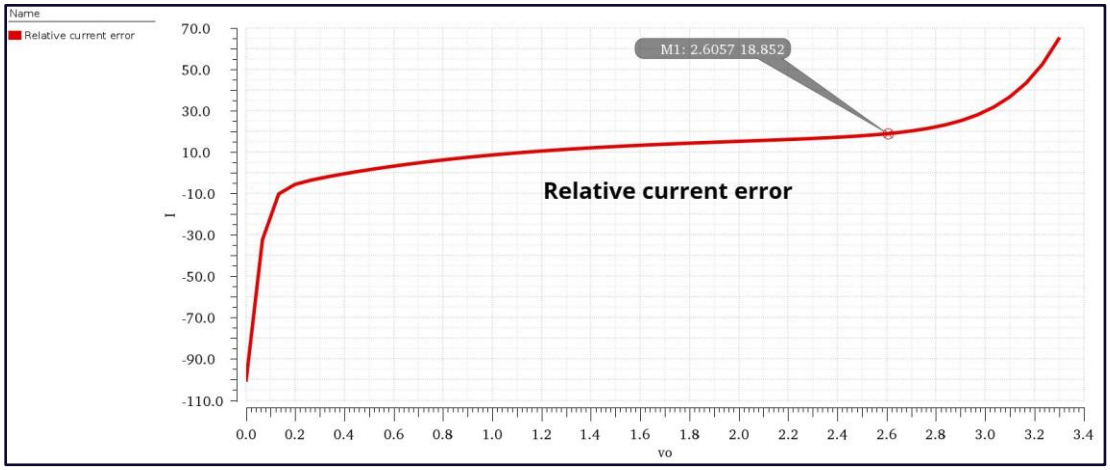


Figure 19: relative current error

$$\boldsymbol{Relative\ Current\ Error} = \frac{\boldsymbol{I_{OUT} - I_{REF}}}{\boldsymbol{I_{REF}}} * \boldsymbol{100} = (\frac{\boldsymbol{I_{OUT}}}{\boldsymbol{I_{REF}}} - \boldsymbol{1}) * \boldsymbol{100}$$

So, it has the Same variation as $\boldsymbol{I_{OUT}}$, but with a different slope and shifted.

5)

Output from simulation:

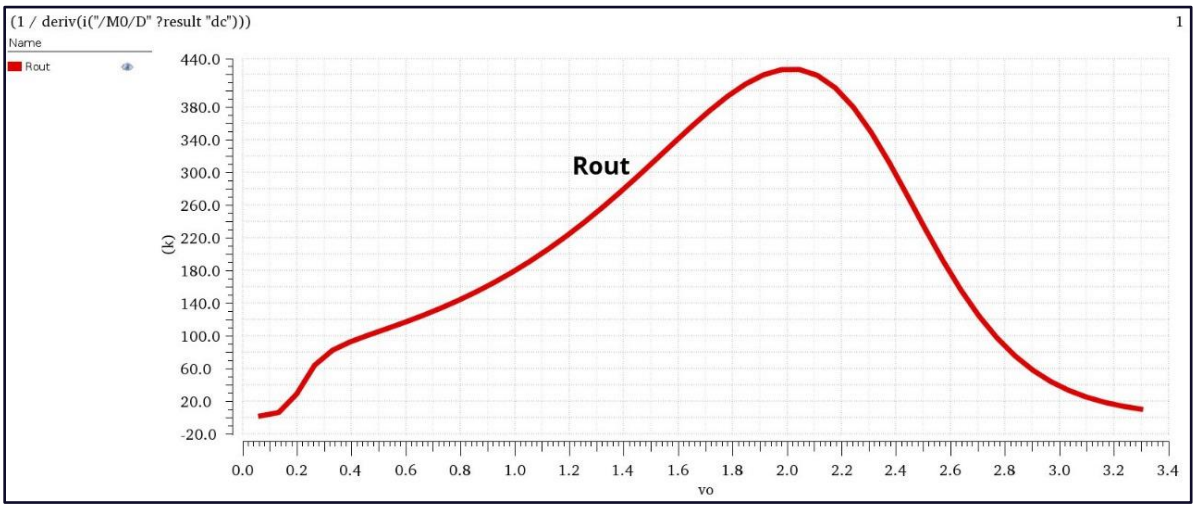


Figure 20: R_{out} from simulation

Comment:

At low V_{ov}values, R_{out} starts low and increases steadily. This could correspond to the saturation of the transistor or the mirror's inability to sustain higher resistance at low output, R_{out} a maximum value at an intermediate V_{ov}, indicating optimal operation of the current mirror at this point. This is where the circuit might achieve the highest output impedance, After the peak, R_{out} begins to drop with further increases in V_{ov} This suggests the circuit enters a region where it can no longer maintain a high impedance, likely due to the transistor moving out of its active region.

Output from simulation:

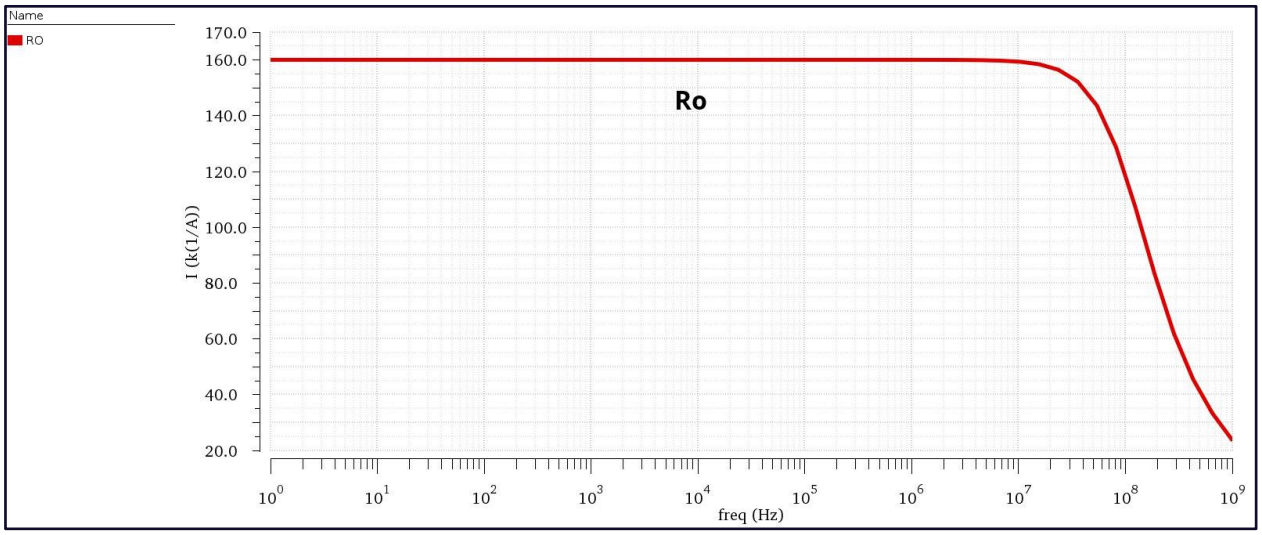


Figure 21: R_0 from simulation

$$\text{At } V_{out} = 2.6\ V$$

$$R_{out} = 160\ Kohm$$

We perform a frequency sweep of R_{out} to identify the frequency at which the influence of the internal capacitance of the transistor becomes significant. This analysis highlights the point where the capacitive effects begin to dominate, impacting the impedance and altering the circuit's performance.

Part3

1- Plot output current vs L :

Output from simulation:

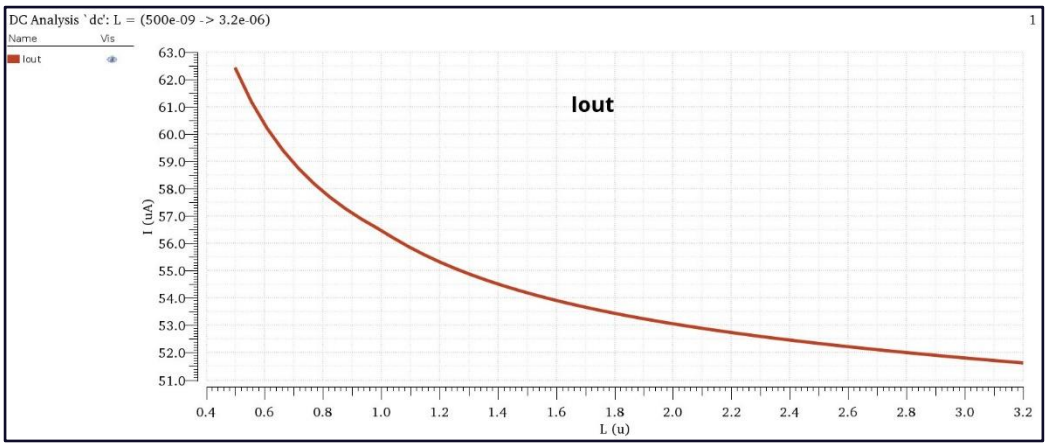


Figure 22: output current vs L

Comment on the results:

$$\frac{I_{OUT}}{I_{REF}} = \frac{\frac{W1}{L1}(1+\lambda V_{ds2})}{\frac{W1}{L1}(1+\lambda V_{ds1})}\ , \qquad \boldsymbol{\lambda \text{ is in an inverse relation with } L}$$

$$V_{ds2} = 2.1\,V \;\&\; V_{ds1} = 0.4\,V$$

So, if we neglected V_{ds1} as it too small compared to V_{ds2} we get that the inverse relation between L and I_{OUT} ,as I_{OUT} direct proportional to λ and as L increases, λ decreases And because it is not an exact linear relation the decreasing in the graph is a curve.

Note that the variation in **L** is the same so λ is the same in the 2 transistors.

2- Use calculator to get relative error :

Output from simulation:

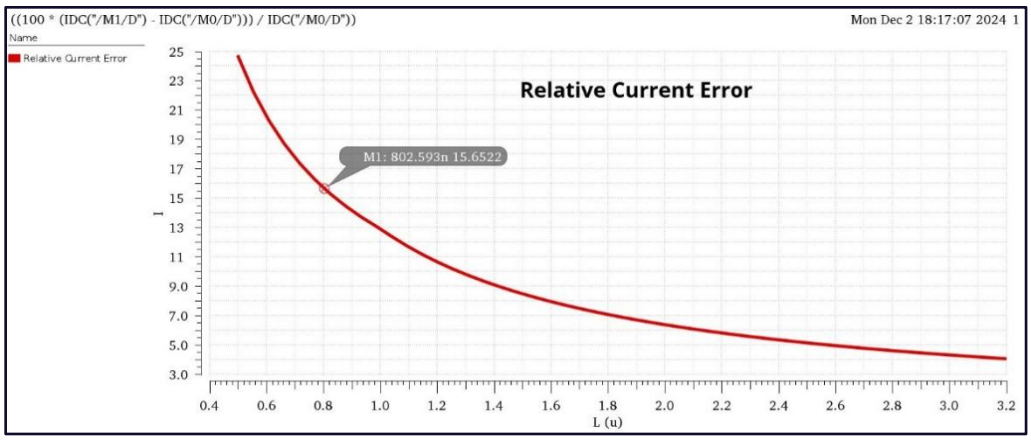


Figure 23:relative error from simulation

Comment:

As L increases the channel length modulation effect decreases so that ,the relative current error decreases as it is easy to know where it could be neglected, And the output current only depends on the input current and there dimensions (**W & L**) .