كلية الهندسة - جامعة الزقازيق

الفرقة: الثالثة هندسة الحاسبات والمنظومات

المقرر: دوائر الحاسب المتكاملة

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الرقم في السكشن: 3

رقم الجروب وإسم الموضوع: Group 5 - Digital Clock

Group 5

Digital Clock Project

Task 1: Timer

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Project Summary:

A project to create a digital clock that displays hours, minutes and seconds in addition to displaying the date (day / month / year).

Components used in the project:

- **NE555** Timer.
- **74LS90** Counter.
- **74LS48** Decoder.
- **7SEG-COM-ANODE** 7 Segment.
- **74LS157** Multiplexer 2 to 1.
- **74S283** 4-Bit Binary Adder

Project completion stages:

- Stage 1: Timer.

At this stage, we need to generate a continuous square wave and this is done by **NE555** timer by connecting it in astable mode, as will be explained later in this report.

- Stage 2: Counter.

At this stage, we need to start counting from 00 to 59 in the seconds and minutes digits, but in the hours digits, we need to count from 1 to

12, and after that a signal comes out to the counter responsible for days.

This is done through the 74LS90 counter which divides the incoming signal whose frequency equals 1 Hz, then divides the signal by 10 in the first digit of the seconds counter, then divides again by 6 in the second digit of the seconds counter and thus we get the numbers from 00 to 59 and similarly in the case of The minutes will take the signal from the second digit of the seconds and then divide it by 10 so that the counter responsible for the minutes starts to count from 0 to 9, then we take a signal from it to divide by 6 so that the counter responsible for the second digit in the minutes starts counting from 0 to 5 and as a result, we get the minutes from 00 To 59.

And by the same principle, we repeat the step on the two-digit hours, so we take a signal from the second digit of the minute counter, then divide it by 10, then the first digit begins to count from 0 to 9 every hour, then we take a sign from it and divide it by 3, so the second digit begins to count from 0 to 2 each 10 hours, and when the clock reaches 12:00:00, the status changes from AM to PM or vice versa, and after an hour the hour counter returns to 01 again.

- Stage 3**:** Decoder & 7 Segment.

At this stage, the pulse is used from the counter to enter the decoder and then to the 7-Segment to be displayed in the time part. In the date part, more logic gates have been added to set the days of the months.

for example, In February only 28 days are displayed. The month of April, June, September and November only 30 days are displayed, and in the remaining months 31 days are displayed.

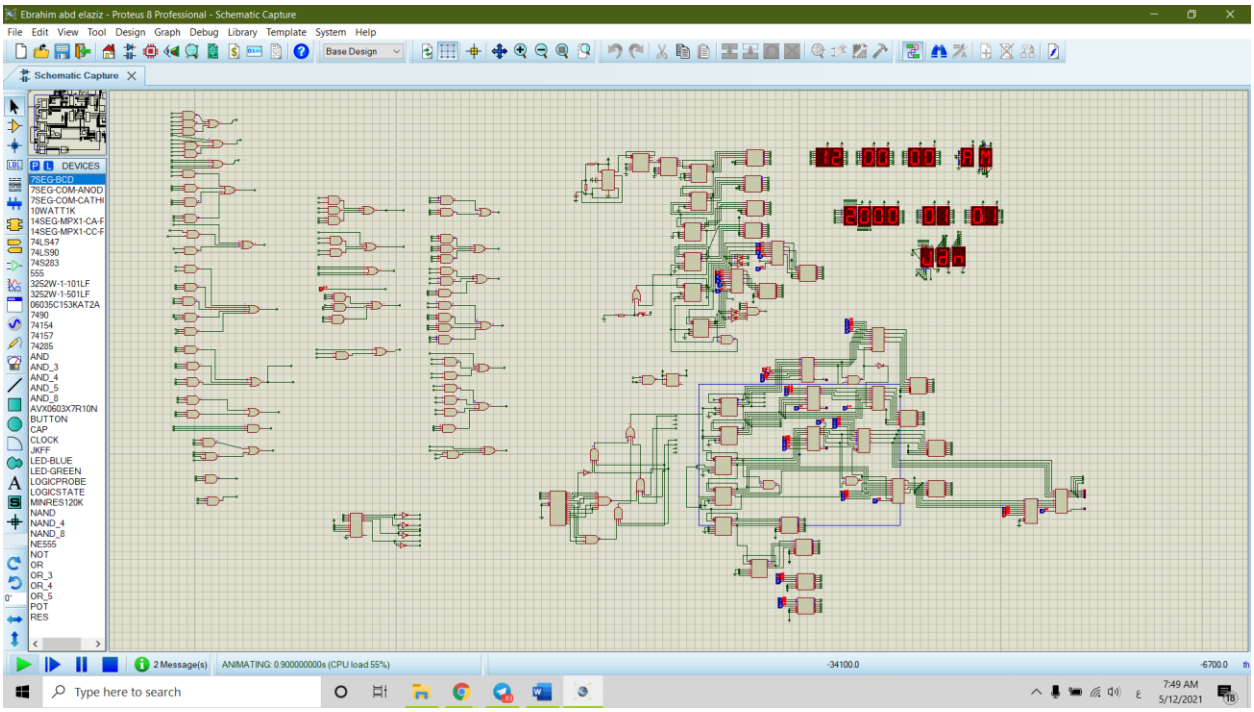
Also, more logic gates have been added, so that the months' abbreviations are displayed on 7-Sigment as they will appear in the Simulation later.

- Stage 4**:** How to handle the Date.

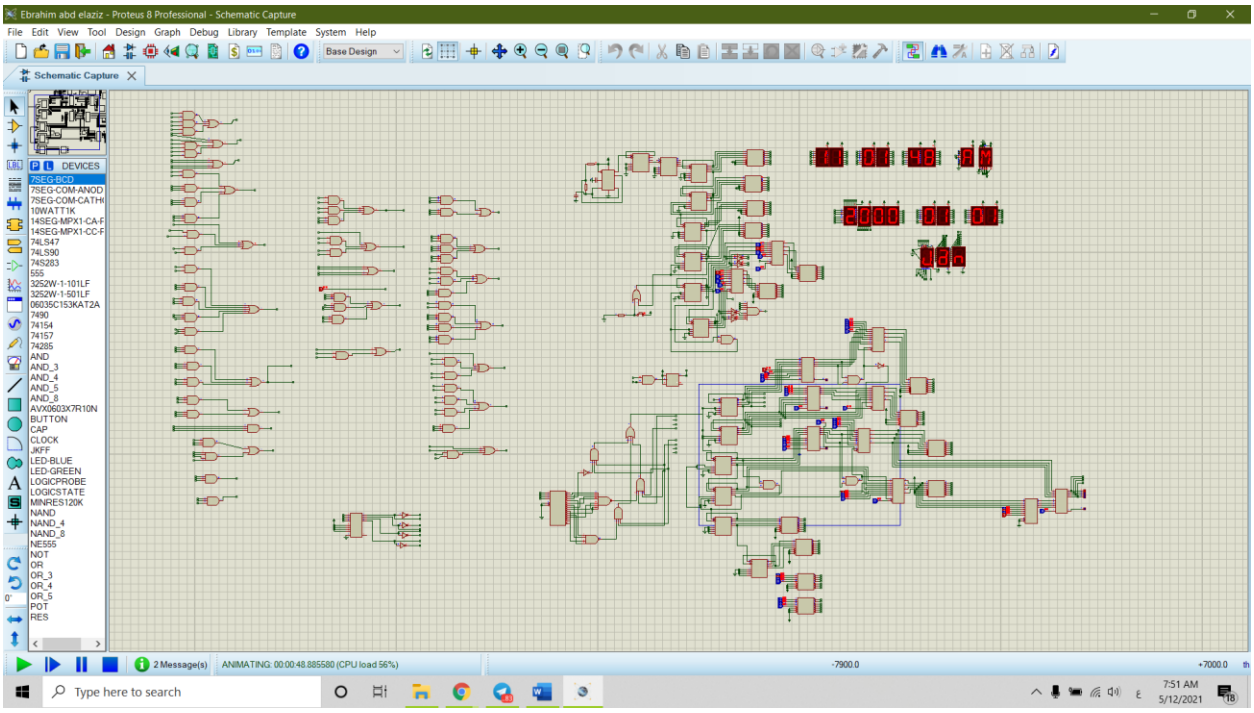
There were some difficulties in this part, which is how to set the counter to start counting from 1 and not from zero in the date part, as there is neither zero day nor zero month, days start from 1 to 30 and months from 1 to 12. Therefore, some components have been added, such as (74LS157 Multiplexer 2 to 1.) and (74S283 4-Bit Binary Adder) and the problem was resolved successfully.

- Stage 5**:** Simulation in Proteus.

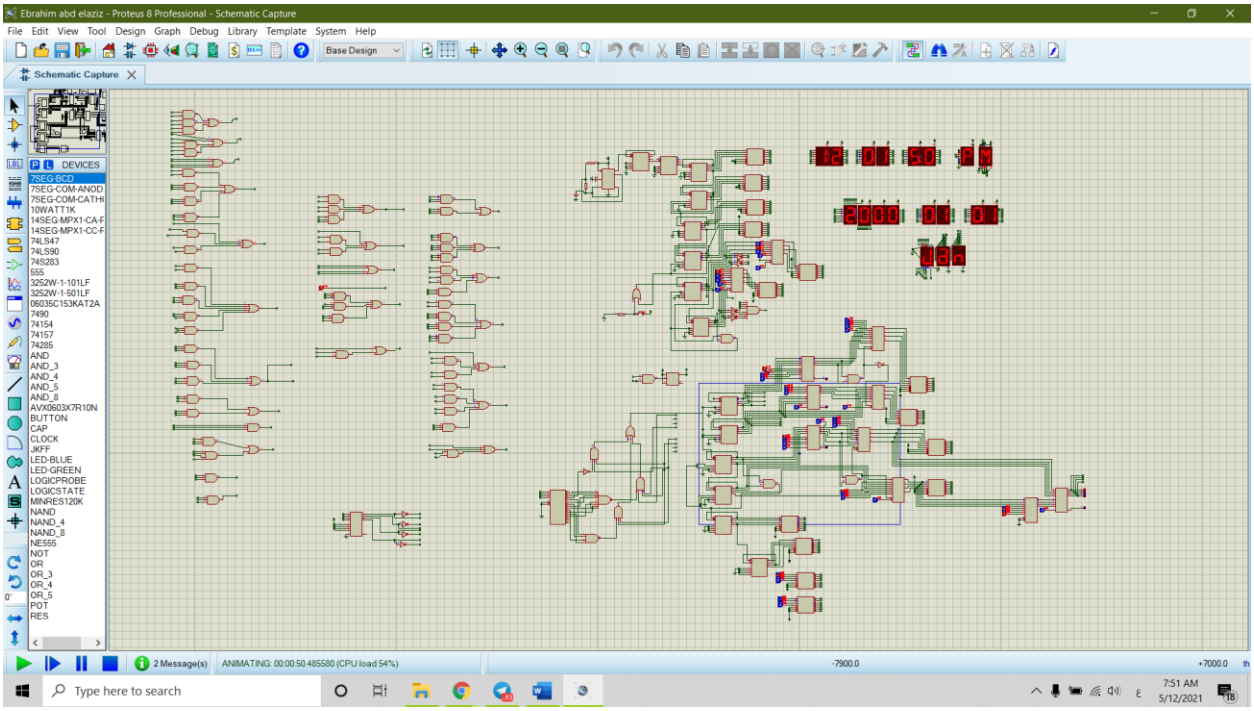
In the first picture it is clear that the time is 12:00:00 AM and the date is 1/1.



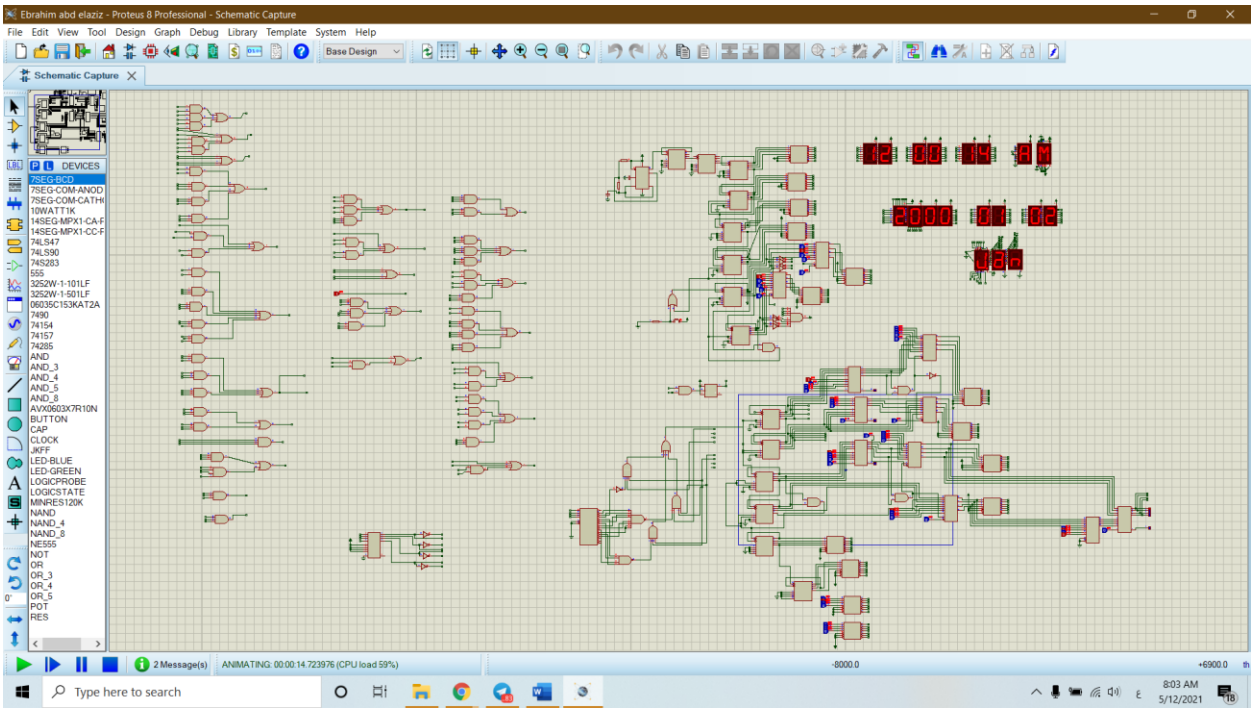
In the second picture, about 11 hours have passed and the AM is still the same, and the date is still 1/1 and there has been no change in it.



After about an hour the AM changed to PM and the date is still the same because not 24 hours have passed, but only 12 hours have passed.



After about 12 hours had passed, the status changed from PM to AM again and the date changed to 1/2.



Task 1: Timer

Components:

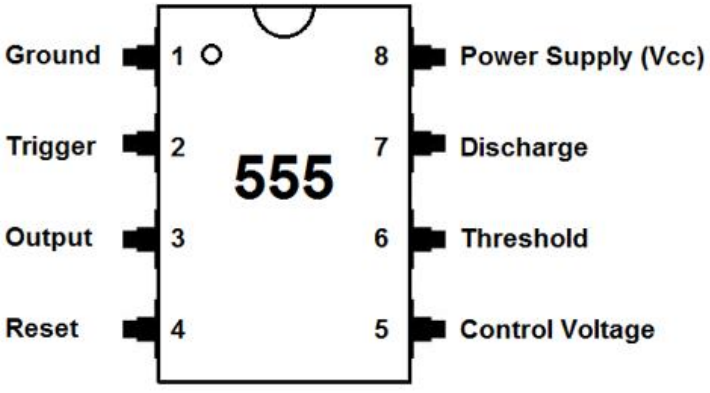
- NE555 IC.
- Resistors R1, R2.
- Capacitor C1.

NE555 IC:

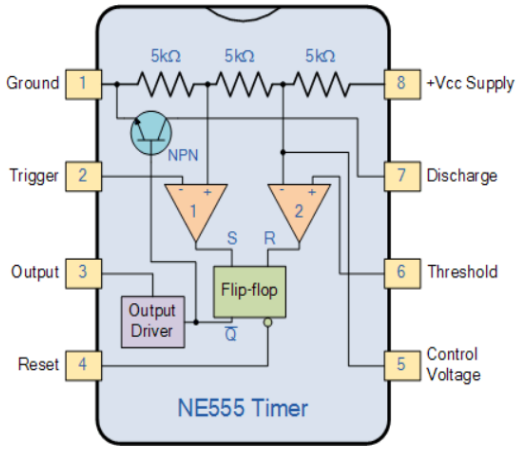
- Pin Connections:

1. Ground
2. Trigger
3. Output
4. Reset

5. Control Voltage
6. Threshold
7. Discharge
8. Vcc



- Block Diagram:



1. 3 Res. 5kΩ

That is why it was called the Timer 555.

2. 2 Op-Amp

The Op-Amp works as a comparator where it compares the value on the negative pin with the value on the positive pin, and if the value on the positive pin is greater than the negative pin, it outputs 1, but if the value on the negative pin is greater than the value on the positive pin, the output is equal to 0.

3. SR flip-flop

When S = 1 and R = 0 that's mean that we are in the state of the **set**.

And if S = 0 and R = 1 so we are in the state od **Reset**.

If S = 0 and R = 0 there is **No Change**.

If S = 1 and R = 1 that's **illegal**.

R	*S*	*Q*
0	0	*NO CHANGE*
0	1	*SET*
1	0	*RESET*
1	1	*ILLEGAL*

4. Not Gate

to invert the output of flip-flop.

5. Transistor

Used to discharge the capacitor through it.

- ELECTRICAL CHARACTERISTICS:

1) VCC = 4.5 to 16 V
2) $I_{source/sink}$ = 200 mA
3) Supply current = up to 15 mA

…

Operation Mode

We should use Astable Mode Which makes the output a continuous square wave, and from data sheet we will know how to make this circuit.

We can get a frequency of 50 Hz by set R1, R 2, and C1 to 830 Ω, 14 kΩ and 1 µF respectively.

We can get the resistance of 830 Ω by connecting 2 resistors 500 Ω and 330 Ω in series.

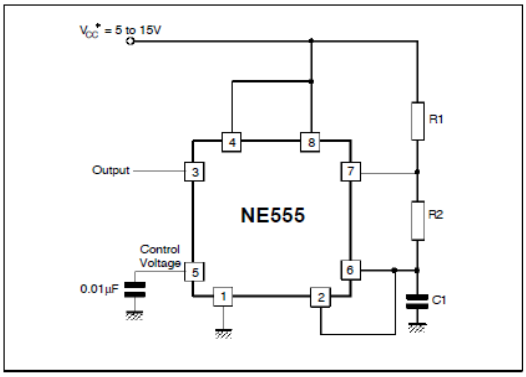


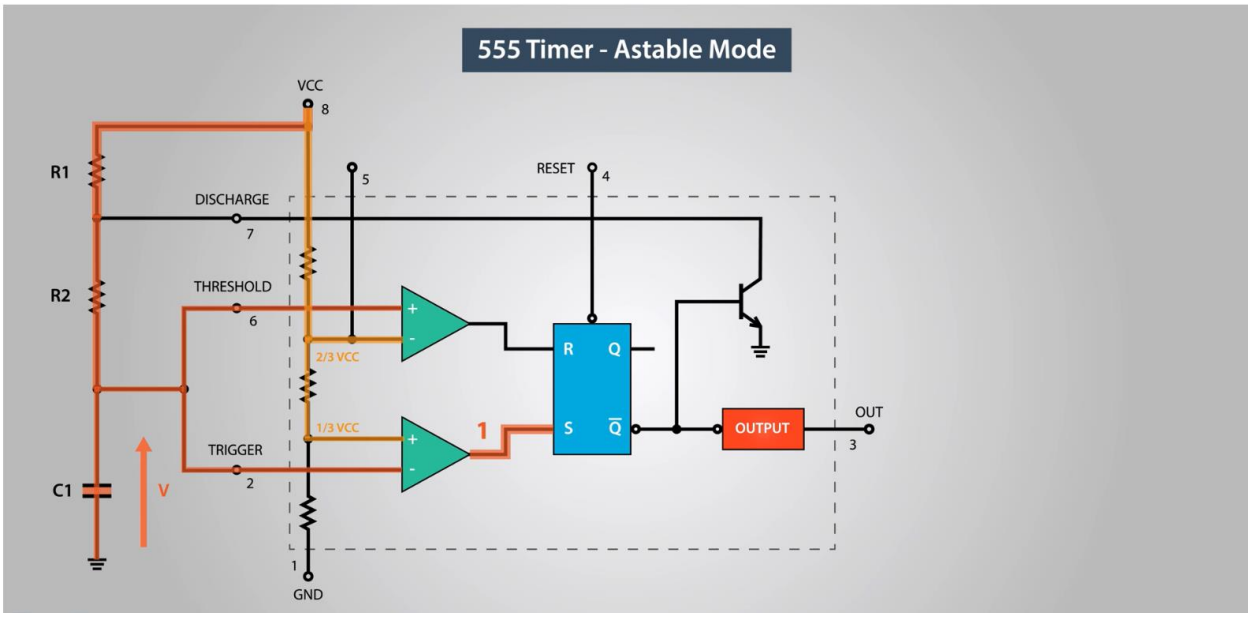
Figure 14 shows actual waveforms generated in this mode of operation.
The charge time (output HIGH) is given by :
$t_1 = 0.693\ (R_1 + R_2)\ C_1$
and the discharge time (output LOW) by :
$t_2 = 0.693\ (R_2)\ C_1$
Thus the total period T is given by :
$T = t_1 + t_2 = 0.693\ (R_1 + 2R_2)\ C_1$
The frequency ofoscillation is them :

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)\ C_1}$$

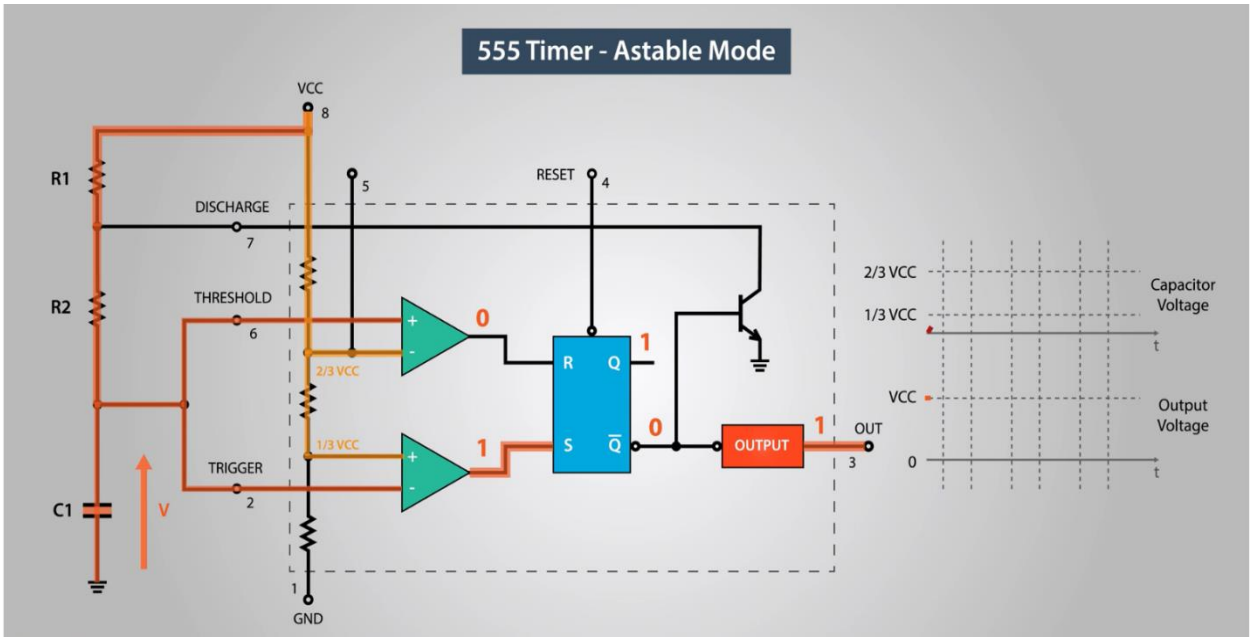
How can we get a square wave?

We should connect the IC NE555 in Astable Mode Which makes the output a continuous square wave.

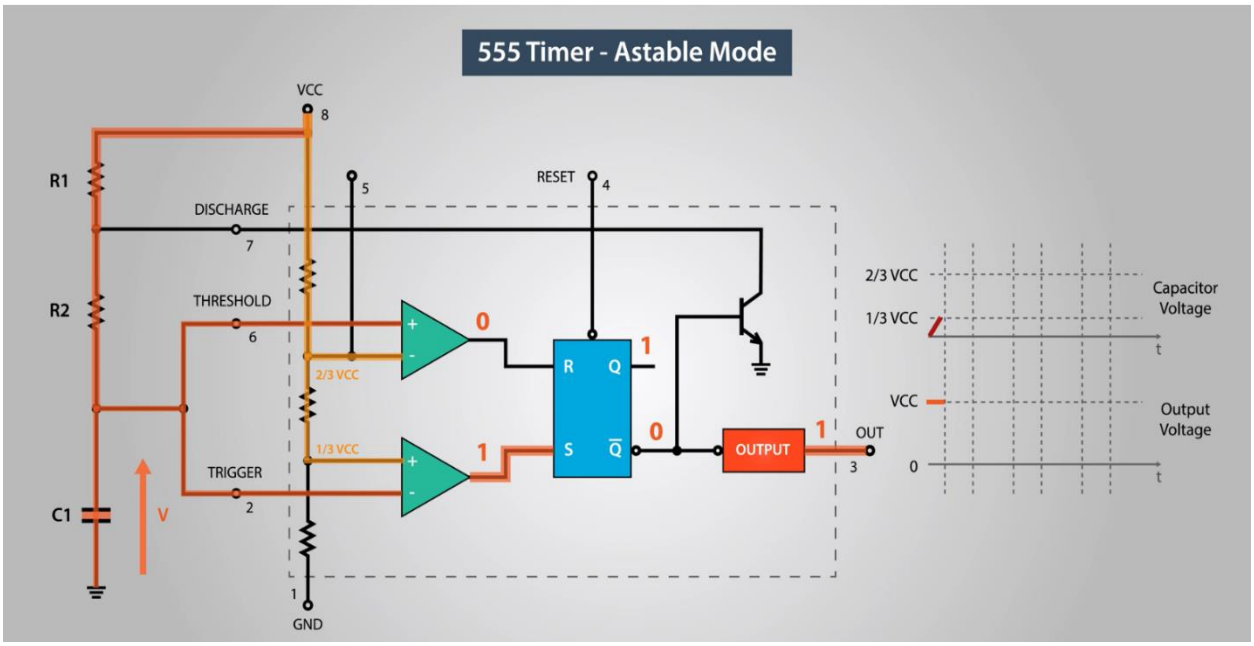
When connected, the capacitor begins to charge, and as long as the capacitor value is still less than the value of 1/3 VCC, the output of the first comparator will be 1 as in the following picture, because the value on the positive pin is greater than the value on the negative pin.



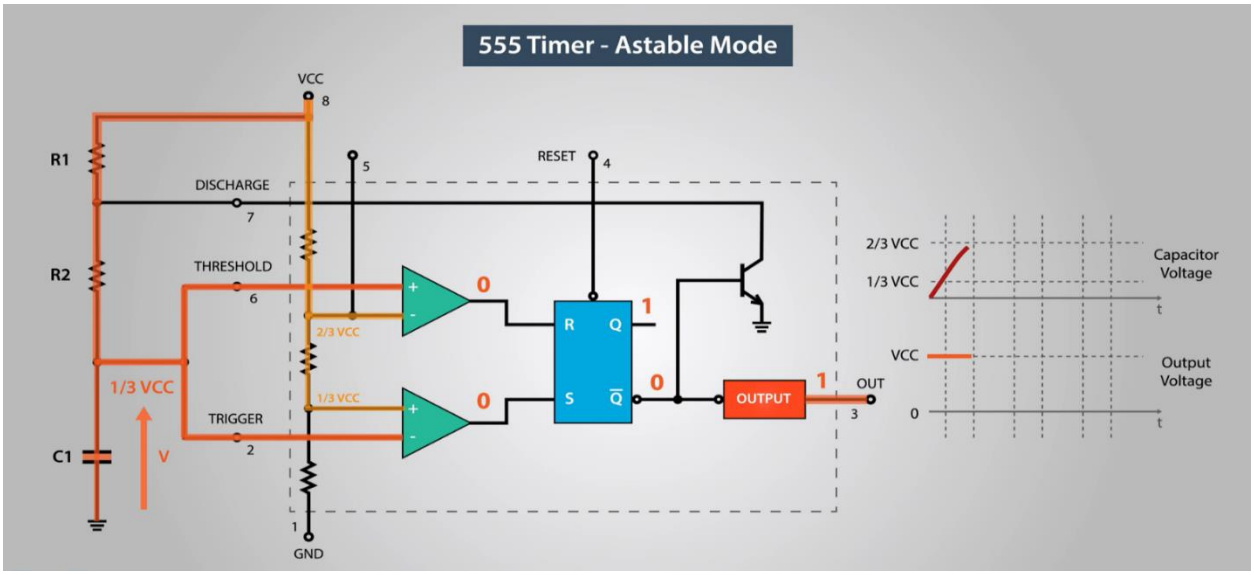
Also, the capacitor value is less than 2/3 of the VCC, so the output of the second comparator will be 0, as in the following picture, because the value on the negative pin is greater than the value on the positive pin.



According to the Truth Table of SR Flip Flops, when S = 1 and R = 0, the output Q = 1 and Q' = 0 and thus the output is = 1 i.e. + VCC, as in the following picture.

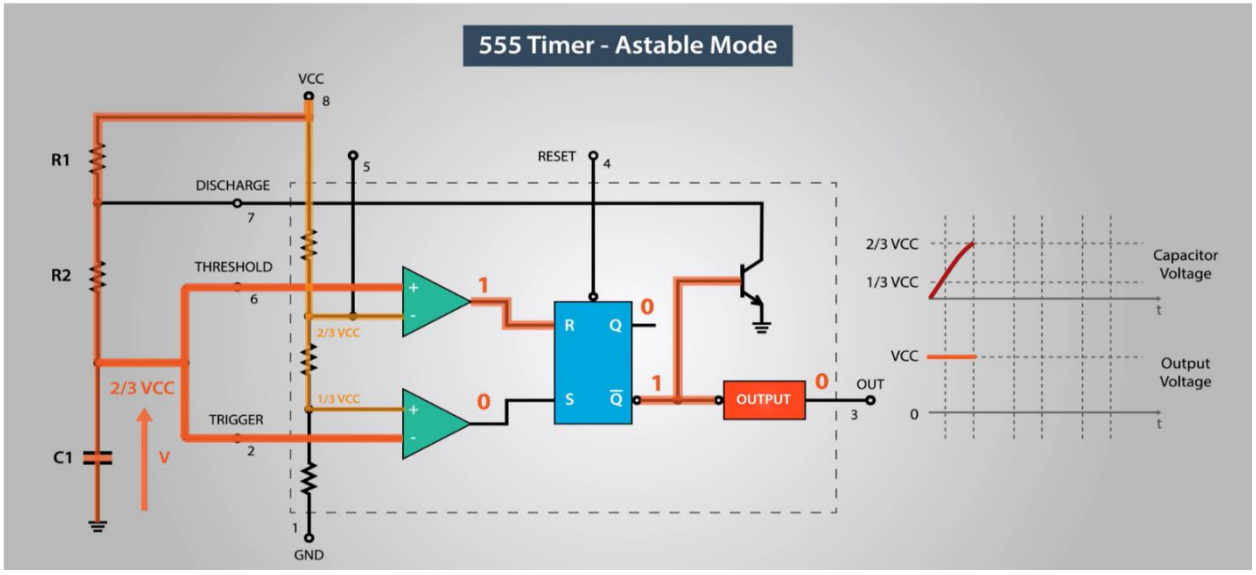


Now the capacitor value has reached 1/3 VCC, but it increases from this value and thus the voltage on the negative pin is greater than the voltage on the positive pin, so the output of the first comparator is = 0, and the output of the second comparator is still = 0 because the voltage on the negative pin is still greater than the voltage on the positive pin, as long as S = 0 and R = 0, then the flip-flop output remains the same.

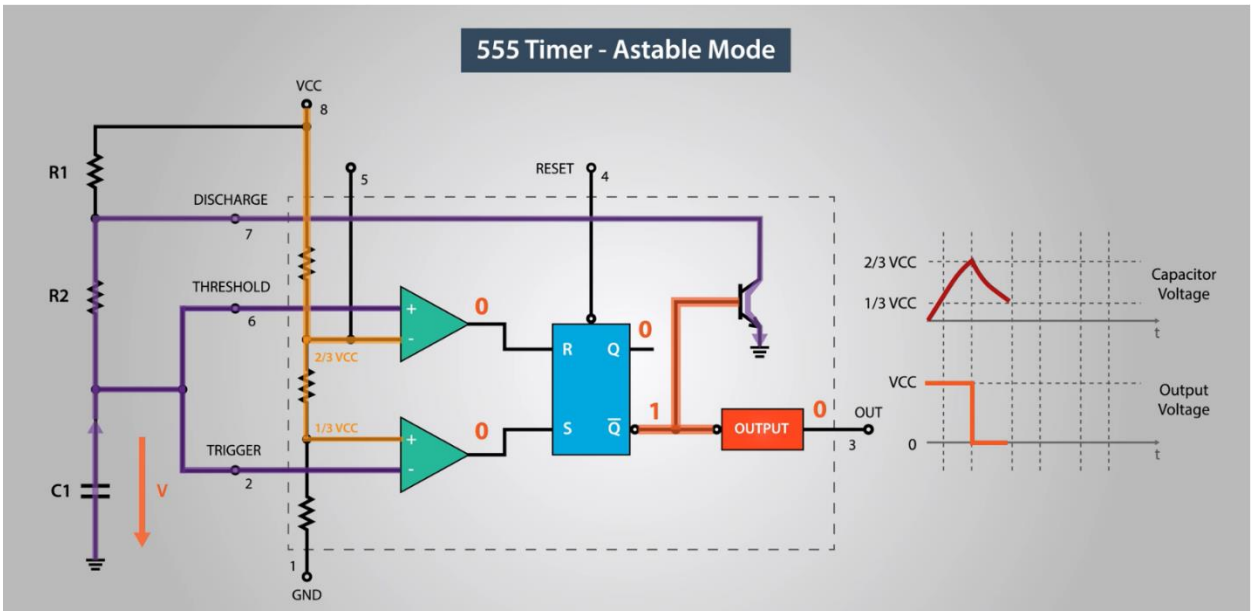


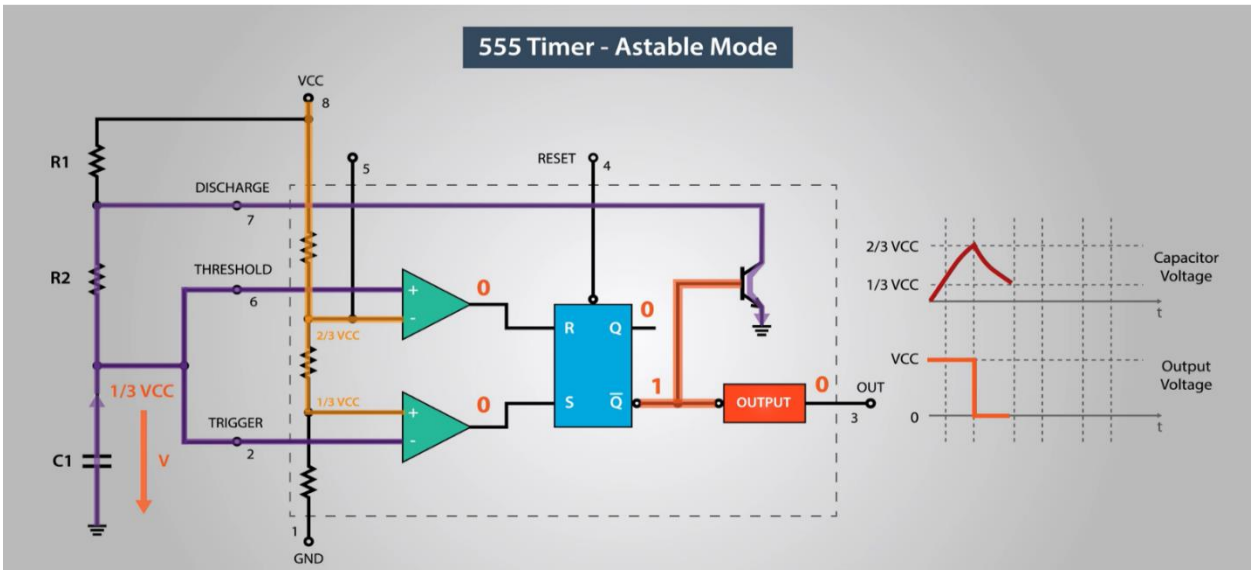
And the capacitor continues to charge until its value reaches 2/3 VCC, and in this case the output of the second comparator changes to become 1, and thus the value of R = 1 while the value of S is the same.

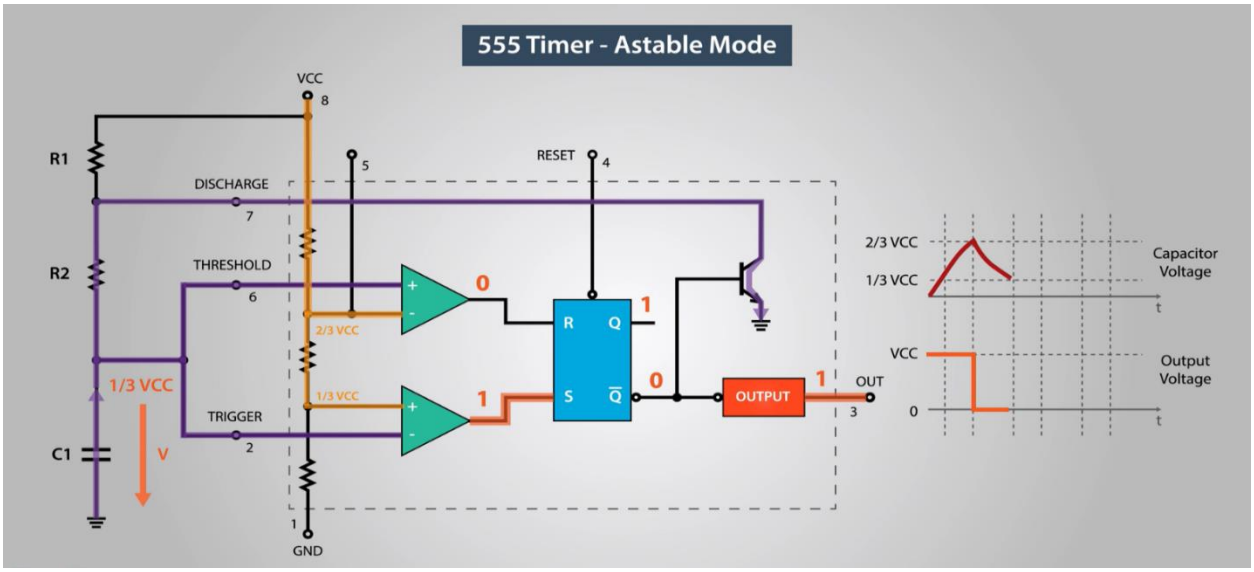
Certainly, the value of the flip-flop output changes to Q = 0 and Q' = 1, so that the final output = 0, and at the same time, the discharge transistor is activated and the capacitor starts discharging.

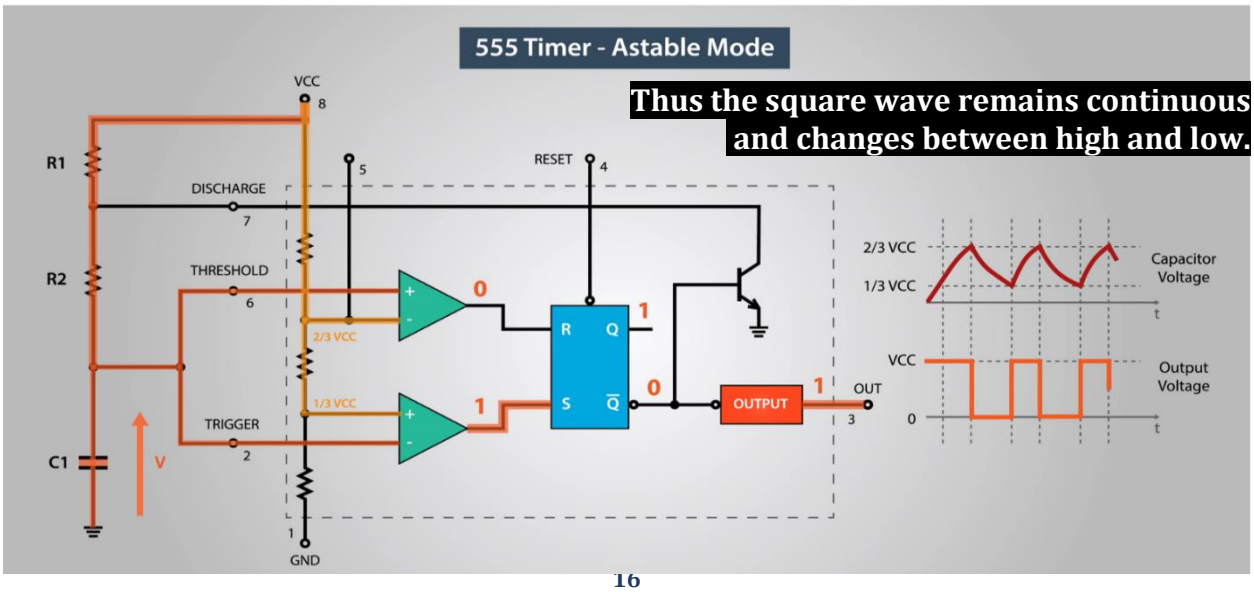


During discharging of the capacitor, and when its value drops to less than 2/3 VCC, the value of the second comparator (located above) returns to 0 again with the values of the flip-flop output constant until the output of the first comparator (below) changes when the capacitor value is less than 1/3 VCC, and at this moment the value of the S changes to be = 1 and accordingly the flip-flop output changes to equal to 1 and the discharge transistor is stopped.




555 Timer - Astable Mode
VCC
8
R1
DISCHARGE
7
5
RESET
4
R2
THRESHOLD
6
2/3 VCC
1/3 VCC
TRIGGER
2
C1
V
1
GND
R
Q
S
Q̄
OUTPUT
OUT
3
2/3 VCC
1/3 VCC
Capacitor Voltage
t
VCC
0
Output Voltage


555 Timer - Astable Mode
VCC
8
R1
DISCHARGE
7
5
RESET
4
R2
THRESHOLD
6
2/3 VCC
1/3 VCC
TRIGGER
2
C1
V
1
GND
R
Q
S
Q̄
OUTPUT
OUT
3
2/3 VCC
1/3 VCC
Capacitor Voltage
t
VCC
0
Output Voltage


555 Timer - Astable Mode
Thus the square wave remains continuous and changes between high and low.
VCC
8
R1
DISCHARGE
7
5
RESET
4
R2
THRESHOLD
6
2/3 VCC
1/3 VCC
TRIGGER
2
C1
V
1
GND
R
Q
S
Q̄
OUTPUT
OUT
3
2/3 VCC
1/3 VCC
Capacitor Voltage
t
VCC
0
Output Voltage