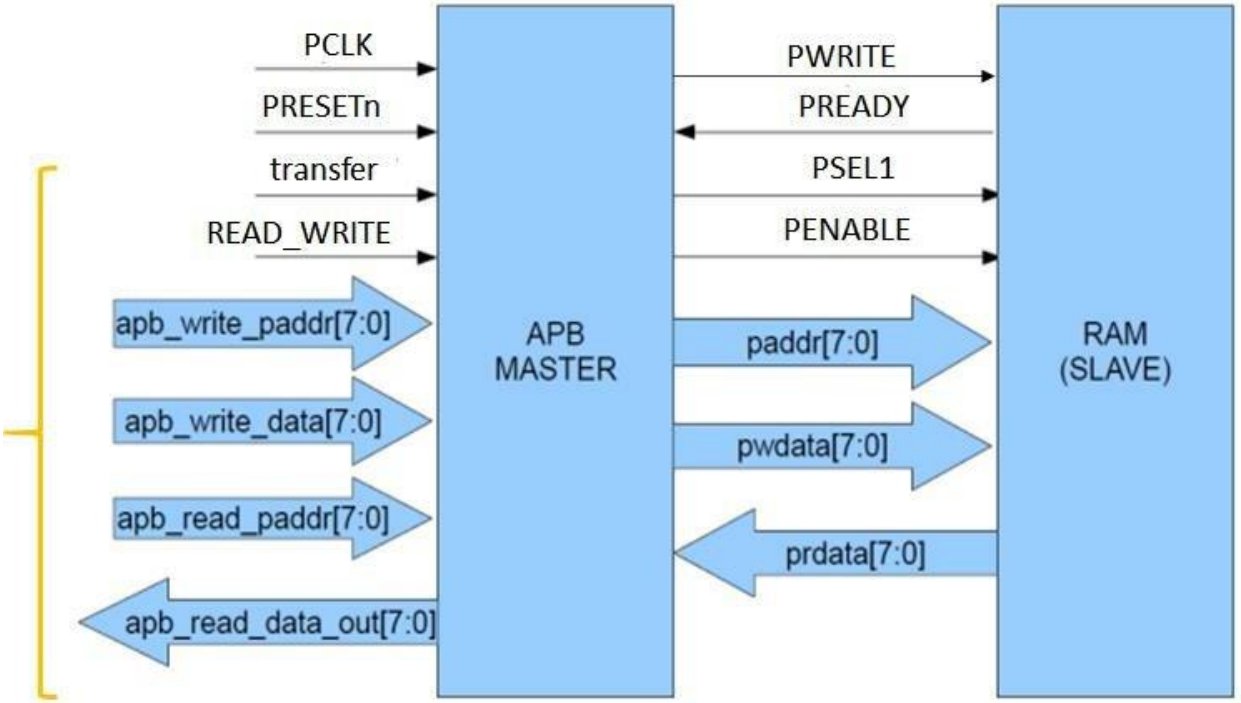
Project Specification Document

Project Title:

Implementation of APB Interface (Master/Slave) Using Combinational and Sequential Logic Circuits



Introduction:

The **Advanced Peripheral Bus (APB)** is a simplified interface used for connecting peripherals to a system in embedded systems, particularly in SoCs (System-on-Chip). It is designed for low-bandwidth, low-latency communication, making it ideal for simpler, slower peripherals such as timers, UARTs, and GPIOs. The APB protocol consists of basic handshaking signals and provides simple, single-cycle access to devices.

The APB bus uses the following primary signals:

- **PADDR**: Address bus.
- **PWDATA**: Write data bus.
- **PRDATA**: Read data bus.
- **PSEL**: Select signal, used to identify which peripheral is being accessed.
- **PWRITE**: Write control signal (indicates write operation).

- **PENABLE**: Enables the transfer cycle.
- **PREADY**: Slave ready signal, indicating the completion of the operation.

This project requires you to implement the APB interface (master and slave) using only combinational and sequential logic circuits, simulating it using an online circuit simulator and providing the schematic and simulation results as the deliverables.

Project Milestones:

Milestone 1: Design and Implement the Master Interface

Deliverables:

- **VHDL/Verilog Design**: Develop the HDL code of the APB master interface.
    - Implement logic for generating and driving the **PADDR**, **PWDATA**, **PWRITE**, and **PENABLE** signals based on a state machine that controls the read and write transactions.
    - Use sequential logic (flip-flops) for managing the transaction states.
- **Simulation Results**: Simulate the master interface using an online simulator. The simulation should show the behavior of the APB master generating address and data during both read and write operations.
    - Provide waveform outputs demonstrating the correct functionality of the master interface (address phase, data phase, and ready signal).

Milestone 2: Design and Implement the Slave Interface

Deliverables:

- **Schematic Design**: Design the APB slave interface.
    - Implement logic for receiving the address and data via **PADDR** and **PWDATA** from the master.
    - Use **PSEL**, **PWRITE**, and **PREADY** to handle read and write transactions.
    - Use flip-flops or registers to store the data temporarily and output the appropriate data during read operations (using **PRDATA**).
- **Simulation Results**: Simulate the slave interface. The simulation should show that the slave responds correctly to read and write operations, asserting **PREADY** at the appropriate times.
    - Provide waveform outputs showing the slave receiving the correct data and sending the correct responses during a transaction.

Milestone 3: Full System Integration and Final Simulation

Deliverables:

- **VHDL/Verilog Design**: Integrate the master and slave interfaces into a complete APB system, where the master communicates with the slave using the APB protocol.
    - Ensure correct transaction flow between the master and slave, including proper handshaking (i.e., **PREADY** and **PENABLE**).
- **Simulation Results**: Provide a full-system simulation showing the interaction between the APB master and slave. Demonstrate that the master initiates reads and writes correctly, and the slave responds appropriately.
    - Include waveforms that verify the complete APB communication process (address phase, data phase, and correct response from the slave).
- **Final Report**: Submit a report summarizing your design, the methodology used, and the results of your simulation. Include the VHDL/Verilog, schematics, simulation waveforms, and any issues or challenges encountered during the project.

Evaluation Criteria:

Your project will be evaluated based on the following criteria:

1. **Correctness**: The APB master and slave interfaces must function correctly according to the APB protocol. This includes correct timing of the control signals and data transfer.
2. **Design Quality**: The clarity and organization of your circuit design and schematics.
3. **Simulation Results**: The waveforms should demonstrate the expected behavior for both the master and slave during read and write transactions.
4. **Report**: The final report should be clear, well-organized, and include the schematic, simulation results, and a brief explanation of the design.

References:

- ARM, "AMBA Specification (APB)", ARM Ltd., 2010, AMBA 3 APB Specification.
- ARM, "AMBA 4 APB Specification", ARM Ltd., 2017, AMBA 4 APB Specification.
- ARM, "AMBA 3: APB and AHB Design", ARM Ltd., 2011.

Project Submission:

- **Deliverables**:
    1. VHDL/Verilog for the APB master and slave interfaces.

2. Simulation results (waveforms) showing the interaction between the master and slave.
3. A final report summarizing the design process and results.

Please submit your project as a ZIP file containing all schematic files, simulation files, and the report.

Good luck!