Mohamed A.Mohamed

900182267

Cache Assignment Report

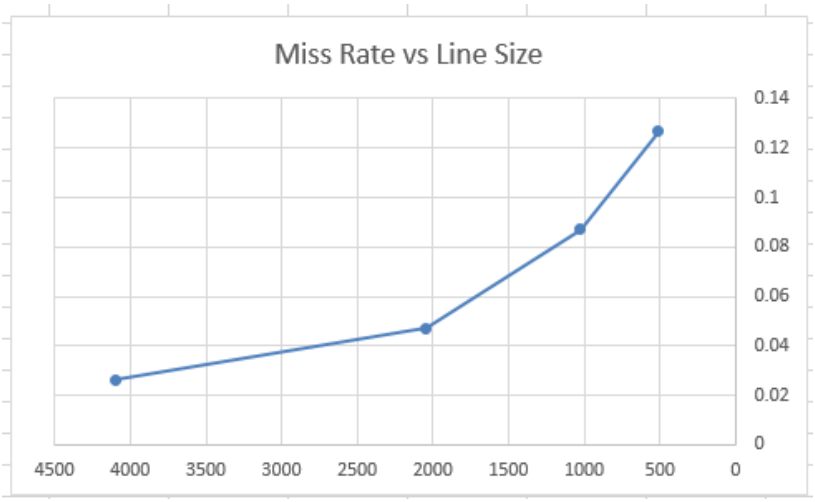
In this assignment, I could simulate what is happening in the cache in different scenarios. Unfortunately, as known, I have been facing the restriction of processing a huge number of instructions in one go due to the slow-down of my Laptop CPU. Anyways, we have made use of the PIN-Tool of INTEL to simulate the cache.

Throughout this experiment, I have tried to change four variables which are Cache Mode, Cache-Ways (number of Sets), Cache-Size, and Line (Block) Size, and remain the other constants.

- The first Part of my analysis is the comparison between the **Miss rate and Line Size.**

Horizontal Access:

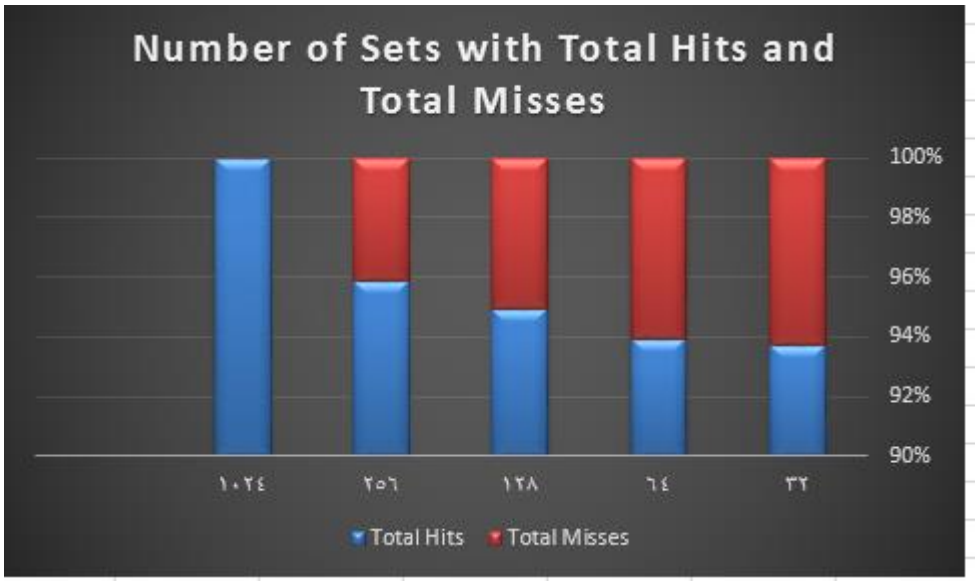
From the data that I have found, I have remained the Cache line and number of sets constants, whereas I have changed the values of line size.



Conclusion from the graph:

- Increasing the size of the block will give the chance to store more elements in this block after being fetched from the memory. This will drastically decrease the number of misses and increase the number of hits. For clarification, when I have an array that needs a tremendous addresses from the memory, I will store all of them in the cache instead of putting part of them in a cache and then back to the memory when needed to take the other part.

- **Second Analysis: "The number of Sets with Total Hits and Misses."**



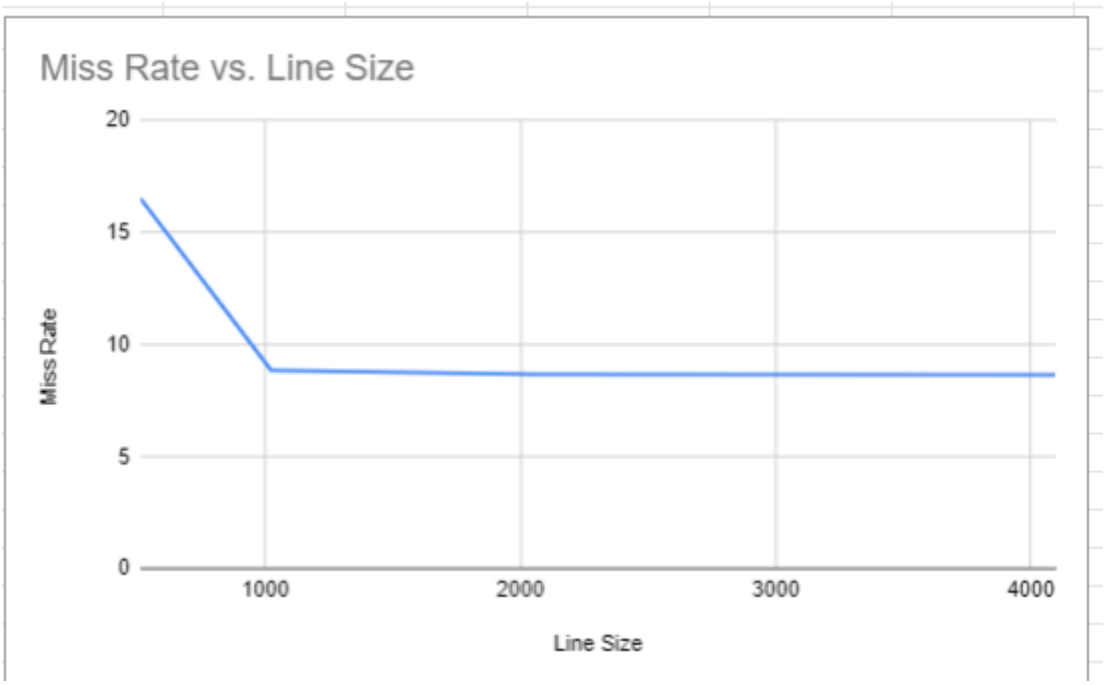
Observation: We can observe from the diagram above that by increasing the number of sets, the total misses can be completely eradicated.

The reason for why we got this observation:

Basically, when we have 32 set associative cache, I will have the space to put 32 arrays, for example, in it; however, with 64 set associative cache, I will have 64 direct maps to store data. This means that I will have the more space for storing data,

which this concludes that with increasing the sets, the total misses will decrease and so the total hits will increase.

Third Analysis: "Summation a 2-D array with each column comparison with the horizontal one.



Observation:

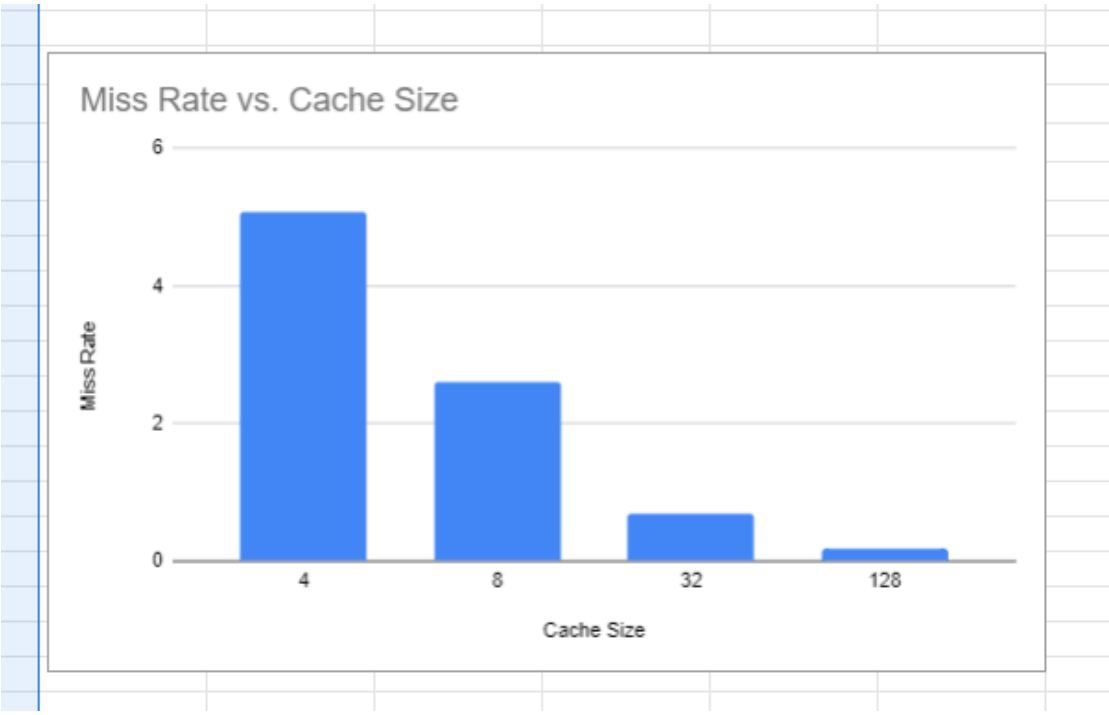
Summing the whole 2-D array vertically leads to a substantial increase in the levels of miss rate.

The reason behind this observation:

- Formally, each time I access a cell from a column, the whole row is loaded to the memory. As a result, the miss rate has increased drastically. The ratio of miss rate of the summing vertically the 2-D array compared to the horizontal (Chart 1) is 15/0.14 times.
- Sometimes, the miss rate can be constant although the line size is increasing.

Not only this, but it also leads to the concept of whether the cache is friendly or not. It is noticeable that from the summation of 2-D array cells by moving vertically does not do the friendly cache, whereas the other one does (the first diagram).

Fourth Analysis: "Cache Line vs Miss Rate".

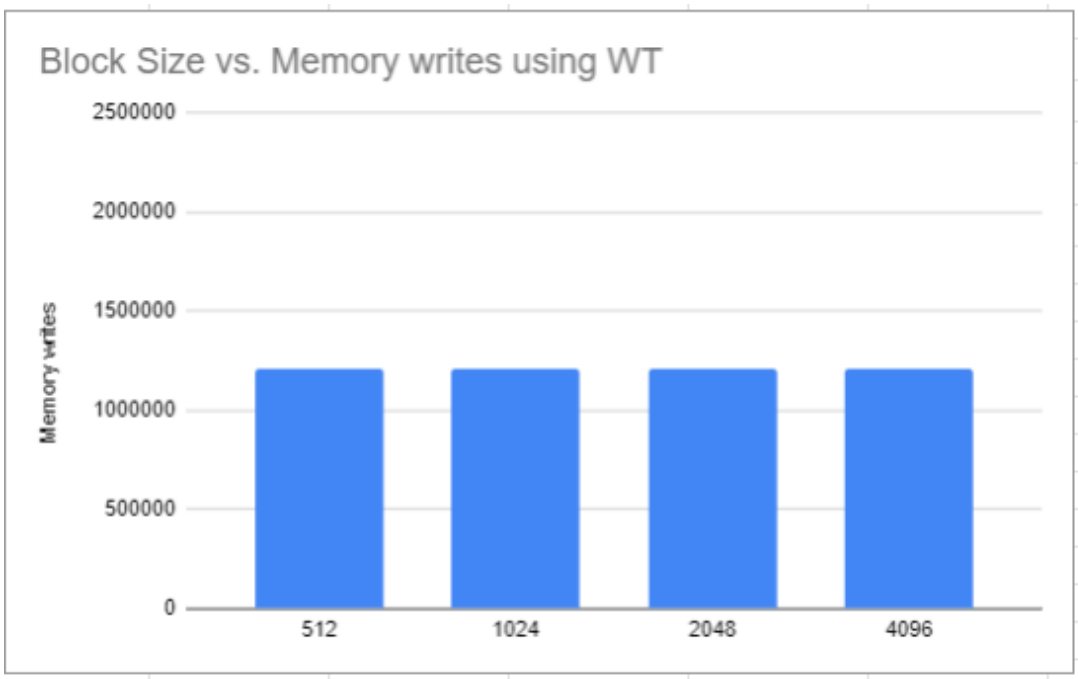


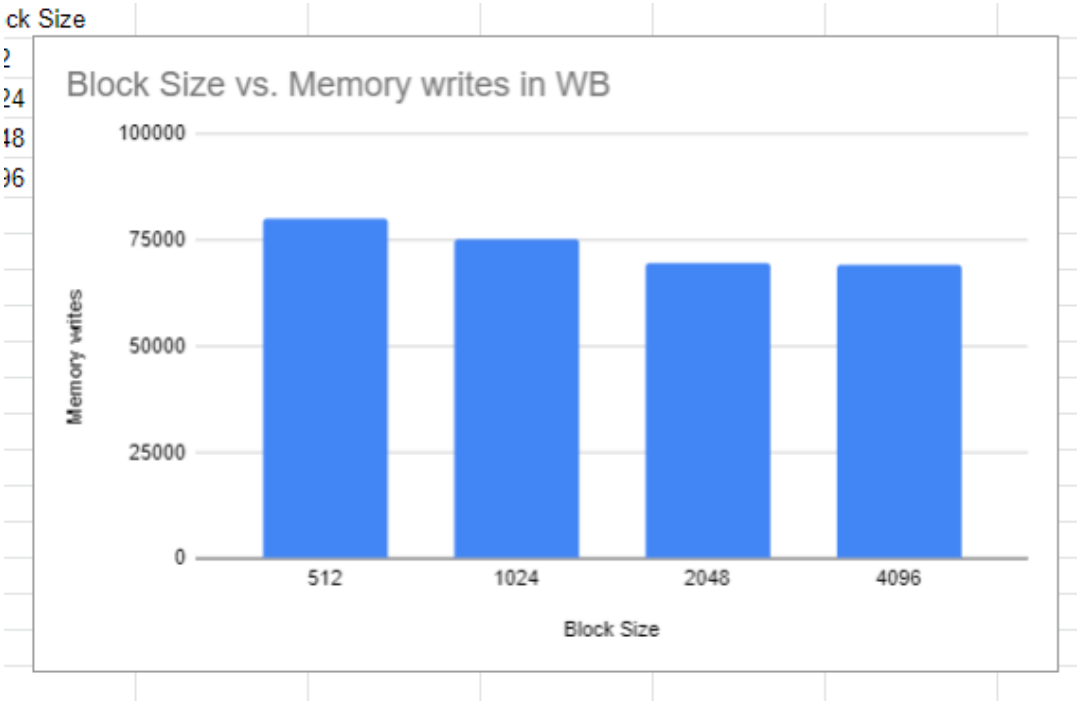
Observation: We can see from the chart below that by increasing the cache size, the miss rate is drastically decreasing.

The reason behind the observation:

Increasing the cache size will give more space for storing some data and addresses. That is why the more size in the cache, the less miss rate.

Fourth Analysis: "Write Back vs Write Through".





Observation: Write through has more writes in memory than Write Back. Write through is constant regardless the increase in the block size.

Explanation to the observation:

- The reason behind this is due to the fact that when I am using write through, every time I write in the cache and memory then. Imagine this I have a for loop; for sure, I will loop the by a number , do some operations, put in the cache then in then in the memory and so on. That is why the number of memory writes got incremented through Write through mode is very high. On the other side, the more efficient mode is write back. I increment and write in the cache as I want till finishing it. Then, I can put a block to the memory.
- Write through mode idea of "Go to the memory to write each time regardless the block size", whereas the WB mode can reduce the number of writing in memories by increasing the block size.

Conclusion:

We can conclude now that Write back mode is more efficient than write through. Imagine a huge number of data is happening each mili-seconds. That is why we have been thinking about the cache size and line size. We need it to have a lot of space for storing a huge amount of data to decrease the missing rate. How efficient Set associative cache compared to the others is a breakthrough. By increasing the number of sets, we can see from the previous graphs a decrease in missing rate. From here, we covered how the effect of spatial locality on the Cache performance.

Keep in mind that I have excel sheet and this link

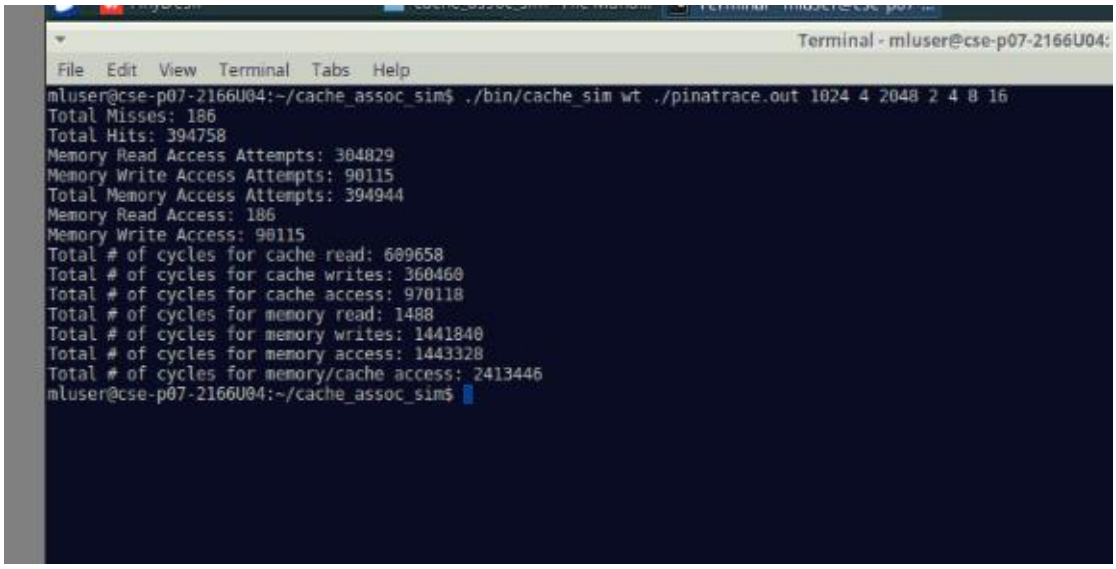
https://docs.google.com/spreadsheets/d/1_msK_UGE7MvDx5etD_1XvBNfObQf1jJN4VG0FjNnT6Y/edit#gid=1135354910

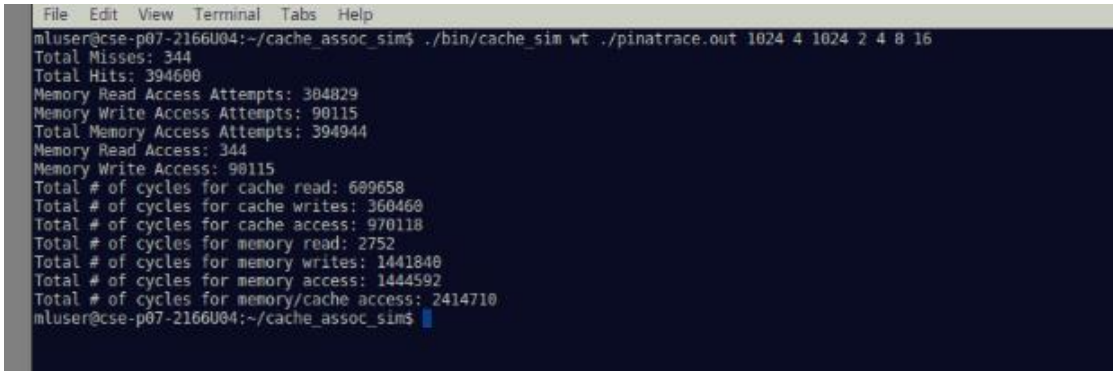
Which has some constructed diagrams.

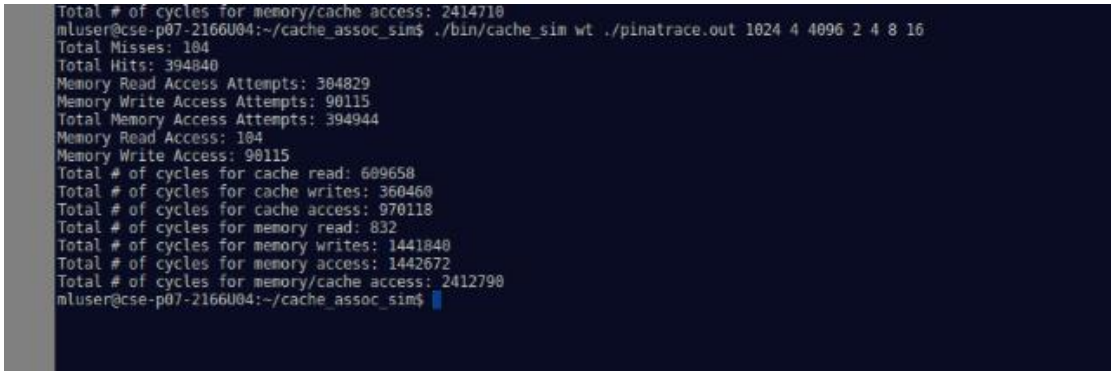
Screenshots from my program:

```
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 1024 4 1024 2 4 8 16
Total Misses: 344
Total Hits: 394600
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 344
Memory Write Access: 0
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 2752
Total # of cycles for memory writes: 0
Total # of cycles for memory access: 2752
Total # of cycles for memory/cache access: 972870
mluser@cse-p07-2166U04:~/cache_assoc_sim$
```

```
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 1024 4 2048 2 4 8 16
Total Misses: 186
Total Hits: 394758
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 186
Memory Write Access: 0
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 1488
Total # of cycles for memory writes: 0
Total # of cycles for memory access: 1488
Total # of cycles for memory/cache access: 971606
mluser@cse-p07-2166U04:~/cache_assoc_sim$
```


Terminal - mluser@cse-p07-2166U04:
File Edit View Terminal Tabs Help
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 1024 4 2048 2 4 8 16
Total Misses: 186
Total Hits: 394758
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 186
Memory Write Access: 90115
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 1488
Total # of cycles for memory writes: 1441840
Total # of cycles for memory access: 1443328
Total # of cycles for memory/cache access: 2413446
mluser@cse-p07-2166U04:~/cache_assoc_sim$


File Edit View Terminal Tabs Help
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 1024 4 1024 2 4 8 16
Total Misses: 344
Total Hits: 394600
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 344
Memory Write Access: 90115
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 2752
Total # of cycles for memory writes: 1441840
Total # of cycles for memory access: 1444592
Total # of cycles for memory/cache access: 2414710
mluser@cse-p07-2166U04:~/cache_assoc_sim$


Total # of cycles for memory/cache access: 2414710
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 1024 4 4096 2 4 8 16
Total Misses: 104
Total Hits: 394840
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 104
Memory Write Access: 90115
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 832
Total # of cycles for memory writes: 1441840
Total # of cycles for memory access: 1442672
Total # of cycles for memory/cache access: 2412790
mluser@cse-p07-2166U04:~/cache_assoc_sim$

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mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 1024 4 4096 2 4 8 16
Total Misses: 104
Total Hits: 394840
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 104
Memory Write Access: 0
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 832
Total # of cycles for memory writes: 0
Total # of cycles for memory access: 832
Total # of cycles for memory/cache access: 970950
mluser@cse-p07-2166U04:~/cache_assoc_sim$
```

```
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 1024 4 4096 2 4 8 16
Total Misses: 104
Total Hits: 394840
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 104
Memory Write Access: 0
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 832
Total # of cycles for memory writes: 0
Total # of cycles for memory access: 832
Total # of cycles for memory/cache access: 970950
mluser@cse-p07-2166U04:~/cache_assoc_sim$
```

```
Total # of cycles for memory/cache access: 32757246
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 4 128 2048 2 4 8 16
Total Misses: 1911
Total Hits: 5464418
Memory Read Access Attempts: 4255479
Memory Write Access Attempts: 1210850
Total Memory Access Attempts: 5466329
Memory Read Access: 1911
Memory Write Access: 1210850
Total # of cycles for cache read: 8510958
Total # of cycles for cache writes: 4843400
Total # of cycles for cache access: 13354358
Total # of cycles for memory read: 15288
Total # of cycles for memory writes: 19373600
Total # of cycles for memory access: 19388888
Total # of cycles for memory/cache access: 32743246
mluser@cse-p07-2166U04:~/cache_assoc_sim$
```

```
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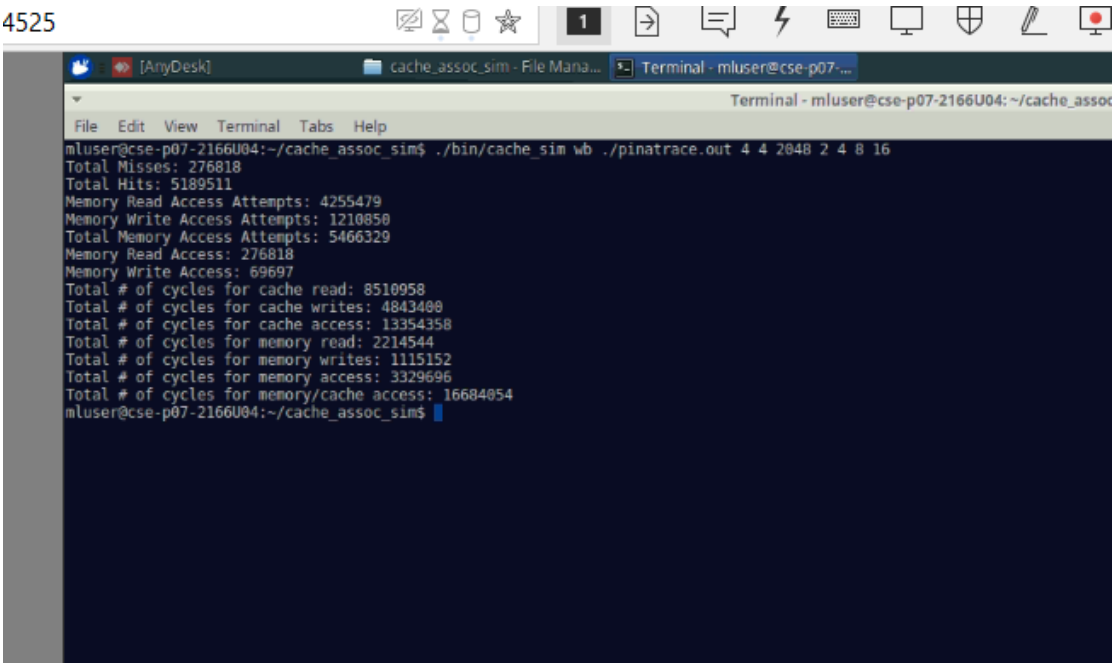
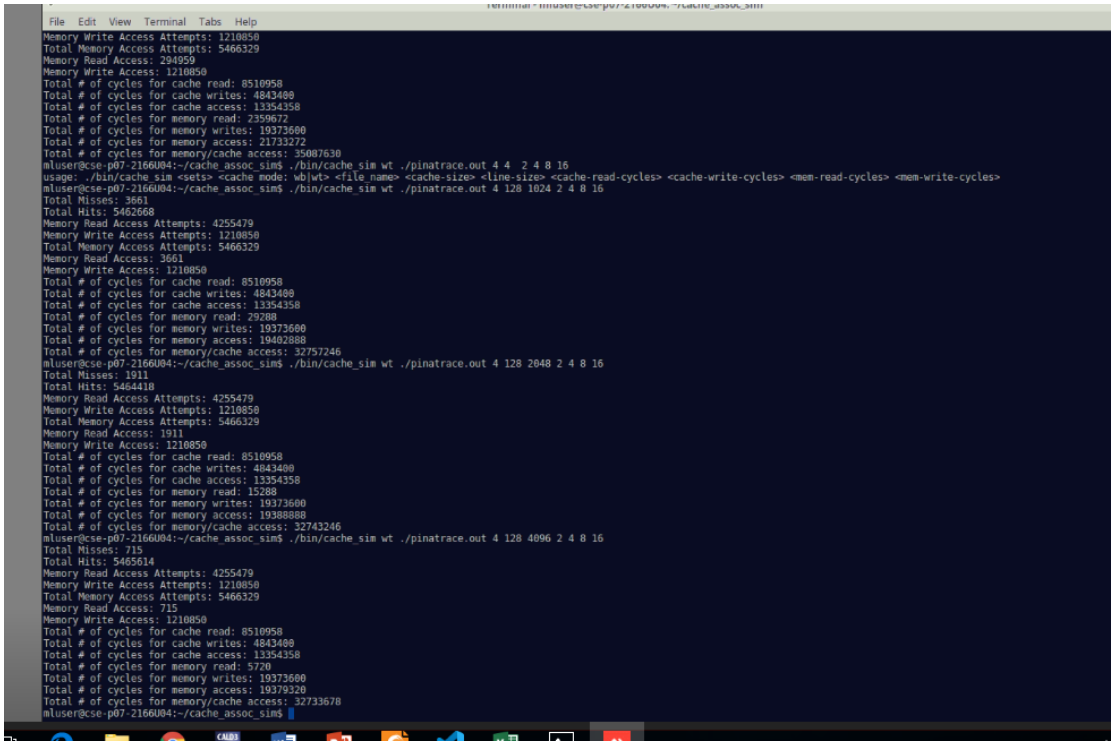
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 4 4 512 2 4 8 16
Total Misses: 295010
Total Hits: 5171319
Memory Read Access Attempts: 4255479
Memory Write Access Attempts: 1210850
Total Memory Access Attempts: 5466329
Memory Read Access: 295010
Memory Write Access: 80106
Total # of cycles for cache read: 8510958
Total # of cycles for cache writes: 4843400
Total # of cycles for cache access: 13354358
Total # of cycles for memory read: 2360080
Total # of cycles for memory writes: 1281696
Total # of cycles for memory access: 3641776
Total # of cycles for memory/cache access: 16996134
mluser@cse-p07-2166U04:~/cache_assoc_sim$
```

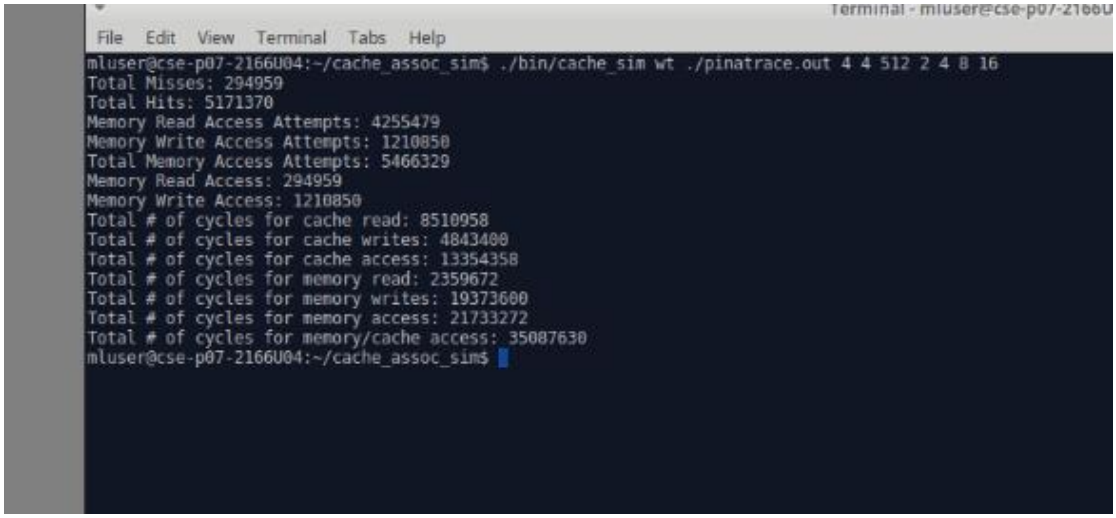
```
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 4 4 1024 2 4 8 16
Total Misses: 285843
Total Hits: 5180486
Memory Read Access Attempts: 4255479
Memory Write Access Attempts: 1210850
Total Memory Access Attempts: 5466329
Memory Read Access: 285843
Memory Write Access: 75472
Total # of cycles for cache read: 8510958
Total # of cycles for cache writes: 4843400
Total # of cycles for cache access: 13354358
Total # of cycles for memory read: 2286744
Total # of cycles for memory writes: 1207552
Total # of cycles for memory access: 3494296
Total # of cycles for memory/cache access: 16848654
mluser@cse-p07-2166U04:~/cache_assoc_sim$
```

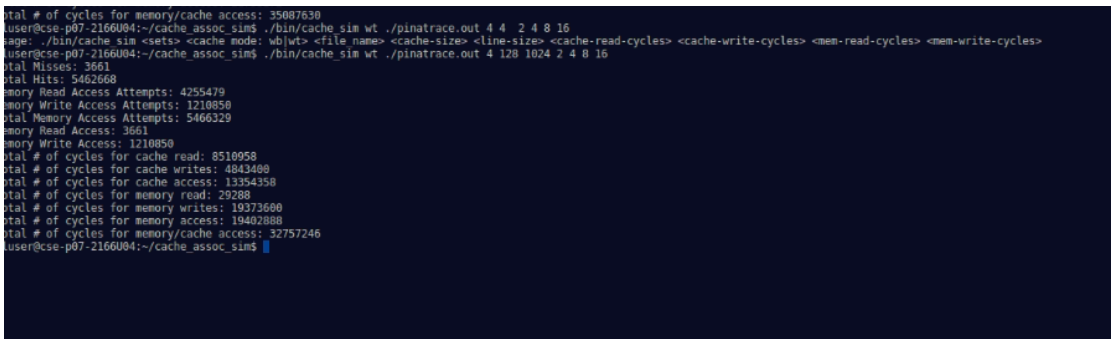
4525




```
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 4 4 4096 2 4 8 16
Total Misses: 277497
Total Hits: 5188832
Memory Read Access Attempts: 4255479
Memory Write Access Attempts: 1210850
Total Memory Access Attempts: 5466329
Memory Read Access: 277497
Memory Write Access: 69360
Total # of cycles for cache read: 8510958
Total # of cycles for cache writes: 4843400
Total # of cycles for cache access: 13354358
Total # of cycles for memory read: 2219976
Total # of cycles for memory writes: 1109760
Total # of cycles for memory access: 3329736
Total # of cycles for memory/cache access: 16684094
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 4 4 1024 2 4 8 16
```


File Edit View Terminal Tabs Help
Memory Write Access Attempts: 1210850
Total Memory Access Attempts: 5466329
Memory Read Access: 294959
Memory Write Access: 1210850
Total # of cycles for cache read: 8510958
Total # of cycles for cache writes: 4843400
Total # of cycles for cache access: 13354358
Total # of cycles for memory read: 2359672
Total # of cycles for memory writes: 19373600
Total # of cycles for memory access: 21733272
Total # of cycles for memory/cache access: 35087630
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 4 4 2 4 8 16
usage: ./bin/cache_sim <sets> <cache mode: wb|wt> <file_name> <cache-size> <line-size> <cache-read-cycles> <cache-write-cycles> <mem-read-cycles> <mem-write-cycles>
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 4 128 1024 2 4 8 16
Total Misses: 3661
Total Hits: 5462668
Memory Read Access Attempts: 4255479
Memory Write Access Attempts: 1210850
Total Memory Access Attempts: 5466329
Memory Read Access: 3661
Memory Write Access: 1210850
Total # of cycles for cache read: 8510958
Total # of cycles for cache writes: 4843400
Total # of cycles for cache access: 13354358
Total # of cycles for memory read: 29288
Total # of cycles for memory writes: 19373600
Total # of cycles for memory access: 19402888
Total # of cycles for memory/cache access: 32757246
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 4 128 2048 2 4 8 16
Total Misses: 1911
Total Hits: 5464418
Memory Read Access Attempts: 4255479
Memory Write Access Attempts: 1210850
Total Memory Access Attempts: 5466329
Memory Read Access: 1911
Memory Write Access: 1210850
Total # of cycles for cache read: 8510958
Total # of cycles for cache writes: 4843400
Total # of cycles for cache access: 13354358
Total # of cycles for memory read: 15288
Total # of cycles for memory writes: 19373600
Total # of cycles for memory access: 19388888
Total # of cycles for memory/cache access: 32743246
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 4 128 4096 2 4 8 16
Total Misses: 715
Total Hits: 5465614
Memory Read Access Attempts: 4255479
Memory Write Access Attempts: 1210850
Total Memory Access Attempts: 5466329
Memory Read Access: 715
Memory Write Access: 1210850
Total # of cycles for cache read: 8510958
Total # of cycles for cache writes: 4843400
Total # of cycles for cache access: 13354358
Total # of cycles for memory read: 5720
Total # of cycles for memory writes: 19373600
Total # of cycles for memory access: 19379320
Total # of cycles for memory/cache access: 32733678
mluser@cse-p07-2166U04:~/cache_assoc_sim$

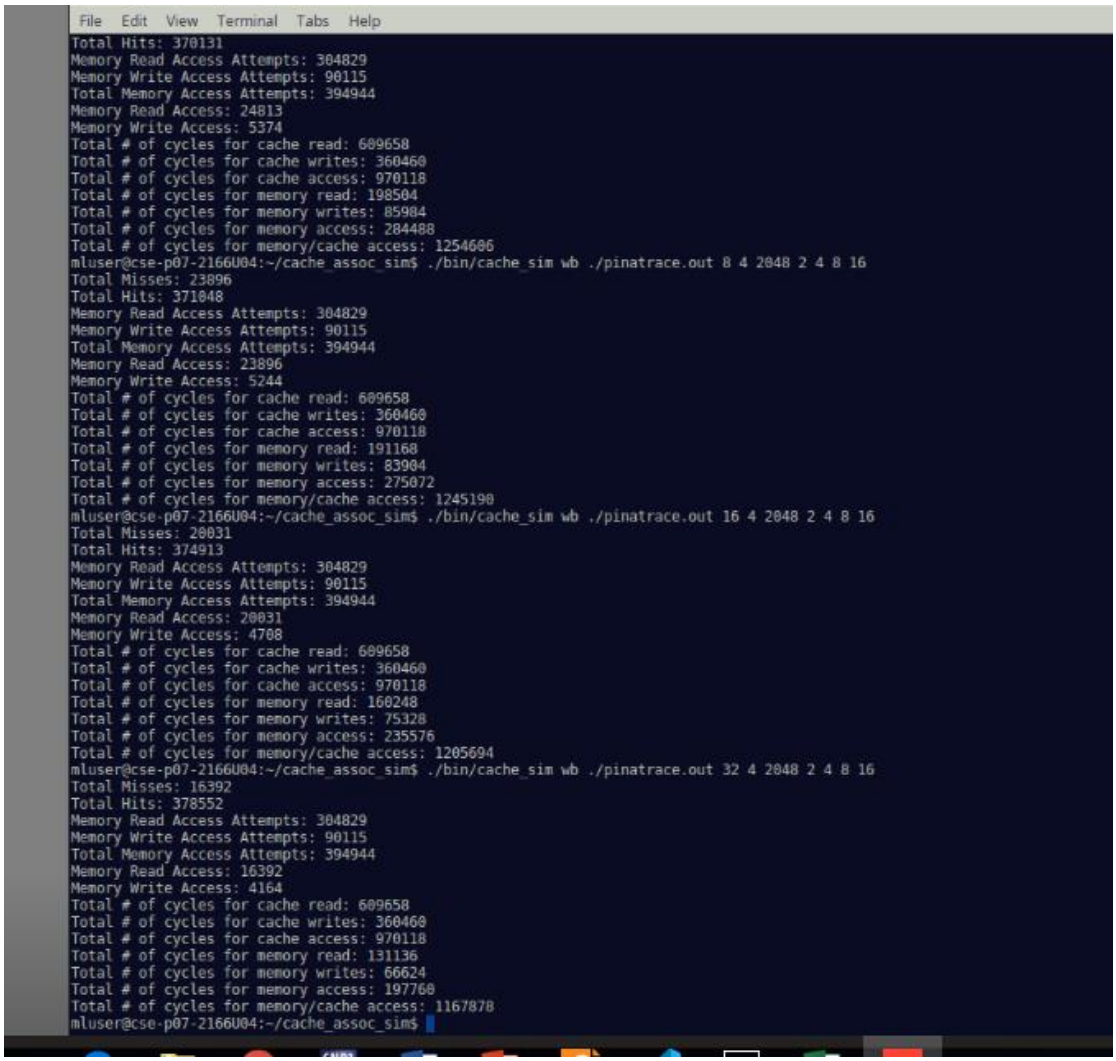

File Edit View Terminal Tabs Help
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 4 4 512 2 4 8 16
Total Misses: 294959
Total Hits: 5171370
Memory Read Access Attempts: 4255479
Memory Write Access Attempts: 1210850
Total Memory Access Attempts: 5466329
Memory Read Access: 294959
Memory Write Access: 1210850
Total # of cycles for cache read: 8510958
Total # of cycles for cache writes: 4843400
Total # of cycles for cache access: 13354358
Total # of cycles for memory read: 2359672
Total # of cycles for memory writes: 19373600
Total # of cycles for memory access: 21733272
Total # of cycles for memory/cache access: 35087630
mluser@cse-p07-2166U04:~/cache_assoc_sim$


otal # of cycles for memory/cache access: 35087630
luser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 4 4 2 4 8 16
sage: ./bin/cache_sim <sets> <cache mode: wb|wt> <file_name> <cache-size> <line-size> <cache-read-cycles> <cache-write-cycles> <mem-read-cycles> <mem-write-cycles>
luser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wt ./pinatrace.out 4 128 1024 2 4 8 16
otal Misses: 3661
otal Hits: 5462668
emory Read Access Attempts: 4255479
emory Write Access Attempts: 1210850
otal Memory Access Attempts: 5466329
emory Read Access: 3661
emory Write Access: 1210850
otal # of cycles for cache read: 8510958
otal # of cycles for cache writes: 4843400
otal # of cycles for cache access: 13354358
otal # of cycles for memory read: 29288
otal # of cycles for memory writes: 19373600
otal # of cycles for memory access: 19402888
otal # of cycles for memory/cache access: 32757246
luser@cse-p07-2166U04:~/cache_assoc_sim$

```
File  Edit  View  Terminal  Tabs  Help
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 4 4 1024 2 4 8 16
Total Misses: 1097374
Total Hits: 20519121
Memory Read Access Attempts: 16864165
Memory Write Access Attempts: 4752330
Total Memory Access Attempts: 21616495
Memory Read Access: 1097374
Memory Write Access: 288098
Total # of cycles for cache read: 33728330
Total # of cycles for cache writes: 19009320
Total # of cycles for cache access: 52737650
Total # of cycles for memory read: 8778992
Total # of cycles for memory writes: 4609568
Total # of cycles for memory access: 13388560
Total # of cycles for memory/cache access: 66126210
```

```
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 4 8 1024 2 4 8 16
Total Misses: 561650
Total Hits: 21054845
Memory Read Access Attempts: 16864165
Memory Write Access Attempts: 4752330
Total Memory Access Attempts: 21616495
Memory Read Access: 561650
Memory Write Access: 152880
Total # of cycles for cache read: 33728330
Total # of cycles for cache writes: 19009320
Total # of cycles for cache access: 52737650
Total # of cycles for memory read: 4493200
Total # of cycles for memory writes: 2446080
Total # of cycles for memory access: 6939280
Total # of cycles for memory/cache access: 59676930
mluser@cse-p07-2166U04:~/cache_assoc_sim$
```

```
Terminal - mluser@cse-p07-216
File  Edit  View  Terminal  Tabs  Help
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 4 32 1024 2 4 8 16
Total Misses: 147046
Total Hits: 21469449
Memory Read Access Attempts: 16864165
Memory Write Access Attempts: 4752330
Total Memory Access Attempts: 21616495
Memory Read Access: 147046
Memory Write Access: 42242
Total # of cycles for cache read: 33728330
Total # of cycles for cache writes: 19009320
Total # of cycles for cache access: 52737650
Total # of cycles for memory read: 1176368
Total # of cycles for memory writes: 675872
Total # of cycles for memory access: 1852240
Total # of cycles for memory/cache access: 54589890
```


File Edit View Terminal Tabs Help
Total Hits: 370131
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 24813
Memory Write Access: 5374
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 198504
Total # of cycles for memory writes: 85984
Total # of cycles for memory access: 284488
Total # of cycles for memory/cache access: 1254606
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 8 4 2048 2 4 8 16
Total Misses: 23896
Total Hits: 371048
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 23896
Memory Write Access: 5244
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 191168
Total # of cycles for memory writes: 83904
Total # of cycles for memory access: 275072
Total # of cycles for memory/cache access: 1245190
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 16 4 2048 2 4 8 16
Total Misses: 20031
Total Hits: 374913
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 20031
Memory Write Access: 4708
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 160248
Total # of cycles for memory writes: 75328
Total # of cycles for memory access: 235576
Total # of cycles for memory/cache access: 1205694
mluser@cse-p07-2166U04:~/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out 32 4 2048 2 4 8 16
Total Misses: 16392
Total Hits: 378552
Memory Read Access Attempts: 304829
Memory Write Access Attempts: 90115
Total Memory Access Attempts: 394944
Memory Read Access: 16392
Memory Write Access: 4164
Total # of cycles for cache read: 609658
Total # of cycles for cache writes: 360460
Total # of cycles for cache access: 970118
Total # of cycles for memory read: 131136
Total # of cycles for memory writes: 66624
Total # of cycles for memory access: 197760
Total # of cycles for memory/cache access: 1167878
mluser@cse-p07-2166U04:~/cache_assoc_sim$