Table 9. Pin muxing

Port	PCR	Alternate			1/0	Pad s	peed <sup>(5)</sup>	Р	in
pin	register	function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin
		Port /	4 (16-bit). Full	y available on 1	00-pin and 1	44-pin pac	kage.	1	
		ALT0	GPIO[0]	SIU Lite	I/O				
		ALT1	ETC[0]	eTimer0	I/O				
A[0]	PCR[0]	ALT2	SCK	DSPI2	I/O	Slow	Medium	51	73
		ALT3	F[0]	FCU0	0				
		_	EIRQ[0]	SIU Lite	I				
		ALT0	GPIO[1]	SIU Lite	I/O				
		ALT1	ETC[1]	eTimer0	I/O				
A[1]	PCR[1]	ALT2	SOUT	DSPI2	0	Slow	Medium	52	74
		ALT3	F[1]	FCU0	0				
		_	EIRQ[1]	SIU Lite	I				
		ALT0	GPIO[2]	SIU Lite	I/O				
		ALT1	ETC[2]	eTimer0	I/O				
		ALT2	_	_	_				
A[2] <sup>(6)</sup>	PCR[2]	ALT3	A[3]	FlexPWM0	0	Slow	Medium	57	84
		_	SIN	DSPI2	I				
		_	ABS[0]	mc_rgm	I				
		_	EIRQ[2]	SIU Lite	I				
		ALT0	GPIO[3]	SIU Lite	I/O				
		ALT1	ETC[3]	eTimer0	I/O				
A[3] <sup>(6)</sup>	PCR[3]	ALT2	CS0	DSPI2	I/O	Slow	Medium	64	92
∆[o]··	i Ori[J]	ALT3	B[3]	FlexPWM0	0	Slow	Mediaiii	04	32
		_	ABS[1]	mc_rgm	I				
		_	EIRQ[3]	SIU Lite	I				
		ALT0	GPIO[4]	SIU Lite	I/O				
		ALT1	ETC[0]	eTimer1	I/O				
A[4] <sup>(6)</sup>	PCR[4]	ALT2	CS1	DSPI2	0	Slow	Medium	75	108
, ,[ ,]	. 0[.]	ALT3	ETC[4]	eTimer0	I/O	O.O.	Modiani	, ,	.00
		_	FAB	mc_rgm	I				
		_	EIRQ[4]	SIU Lite	I				
		ALT0	GPIO[5]	SIU Lite	I/O				
		ALT1	CS0	DSPI1	I/O				
A[5]	PCR[5]	ALT2	ETC[5]	eTimer1	I/O	Slow	Medium	8	14
		ALT3	CS7	DSPI0	0				
		_	EIRQ[5]	SIU Lite	I				
		ALT0	GPIO[6]	SIU Lite	I/O				
		ALT1	SCK	DSPI1	I/O				
A[6]	PCR[6]	ALT2	_	_	_	Slow	Medium	2	2
		ALT3			_				
		_	EIRQ[6]	SIU Lite	l				

Table 9. Pin muxing (continued)

Port	PCR	Alternate function <sup>(1),</sup>	Functions	Peripheral <sup>(3)</sup>	I/O	Pad s	peed <sup>(5)</sup>	P	in	
pin	register	(2)	Functions	Peripheral	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin	
		ALT0	GPIO[7]	SIU Lite	I/O					
		ALT1	SOUT	DSPI1	0					
A[7]	PCR[7]	ALT2	_	_	_	Slow	Medium	4	10	
		ALT3	_	_	_					
		_	EIRQ[7]	SIU Lite	I					
		ALT0	GPIO[8]	SIU Lite	I/O					
		ALT1	_	_	_					
A[8]	PCR[8]	ALT2	_	_	_	Slow	Medium	6	12	
71[0]	1 011[0]	ALT3	_	_	_	Olow	Wicalain		12	
		_	SIN	DSPI1	I					
		_	EIRQ[8]	SIU Lite	I					
		ALT0	GPIO[9]	SIU Lite	I/O					
		ALT1	CS1	DSPI2	0					
A[9]	PCR[9]	ALT2	_	_	_	Slow	Medium	94	134	
		ALT3	B[3]	FlexPWM0	0					
		_	FAULT[0]	FlexPWM0	I					
		ALT0	GPIO[10]	SIU Lite	I/O					
		ALT1	CS0	DSPI2	I/O					
A[10]	PCR[10]	ALT2	B[0]	FlexPWM0	0	Slow	Medium	81	118	
		ALT3	X[2]	FlexPWM0	I/O					
		_	EIRQ[9]	SIU Lite	I					
		ALT0	GPIO[11]	SIU Lite	I/O					
		ALT1	SCK	DSPI2	I/O					
A[11]	PCR[11]	ALT2	A[0]	FlexPWM0	0	Slow	Medium	82	120	
		ALT3	A[2]	FlexPWM0	0					
		_	EIRQ[10]	SIU Lite	I					
		ALT0	GPIO[12]	SIU Lite	I/O					
		ALT1	SOUT	DSPI2	0					
A[12]	PCR[12]	ALT2	A[2]	FlexPWM0	0	Slow	Medium	83	122	
		ALT3	B[2]	FlexPWM0	0					
		_	EIRQ[11]	SIU Lite	Į					
		ALT0	GPIO[13]	SIU Lite	I/O					
		ALT1		_	_					
		ALT2	B[2]	FlexPWM0	0					
A[13]	PCR[13]	ALT3	_	_	_	Slow	Medium	95	136	
		_	SIN	DSPI2	I	Slow	Slow   Medium			130
		_	FAULT[0]	FlexPWM0	I					
		_	EIRQ[12]	SIU Lite	I					

Table 9. Pin muxing (continued)

Port	PCR	Alternate		9. Pin muxin	1/0		peed <sup>(5)</sup>	Р	in
pin	register	function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin
		ALT0	GPIO[14]	SIU Lite	I/O				
		ALT1	TXD	Safety Port0	0				
A[14]	PCR[14]	ALT2	ETC[4]	eTimer1	I/O	Slow	Medium	99	143
		ALT3	_	_	_				
		_	EIRQ[13]	SIU Lite	I				
		ALT0	GPIO[15]	SIU Lite	I/O				
		ALT1	_	_	_				
A[4.5]	DOD[45]	ALT2	ETC[5]	eTimer1	I/O	Class	Madium	100	144
A[15]	PCR[15]	ALT3		_	_	Slow	Medium	100	144
		_	RXD	Safety Port0	I				
		_	EIRQ[14]	SIU Lite	I				
		Port E	3 (16-bit). Full	y available on 1	00-pin and 1	44-pin pacl	kage.		
		ALT0	GPIO[16]	SIU Lite	I/O				
		ALT1	TXD	CAN0	0				
B[0]	PCR[16]	ALT2	ETC[2]	eTimer1	I/O	Slow	Medium	76	109
		ALT3	DEBUG[0]	SSCM	_				
		_	EIRQ[15]	SIU Lite	I				
		ALT0	GPIO[17]	SIU Lite	I/O				
		ALT1	_	_	_				
D[4]	DCD[47]	ALT2	ETC[3]	eTimer1	I/O	Claur	Madium	77	110
B[1]	PCR[17]	ALT3	DEBUG[1]	SSCM	_	Slow	Medium	77	110
		_	RXD	CAN0	I				
		_	EIRQ[16]	SIU Lite	I				
		ALT0	GPIO[18]	SIU Lite	I/O				
		ALT1	TXD	LIN0	0				
B[2]	PCR[18]	ALT2	_	_	_	Slow	Medium	79	114
		ALT3	DEBUG[2]	SSCM	_				
		_	EIRQ[17]	SIU Lite	I				
		ALT0	GPIO[19]	SIU Lite	I/O				
		ALT1	_	_	_				
B[3]	PCR[19]	ALT2	_	_	_	Slow	Medium	80	116
		ALT3	DEBUG[3]	SSCM	_				
		_	RXD	LIN0	I				
		ALT0	GPIO[22]	SIU Lite	I/O				
		ALT1	CLKOUT	Control	0				
B[6]	PCR[22]	ALT2	CS2	DSPI2	0	Slow	Medium	96	138
		ALT3	_	_	_				
		_	EIRQ[18]	SIU Lite	I				

Table 9. Pin muxing (continued)

Port	PCR	Alternate function <sup>(1),</sup>	Functions	Davishaval(3)	I/O		peed <sup>(5)</sup>	Р	in
pin	register	(2)	Functions	Peripheral <sup>(3)</sup>	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin
		ALT0	GPIO[23]	SIU Lite					
		ALT1	_	_					
B[7]	PCR[23]	ALT2	_	_	Input Only	_	_	29	43
	1 011[20]	ALT3	_	_	input Only				10
		_	AN[0]	ADC0					
		_	RXD	LIN0					
		ALT0	GPIO[24]	SIU Lite					
		ALT1	_	_					
B[8]	PCR[24]	ALT2	_	_	Input Only	_	_	31	47
احار	1 011[21]	ALT3	_	_	input Only				.,
		_	AN[1]	ADC0					
		_	ETC[5]	eTimer0					
		ALT0	GPIO[25]	SIU Lite					
		ALT1	_	_					
B[9]	PCR[25]	ALT2	_	_	Input Only	_	_	35	52
		ALT3	_	_					
		_	AN[11]	ADC0 – ADC1					
		ALT0	GPIO[26]	SIU Lite					
		ALT1	_	_					
B[10]	PCR[26]	ALT2	_	_	Input Only	_	_	36	53
		ALT3	_	_					
		_	AN[12]	ADC0 – ADC1					
		ALT0	GPIO[27]	SIU Lite					
		ALT1	_	_					
B[11]	PCR[27]	ALT2	_	_	Input Only	_	_	37	54
		ALT3	_	_					
		_	AN[13]	ADC0 – ADC1					
		ALT0	GPIO[28]	SIU Lite					
		ALT1	_	_					
B[12]	PCR[28]	ALT2	_	_	Input Only	_	_	38	55
		ALT3	_	_					
		_	AN[14]	ADC0 – ADC1					
		ALT0	GPIO[29]	SIU Lite					
		ALT1	_	_					
D[40]	DCD[00]	ALT2	_	_	Input Only			42	60
B[13]	PCR[29]	ALT3	_	_	Input Only	ıly —	-   -	42	60
		_	AN[0]	ADC1					
		_	RXD	LIN1					

Table 9. Pin muxing (continued)

Port	PCR	Alternate		5. FIII IIIUXIII	1/0		speed <sup>(5)</sup>	Р	in
pin	register	function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin
		ALT0	GPIO[30]	SIU Lite					
		ALT1	_	_					
		ALT2	_	_					
B[14]	PCR[30]	ALT3	_	_	Input Only	_	_	44	64
		_	AN[1]	ADC1					
		_	ETC[4]	eTimer0					
		_	EIRQ[19]	SIU Lite					
		ALT0	GPIO[31]	SIU Lite					
		ALT1	_	_					
D[4.5]	DCD[04]	ALT2	_	_	Innut Only			40	60
B[15]	PCR[31]	ALT3	_	_	Input Only	_	_	43	62
		_	AN[2]	ADC1					
		_	EIRQ[20]	SIU Lite					
		Port (	C (16-bit). Full	y available on 1	00-pin and 1	44-pin pac	kage.		
		ALT0	GPIO[32]	SIU Lite					
		ALT1	_	_					
C[0]	PCR[32]	ALT2	_	_	Input Only	_	_	45	66
		ALT3	_	_					
		_	AN[3]	ADC1					
		ALT0	GPIO[33]	SIU Lite					
		ALT1	_	_					
C[1]	PCR[33]	ALT2	_	_	Input Only	_	_	28	41
		ALT3	_	_					
		_	AN[2]	ADC0					
		ALT0	GPIO[34]	SIU Lite					
		ALT1	_	_					
C[2]	PCR[34]	ALT2		_	Input Only	_	_	30	45
		ALT3		_					
		_	AN[3]	ADC0					
		ALT0	GPIO[35]	SIU Lite	I/O				
		ALT1	CS1	DSPI0	0				
C[3]	PCR[35]	ALT2	ETC[4]	eTimer1	I/O	Slow	Medium	10	16
		ALT3	TXD	LIN1	0				
		_	EIRQ[21]	SIU Lite	l				
		ALT0	GPIO[36]	SIU Lite	I/O				
		ALT1	CS0	DSPI0	I/O				
C[4]	PCR[36]	ALT2	X[1]	FlexPWM0	I/O	Slow	Medium	5	11
		ALT3	DEBUG[4]	SSCM	_				
		_	EIRQ[22]	SIU Lite	I				

Table 9. Pin muxing (continued)

Port	PCR	Alternate		9. Pin muxin	1/0	-	peed <sup>(5)</sup>	Р	in
pin	register	function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin
		ALTO	GPIO[37] SCK	SIU Lite DSPI0	I/O I/O				
C[5]	PCR[37]	ALT2 ALT3 — —	DEBUG[5] FAULT[3] EIRQ[23]	SSCM FlexPWM0 SIU Lite	_ _   	Slow	Medium	7	13
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 —	GPIO[38] SOUT B[1] DEBUG[6] EIRQ[24]	SIU Lite DSPI0 FlexPWM0 SSCM SIU Lite	I/O O O —	Slow	Medium	98	142
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3 —	GPIO[39] — A[1] DEBUG[7] SIN	SIU Lite  — FlexPWM0 SSCM DSPI0	O   -	Slow	Medium	9	15
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3 —	GPIO[40] CS1 — CS6 FAULT[2]	SIU Lite DSPI1 — DSPI0 FlexPWM0	I/O O — O I	Slow	Medium	91	130
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3 —	GPIO[41]	SIU Lite DSPI2 — FlexPWM0 FlexPWM0	I/O O — I/O I	Slow	Medium	84	123
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3 —	GPIO[42] CS2 — A[3] FAULT[1]	SIU Lite DSPI2 — FlexPWM0 FlexPWM0	I/O O — O	Slow	Medium	78	111
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[4] CS2 CS0	SIU Lite eTimer0 DSPI2 DSPI3	I/O I/O O I/O	Slow	Medium	55	80
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3	GPIO[44] ETC[5] CS3 CS1	SIU Lite eTimer0 DSPI2 DSPI3	I/O I/O O	Slow	Medium	56	82

Table 9. Pin muxing (continued)

Port	PCR	Alternate		9. Pin muxin	1/0	•	speed <sup>(5)</sup>	Р	in
pin	register	function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin
		ALT0	GPIO[45]	SIU Lite	I/O				
		ALT1	ETC[1]	eTimer1	I/O				
C[13]	PCR[45]	ALT2	_	_	_	Slow	Medium	71	101
		ALT3		_	_				
		_	EXT IN EXT. SYNC	ctu0 FlexPWM0	I				
		ALT0	GPIO[46]	SIU Lite	1/0				
C[14]	DCD[46]	ALT1	ETC[2]	eTimer1	I/O	Slow	Medium	72	103
C[14]	PCR[46]	ALT2	EXT TGR	ctu0	0	Slow	Medium	12	103
		ALT3	_	_	_				
		ALT0	GPIO[47]	SIU Lite	I/O				
		ALT1	CA TR EN	FlexRay0	0				
0[45]	DOD[47]	ALT2	ETC[0]	eTimer1	I/O	01	0	0.5	404
C[15]	PCR[47]	ALT3	A[1]	FlexPWM0	0	Slow	Symmetric	85	124
		_	EXT IN	ctu0	I				
		_	EXT. SYNC	FlexPWM0	I				
		Port I	D (16-bit). Full	y available on 1	00-pin and 1	44-pin pac	kage.	l	
		ALT0	GPIO[48]	SIU Lite	I/O				
D[0]	PCR[48]	ALT1	CA TX	FlexRay0	0	Slow	Cummotrio	96	125
D[O]	FON[40]	ALT2	ETC[1]	eTimer1	I/O	SIOW	Symmetric	86	125
		ALT3	B[1]	FlexPWM0	0				
		ALT0	GPIO[49]	SIU Lite	I/O				
		ALT1	_	_	_				
D[1]	PCR[49]	ALT2	ETC[2]	eTimer1	I/O	Slow	Medium	3	3
		ALT3	EXT TRG	ctu0	0				
		_	CA RX	FlexRay0	1				
		ALT0	GPIO[50]	SIU Lite	I/O				
		ALT1		_	_				
D[2]	PCR[50]	ALT2	ETC[3]	eTimer1	I/O	Slow	Medium	97	140
		ALT3	X[3]	FlexPWM0	I/O				
		_	CB RX	FlexRay0	I				
		ALT0	GPIO[51]	SIU Lite	I/O				
ופות	DCD[E41	ALT1	CB TX	FlexRay0	0	Slow	Symmetric	90	100
D[3]	PCR[51]	ALT2	ETC[4]	eTimer1	I/O	Slow	Symmetric	ric 89	128
		ALT3	A[3]	FlexPWM0	0				
		ALT0	GPIO[52]	SIU Lite	I/O				
DIAI	DODICO	ALT1	CB TR EN	FlexRay0	0	Cle	ou Summetrie 00	120	
D[4]	PCR[52]	ALT2	ETC[5]	eTimer1	I/O	Slow	Symmetric	90	129
		ALT3	B[3]	FlexPWM0	0				

Table 9. Pin muxing (continued)

Port	PCR	Alternate		9. FIII III (3)	I/O		peed <sup>(5)</sup>	Р	in
pin	register	function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] SOUT	SIU Lite DSPI0 FCU0 DSPI3	I/O O O	Slow	Medium	22	33
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3	GPIO[54] CS2 SCK — FAULT[1]	SIU Lite DSPI0 DSPI3 — FlexPWM0	I/O O I/O —	Slow	Medium	23	34
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3 F[1] CS4 SIN	SIU Lite DSPI1 FCU0 DSPI0 DSPI3	I/O O O O	Slow	Medium	26	37
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3	GPIO[56] CS2 — CS5 FAULT[3]	SIU Lite DSPI1 — DSPI0 FlexPWM0	-0 05	Slow	Medium	21	32
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIU Lite FlexPWM0 LIN1 —	I/O I/O O	Slow	Medium	15	26
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] CS0	SIU Lite FlexPWM0 DSPI3 —	I/O O I/O —	Slow	Medium	53	76
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] CS1 SCK	SIU Lite FlexPWM0 DSPI3 DSPI3	9009	Slow	Medium	54	78
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3	GPIO[60] X[1] — — RXD	SIU Lite FlexPWM0 — — LIN1	-	Slow	Medium	70	99
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] CS2 SOUT	SIU Lite FlexPWM0 DSPI3 DSPI3	I/O O O	Slow	Medium	67	95

Table 9. Pin muxing (continued)

		Alternate	Table	9. Pin muxin			peed <sup>(5)</sup>	Р	in
Port pin	PCR register	function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	I/O direction <sup>(4)</sup>	SRC = 0	SRC = 1		144-pin
D[14]	PCR[62]	ALTO ALT1 ALT2 ALT3	GPIO[62] B[1] CS3 — SIN	SIU Lite FlexPWM0 DSPI3 — DSPI3	I/O O O —	Slow	Medium	73	105
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — — AN[4]	SIU Lite  ADC1	Input Only	1	_	41	58
	Port E(16-	bit). Fully ava	ilable on 144-	pin package. E[	0], E[1] and E	E[2] availat	ole on 100-p	in package	Э.
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — — AN[5]	SIU Lite  —  —  —  ADC1	Input Only	-	_	46	68
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — — AN[4]	SIU Lite  —  —  —  ADC0	Input Only	I	_	27	39
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — — AN[5]	SIU Lite  —  —  ADC0	Input Only	-	_	32	49
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — — AN[6]	SIU Lite  ADC0	Input Only	_	_	_	40
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — — AN[7]	SIU Lite  —  —  ADC0	Input Only	_	_	_	42
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — — AN[8]	SIU Lite  —  —  —  ADC0	Input Only	_	_	_	44

Table 9. Pin muxing (continued)

Port	PCR	Alternate		9. Pin muxin	1/0		peed <sup>(5)</sup>	Р	in
pin	register	function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — — AN[9]	SIU Lite  —  —  —  ADC0	Input Only	-	_	_	46
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] AN[10]	SIU Lite  ADC0	Input Only	_	_	_	48
E[8]	PCR[72]	ALT0 ALT1 ALT2 ALT3 —	GPIO[72] — — — — AN[6]	SIU Lite  —  —  —  ADC1	Input Only	_	_	_	59
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3	GPIO[73] — — — — AN[7]	SIU Lite  ADC1	Input Only	_	_	_	61
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3 —	GPIO[74] AN[8]	SIU Lite  ADC1	Input Only		_	_	63
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3 —	GPIO[75] — — — — AN[9]	SIU Lite  ADC1	Input Only	-	_	_	65
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3 —	GPIO[76] — — — — AN[10]	SIU Lite  ADC1	Input Only		_	_	67
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3 —	GPIO[77] SCK — — EIRQ[25]	SIU Lite DSPI3 — — SIU Lite	I/O I/O — — I	Slow	Medium	_	117

Table 9. Pin muxing (continued)

	Port PCR		on <sup>(1),</sup> Functions P	no Dowinhows (3)	Pad speed <sup>(5)</sup>		Pin		
"   '	register	function <sup>(1)</sup> , (2)	Functions	Peripheral <sup>(3)</sup>	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin
		ALT0	GPIO[78]	SIU Lite	I/O				
F(4.4) F	DOD(701	ALT1	SOUT	DSPI3	0	01			440
E[14] F	PCR[78]	ALT2	_	_		Slow	Medium	_	119
		ALT3	— EIRQ[26]	— SIU Lite	_ 				
		ALTO							
		ALT0	GPIO[79]	SIU Lite	I/O				
		ALT1	_	_	_				
E[15] F	PCR[79]	ALT2	_	_	_	Slow	Medium	_	121
		ALT3	— —	— —	_				
		_	SIN	DSPI3	l I				
			EIRQ[27]	SIU Lite	I				
			Port F (16-bi	t). Fully availabl	e on 144-pin	package			
		ALT0	GPIO[80]	SIU Lite	I/O				
		ALT1	DBG0	FlexRay0	0				
F[0] F	PCR[80]	ALT2	CS3	DSPI3	0	Slow	Medium	_	133
		ALT3	_	_	_				
		_	EIRQ[28]	SIU Lite	I				
		ALT0	GPIO[81]	SIU Lite	I/O				
		ALT1	DBG1	FlexRay0	0				
F[1] F	PCR[81]	ALT2	CS2	DSPI3	0	Slow	Medium	_	135
		ALT3		_	_				
		_	EIRQ[29]	SIU Lite	1				
		ALT0	GPIO[82]	SIU Lite	I/O				
F[2] F	PCR[82]	ALT1	DBG2	FlexRay0	0	Slow	Medium		137
' [2]   '	1 011[02]	ALT2	CS1	DSPI3	0	Olow	Mediaiii		107
		ALT3	_	_	_				
		ALT0	GPIO[83]	SIU Lite	I/O				
F[3] F	PCR[83]	ALT1	DBG3	FlexRay0	0	Slow	Medium		139
1 [0] 1	i Ori[00]	ALT2	CS0	DSPI3	I/O	SIOW	Medium		109
		ALT3	_	_	_				
		ALT0	GPIO[84]	SIU Lite	I/O				
E[4]   F	PCR[84]	ALT1	MDO[3]	nexus0	0	Slow	East		4
F[4] F	PCR[04]	ALT2	_	_	_	Slow	Fast	_	4
		ALT3	_	_	_				
		ALT0	GPIO[85]	SIU Lite	I/O				
EIE1 F	PCR[85]	ALT1	MDO[2]	nexus0	0	Slow	East		E
F[5] F		ALT2	_	_	_	Slow	Fast		5
		ALT3	_	_	_				

Table 9. Pin muxing (continued)

Port	PCR	Alternate		5. 1 III III (3)	I/O		peed <sup>(5)</sup>	Р	in
pin	register	function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	direction <sup>(4)</sup>	SRC = 0	SRC = 1	100-pin	144-pin
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] MDO[1] — —	SIU Lite nexus0 — —	I/O O —	Slow	Fast	_	8
F[7]	PCR[87]	ALT0 ALT1 ALT2 ALT3	GPIO[87] MCKO —	SIU Lite nexus0 — —	I/O O —	Slow	Fast	_	19
F[8]	PCR[88]	ALT0 ALT1 ALT2 ALT3	GPIO[88] MSEO1 —	SIU Lite nexus0 —	I/O O —	Slow	Fast	_	20
F[9]	PCR[89]	ALT0 ALT1 ALT2 ALT3	GPIO[89] MSEO0 —	SIU Lite nexus0 — —	I/O O —	Slow	Fast	_	23
F[10]	PCR[90]	ALT0 ALT1 ALT2 ALT3	GPIO[90] EVTO — —	SIU Lite nexus0 — —	I/O O —	Slow	Fast	_	24
F[11]	PCR[91]	ALT0 ALT1 ALT2 ALT3 —	GPIO[91] — — — EVTI	SIU Lite  —  —  —  nexus0	I/O — — — —	Slow	Medium	_	25
F[12]	PCR[92]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[3] — —	SIU Lite eTimer1 — —	I/O I/O —	Slow	Medium	_	106
F[13]	PCR[93]	ALT0 ALT1 ALT2 ALT3 —	GPIO[93]	SIU Lite  —  —  —  eTimer1	I/O — — — —	Slow	Medium	_	112
F[14]	PCR[94]	ALT0 ALT1 ALT2 ALT3	GPIO[94] TXD — —	SIU Lite LIN1 — —	I/O O —	Slow	Medium	_	115

Table 9. Pin muxing (continued)

Port pin	PCR register	Alternate function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	I/O direction <sup>(4)</sup>	Pad speed <sup>(5)</sup>		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
F[15]	PCR[95]	ALT0 ALT1 ALT2 ALT3 —	GPIO[95] — — — — RXD	SIU Lite  LIN1	I/O — — —	Slow	Medium	_	113
Port G (12-bit). Fully available on 144-pin package.									
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3 —	GPIO[96] F[0] — — EIRQ[30]	SIU Lite FCU0 — — SIU Lite	I/O O — —	Slow	Medium	_	38
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3 —	GPIO[97] F[1] — — EIRQ[31]	SIU Lite FCU0 — — SIU Lite	I/O O — — I	Slow	Medium	_	141
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3	GPIO[98] X[2] — —	SIU Lite FlexPWM0 — —	I/O I/O —	Slow	Medium	_	102
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] A[2] — —	SIU Lite FlexPWM0 — —	0 5	Slow	Medium	_	104
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	GPIO[100] B[2] — —	SIU Lite FlexPWM0 — —	I/O O —	Slow	Medium	_	100
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	GPIO[101] X[3] — —	SIU Lite FlexPWM0 — —	I/O I/O —	Slow	Medium	_	85
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	GPIO[102] A[3] — —	SIU Lite FlexPWM0 — —	I/O O —	Slow	Medium	_	98
G[7]	PCR[103]	ALT0 ALT1 ALT2 ALT3	GPIO[103] B[3] — —	SIU Lite FlexPWM0 — —	I/O O —	Slow	Medium	_	83

Table 9. Pin muxing (continued)

Port pin	PCR register	Alternate function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	I/O direction <sup>(4)</sup>	Pad speed <sup>(5)</sup>		Pin	
						SRC = 0	SRC = 1	100-pin	144-pin
G[8]	PCR[104]	ALT0	GPIO[104]	SIU Lite	I/O	Slow	Medium		81
		ALT1	_	_	_				
		ALT2		_	_				
		ALT3	_	_	_				
		_	FAULT[0]	FlexPWM0	I				
	PCR[105]	ALT0	GPIO[105]	SIU Lite	I/O	Slow	Medium		79
		ALT1	_	_	_				
G[9]		ALT2	_	_	_				
		ALT3	_	_	_				
		_	FAULT[1]	FlexPWM0	l				
	PCR[106]	ALT0	GPIO[106]	SIU Lite	I/O	Slow	Medium		77
		ALT1	_	_	_				
G[10]		ALT2	_	_	_				
		ALT3	_	_	_				
		_	FAULT[2]	FlexPWM0	l				
G[11]	PCR[107]	ALT0	GPIO[107]	SIU Lite	I/O	Slow	Medium	_	75
		ALT1	_	_	_				
		ALT2	_	_	_				
		ALT3	_	_	_				
		_	FAULT[3]	FlexPWM0	I				

<sup>1.</sup> ALT0 is the primary (default) function for each port after reset.

- 5. Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
- 6. Weak pull down during reset.

## 3.4 CTU / ADCs / FlexPWM / eTimers connections

Figure 9 shows the interconnections between the CTU, ADCs, FlexPWM, and eTimers.

<sup>2.</sup> Alternate functions are chosen by setting the values of the PCR[PA] bitfields inside the SIU module. PCR[PA] = 00 → ALT0; PCR[PA] = 01 → ALT1; PCR[PA] = 10 → ALT2; PCR[PA] = 11 → ALT3. This is intended to select the output functions; to use one of the input-only functions, the PCR[IBE] bit must be written to '1', regardless of the values selected in the PCR[PA] bitfields. For this reason, the value corresponding to an input only function is reported as "—".

<sup>3.</sup> Module included on the MCU.

<sup>4.</sup> Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMI[PADSELx] bitfields inside the SIUL module.