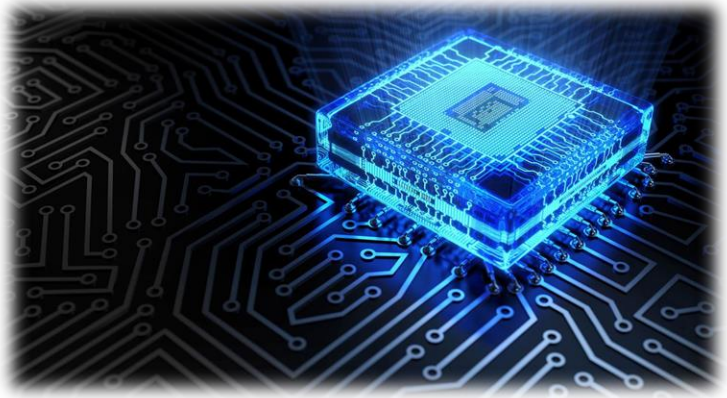
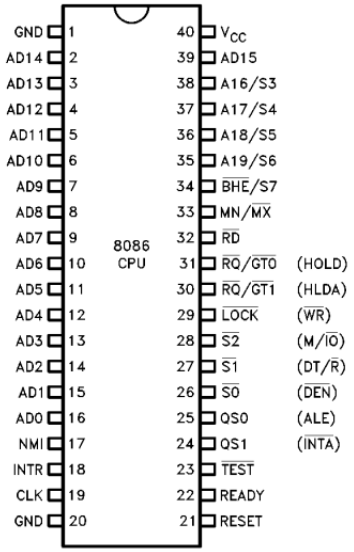


MICROPROCESSORS AND INTERFACING SYSTEMS

Dr. Amr Elkholy

Lecture 8: 8086/8088 Hardware Specifications (Part2)

PREVIOUS



TODAY

✓8086/8088 HW Specs (Ch9)

- Pin-Outs and Pin Function
- Clock Generator
- Bus Buffering and Latching

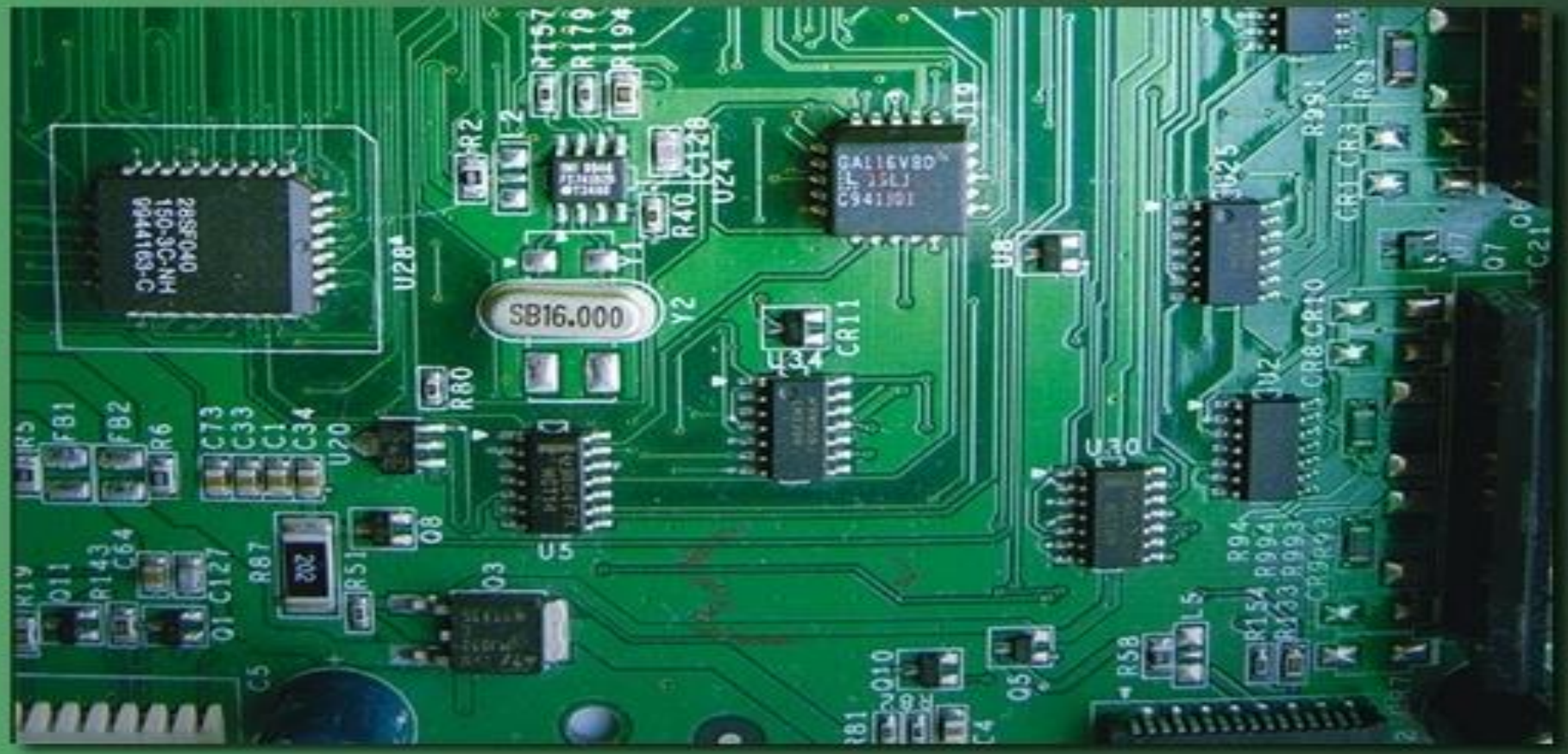
✓8086/8088 HW Specs (Ch9)

- Bus Timing
- Ready and The Wait State
- Minimum vs Maximum Mode

The Intel Microprocessors

8086/8088, 80186/80188, 80286, 80386, 80486 Pentium, Pentium Pro Processor, Pentium II, Pentium 4, and Core2 with 64-bit Extensions

Architecture, Programming, and Interfacing



EIGHTH EDITION

Barry B. Brey

PEARSON

CHAPTER 9: 8086/8088 HARDWARE SPECIFICATIONS (PART2)

CH9: 8086/8088 HARDWARE SPECIFICATIONS (PART2)

CH9: 8086/8088 HW SPECS

Bus Timing

Ready and the Wait State

Minimum vs Maximum Mode

CH9: 8086/8088 HW SPECS

Bus Timing

Ready and the Wait State

Minimum vs Maximum Mode

9–4 BUS TIMING

- It is essential to understand system bus timing before **choosing memory or I/O devices** for interfacing to 8086 or 8088 microprocessors.

- This section provides insight into **operation of the bus signals** and the **basic read/write timing** of the 8086/8088.

9–4 BUS TIMING

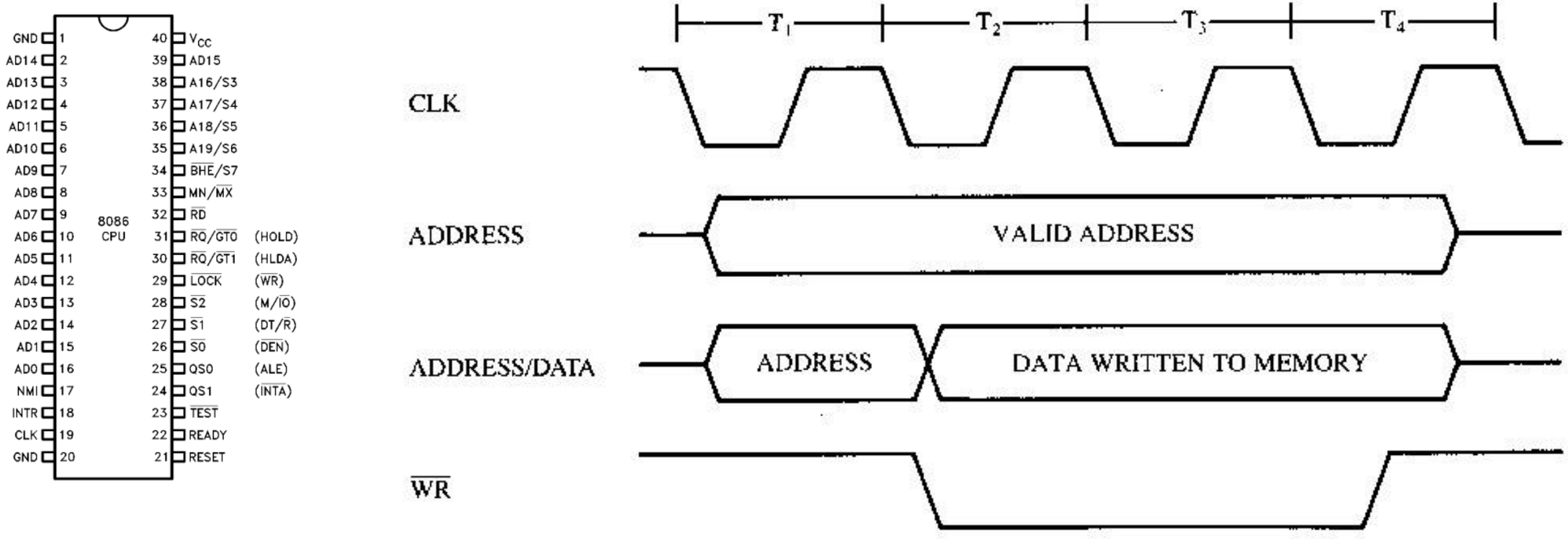
BASIC BUS OPERATION

- The **three buses of 8086/8088 function the same way** as any other microprocessor.

- If data are written to memory the processor:
  1. outputs the memory address on the address bus
  2. outputs the data to be written on the data bus
  3. issues a write ($\overline{WR}$) to memory
  4. and IO/$\overline{M}$= 0 for 8088 and $\overline{IO}$/M = 1 for 8086

- See simplified timing for write in Fig 9–9.

FIGURE 9–9 SIMPLIFIED 8086/8088 WRITE BUS CYCLE.

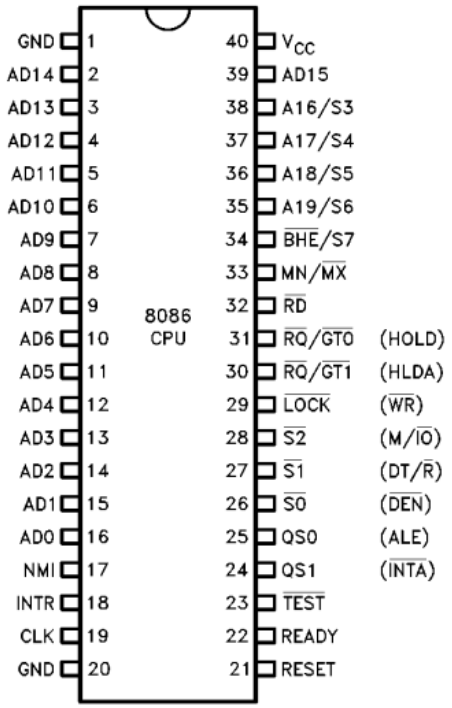


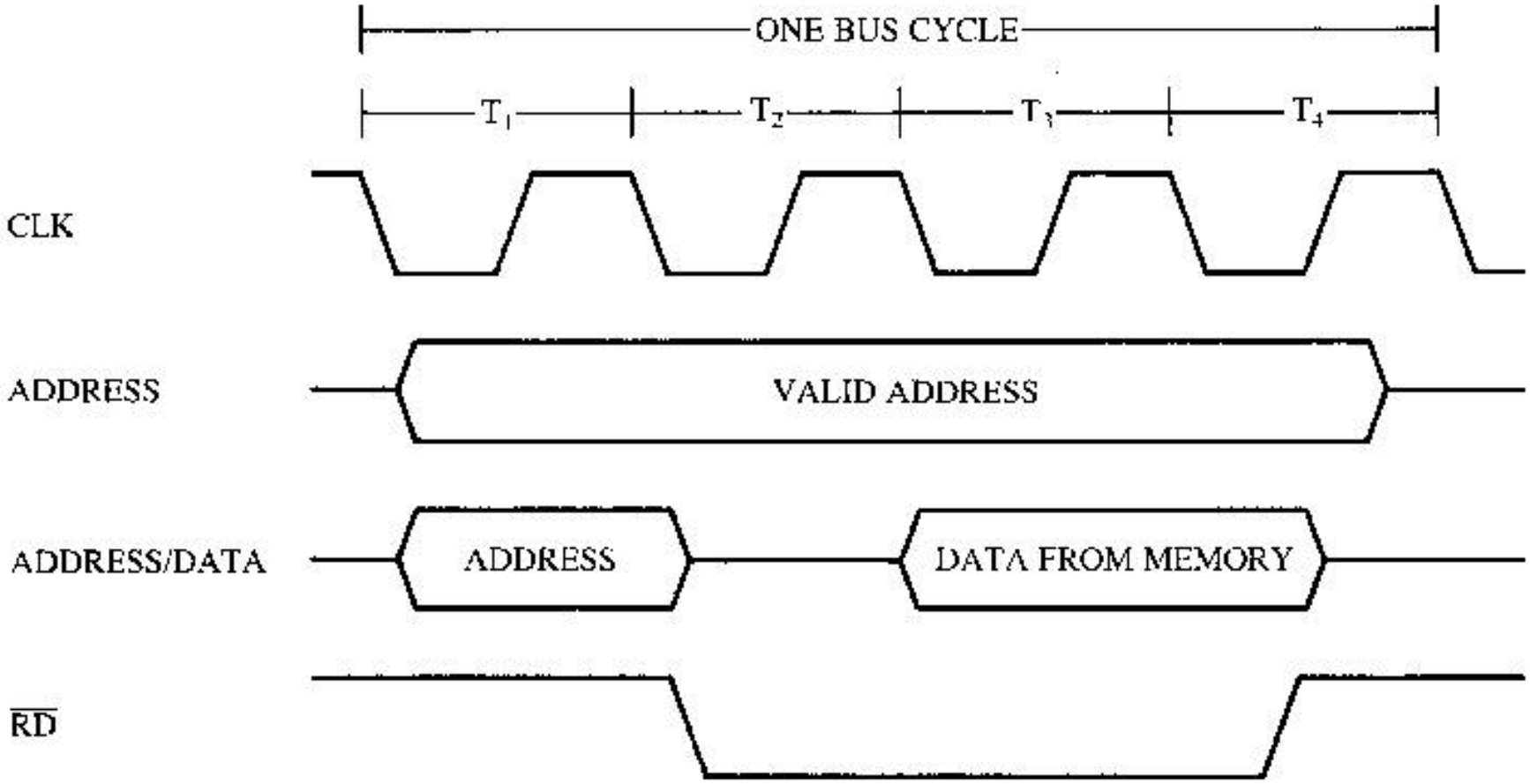
9–4 BUS TIMING

- If data are read from the memory the microprocessor:
  1. outputs the memory address on the address bus
  2. issues a read memory signal $\overline{(RD)}$
  3. and accepts the data via the data bus

- See simplified timing for read in Fig 9–10.

FIGURE 9–10 SIMPLIFIED 8086/8088 READ BUS CYCLE.





9–4 BUS TIMING

TIMING IN GENERAL

- 8086/8088 use memory and I/O in periods called **bus cycles**.

- **Each cycle equals four system-clocking periods** (T states).
  - newer microprocessors divide the bus cycle into as few as **two clocking periods**

- If the clock is operated at 5 MHz, one 8086/8088 bus cycle is complete in 800 ns.
  - basic operating frequency for these processors

9–4 BUS TIMING

- During the first clocking period in a bus cycle, **called T1**, many things happen:
  - **the address of the memory or I/O location is sent out via the address bus** and the address/data bus connections.

- During **TI, control signals are also output.**
  - indicating whether the address bus contains a **memory address or an I/O device (port) number**

- During **T2**, the processors issue the **$\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal, $\overline{\text{DEN}}$**, and in **the case of a write, the data to be written appear on the data bus.**

9–4 BUS TIMING

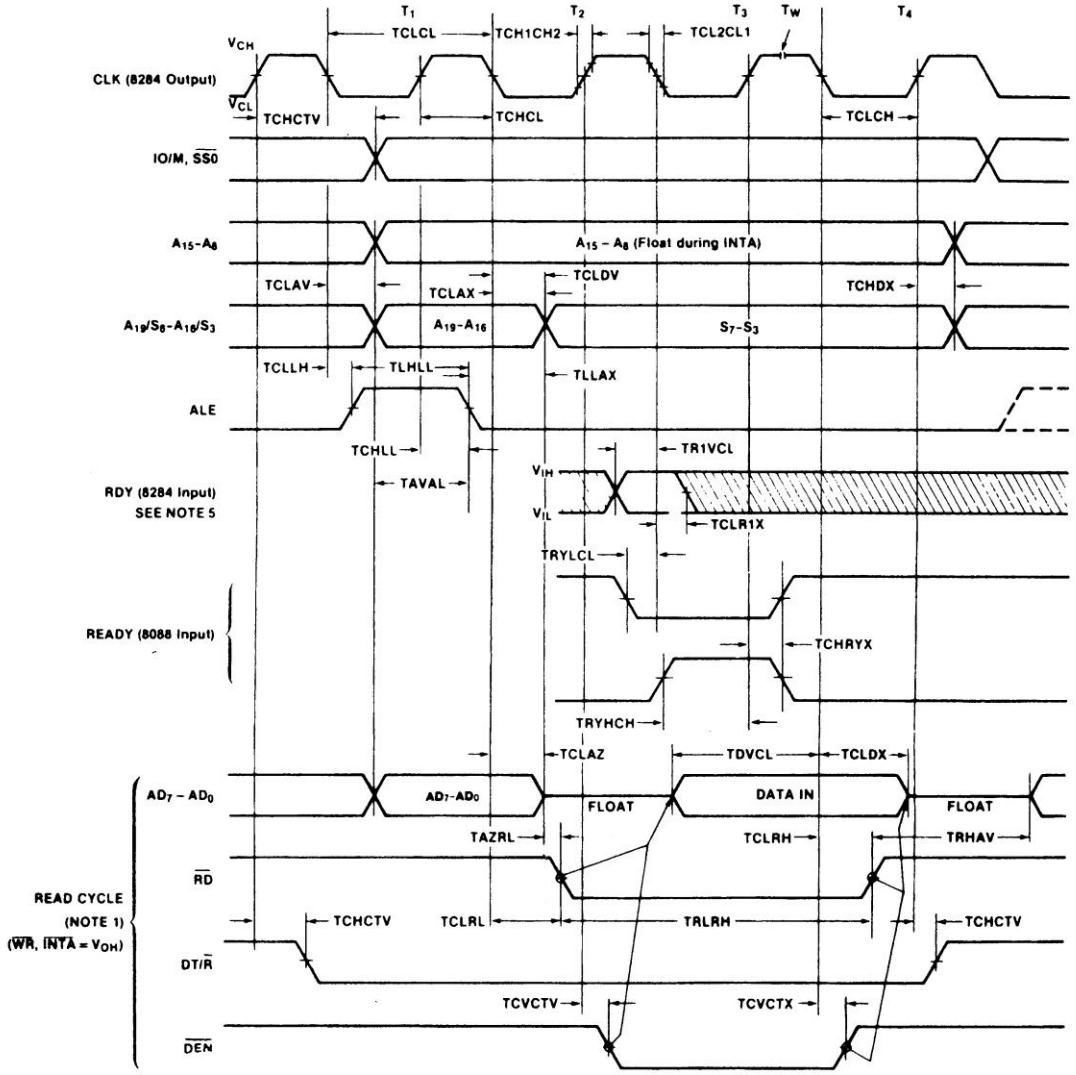
- These events cause the memory or I/O device to begin to perform a read or a write.

- **READY is sampled at the end of T2.**
  - if low at this time, **T3 becomes a wait state (Tw)**
  - this clocking period is provided to allow the memory time to access data

- If a **read** bus cycle, **the data bus is sampled at the end of T3.**

- Illustrated in Figure 9–11.

FIGURE 9–11 MINIMUM MODE 8088 BUS TIMING FOR A READ OPERATION.



- To find memory access time in this diagram:
  - locate the point in T_3 when data are sampled
  - you will notice a line that extends from the end of T_3 down to the data bus
  - at the end of T_3, the microprocessor samples the data bus.

  - **In T_4, all bus signals are deactivated in preparation for the next bus cycle**

9–4 BUS TIMING

READ TIMING

- Figure 9–11 also depicts 8088 read timing.
  - 8086 has 16 rather than eight data bus bits
- Important item in the read timing diagram is **time allowed for memory & I/O to read data.**
- Memory is chosen by its **access time**.
  - the fixed amount of time the microprocessor allows it to access data for the read operation

- It is extremely important that memory chosen complies with the limitations of the system.

9–4 BUS TIMING

- The microprocessor timing diagram **does not provide a listing for memory access time.**
  - necessary to combine several times to arrive at the access time
- **Memory access time starts when the address appears on the memory address bus and continues until the microprocessor samples the memory data at T3.**
  - about **three T states** elapse between these times
- The address does not appear until T_{CLAV} time (110 ns if a 5 MHz clock) after the start of T1.

9–4 BUS TIMING

- **T_{CLAV} time must be subtracted from the three clocking states** (600 ns) separating the appearance of the address (T1) and the sampling of the data (T3).

- The **data setup time (T_{DVCL})**, which occurs before T3 must also be subtracted.

- Memory access time is thus **three clocking states minus the sum of T_{CLAV} and T_{DVCL}**.

- Because T_{DVCL} is 30 ns with a 5 MHz clock, the allowed memory access time is only **460 ns** (access time = 600 ns –110 ns – 30 ns).

9–4 BUS TIMING

- Memory devices chosen for connection to the 8086/8088 operating at 5 MHz **must be able to access data in less than 460 ns.**
  - because of the time delay introduced by the address decoders and buffers in the system **a 30- or 40-ns margin should exist** for the operation of these circuits

- The memory speed should be **no slower than about 420 ns** to operate correctly with the 8086/8088 microprocessors.

9–4 BUS TIMING

STROBE WIDTH

- The other timing factor to affect memory operation is the **width of the RD strobe.**
- On the timing diagram, the read strobe is given as T_{RLRH}.
- The time for this strobe at a 5 MHz clock rate is **325 ns**.
- This is wide enough for almost all memory devices manufactured with an access time of 400 ns or less.

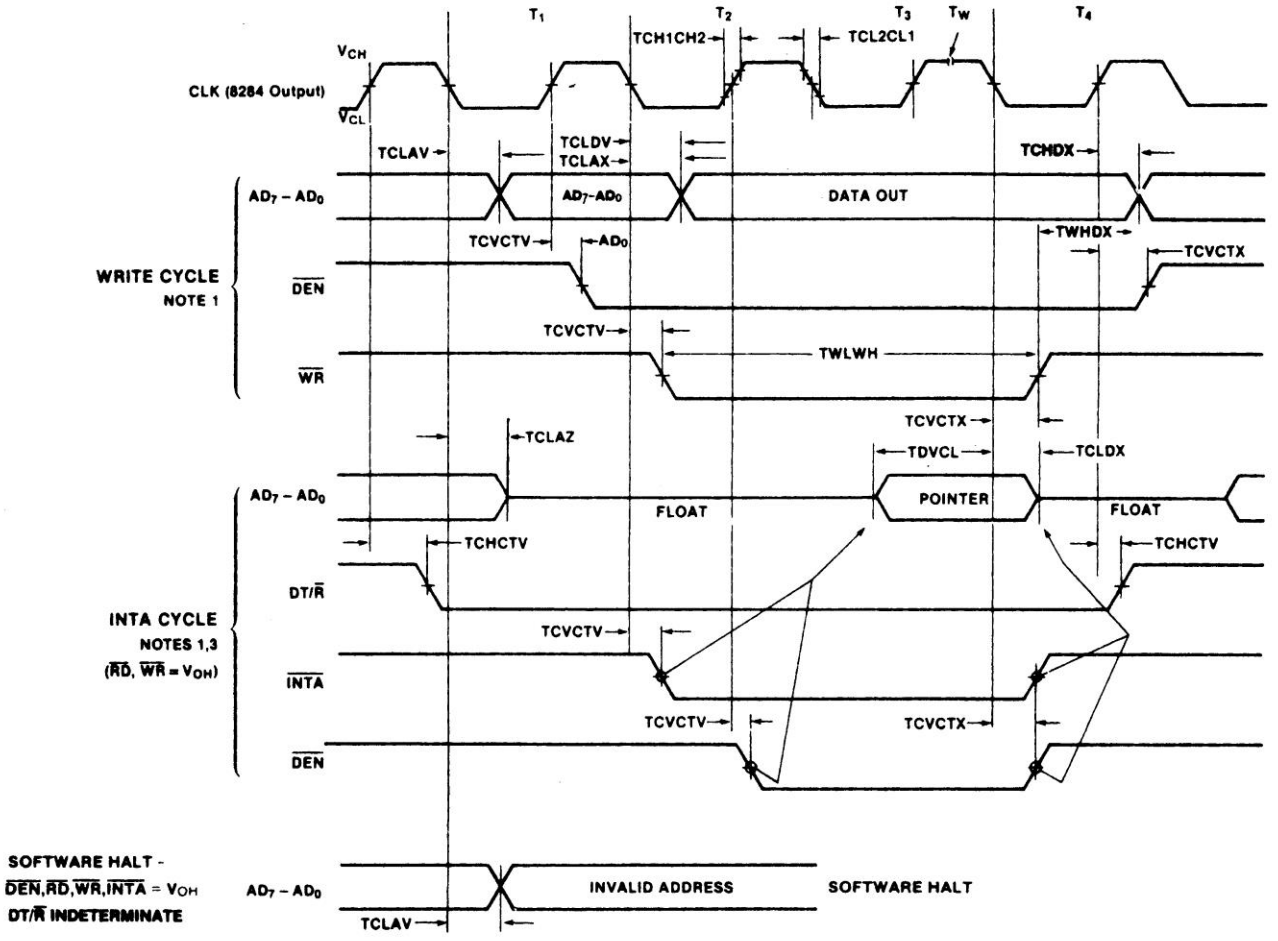
9–4 BUS TIMING

WRITE TIMING

- Figure 9–13 illustrates 8088 write-timing.
  - 8086 is nearly identical

- The $\overline{RD}$ strobe is replaced by the $\overline{WR}$ strobe,
  - the data bus contains information for the memory rather than information from the memory,
  - DT/$\overline{R}$ remains a logic 1 instead of a logic 0 throughout the bus cycle

FIGURE 9–13 MINIMUM MODE 8088 WRITE BUS TIMING.



NOTES:
1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2, T_3, T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL SIGNALS ARE SHOWN FOR THE SECOND INTA CYCLE.
4. SIGNALS AT 8284 ARE SHOWN FOR REFERENCE ONLY.
5. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED

9–4 BUS TIMING

- Memory data are written at the trailing edge of the $\overline{WR}$ strobe.
- On the diagram, this critical period is T_{WHDX} or 88 ns when 8088 on a 5 MHz clock.
- The width of the $\overline{WR}$ strobe is T_{WLWH} or 340 ns with a 5 MHz clock.
- This rate is compatible with most memory devices with access time of 400 ns or less.

Bus Timing

Ready and the Wait State

Minimum vs Maximum Mode

CH9: 8086/8088 HW SPECS

9–5 READY AND THE WAIT STATE

- The READY input **causes wait states for slower memory and I/O components.**
  - **a wait state (Tw) is an extra clocking period between T2 and T3** to lengthen bus cycle
  - on one wait state, memory access time of 460 ns, is lengthened by one clocking period (200 ns) to 660 ns, based on a 5 MHz clock

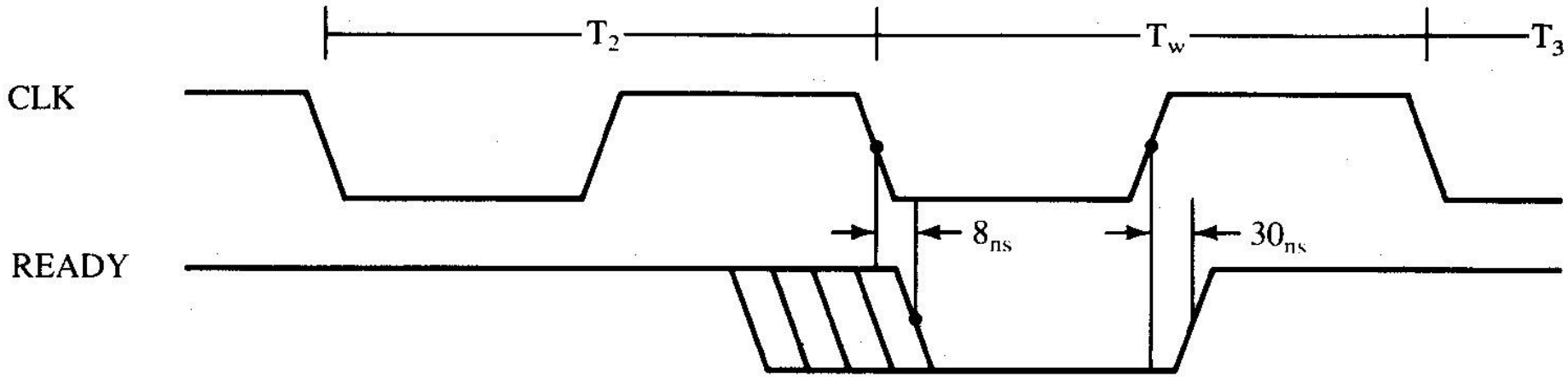
- This section covers READY synchronization circuitry inside the 8284A clock generator.

9–5 READY AND THE WAIT STATE

THE READY INPUT

- The READY input is sampled at **the end of T2** and again, if applicable, in **the middle of Tw.**
- The READY input to 8086/8088 has stringent timing requirements.
- Fig 9–14 shows READY causing one wait state (Tw), with the required setup and hold times from the system clock.
- When the 8284A is used for READY, the RDY (ready input to 8284A) input occurs at the end of each T state.

FIGURE 9–14 8086/8088 READY INPUT TIMING.



- If READY is logic 0 at the end of T_2, T_3 is delayed and T_w inserted between T_2 and T_3.
- READY is next sampled at the middle of T_w to determine if the next state is **T_w or T_3**.

9–5 READY AND THE WAIT STATE

RDY AND THE 8284A

- RDY is the synchronized ready input to the 8284A clock generator.

- Internal 8284A circuitry guarantees the accuracy of the READY synchronization.

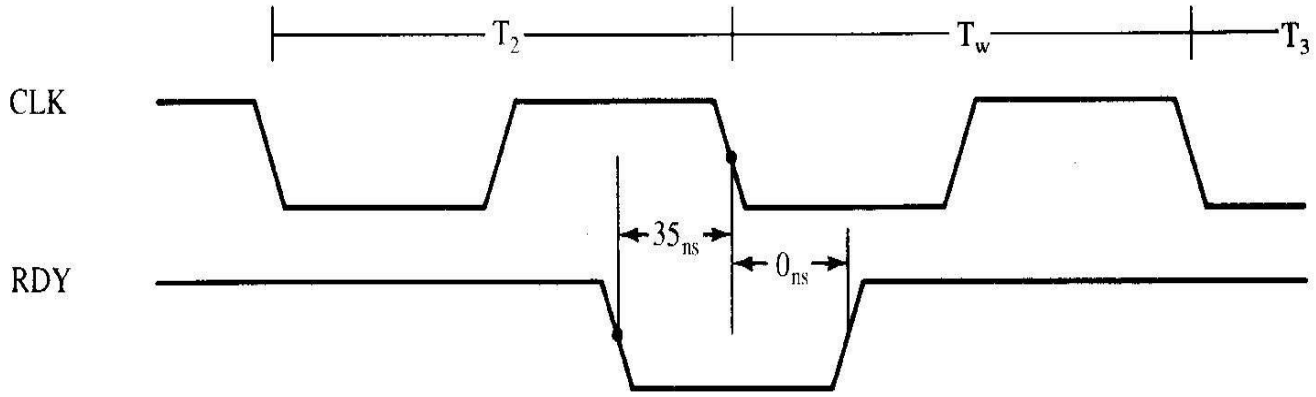


Figure 9–15 8284A RDY input timing

FIGURE 9–16 THE INTERNAL BLOCK DIAGRAM OF THE 8284A CLOCK GENERATOR.

- Fig 9–16 depicts internal structure of 8284A.
  - the bottom half is the READY synch circuitry

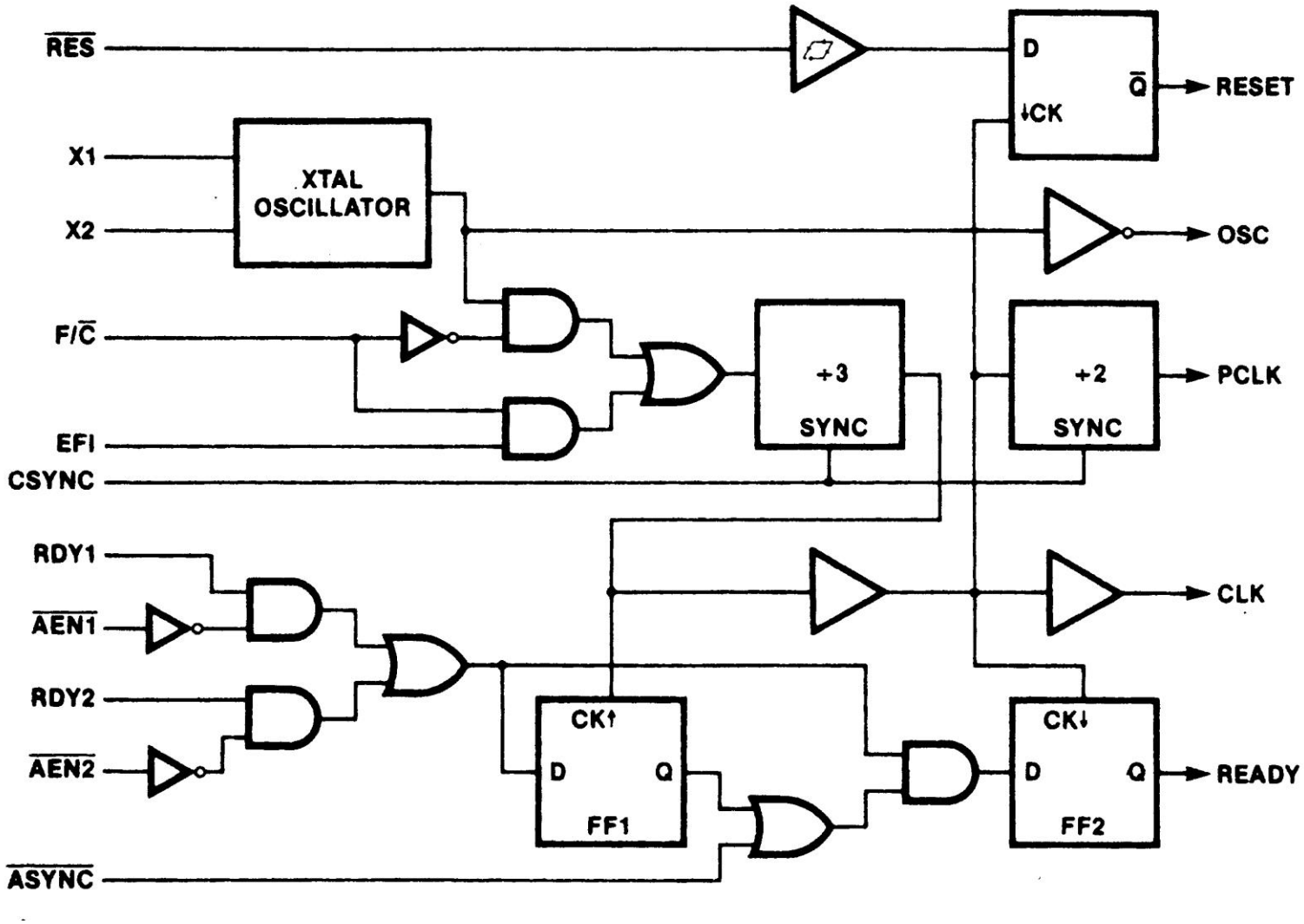
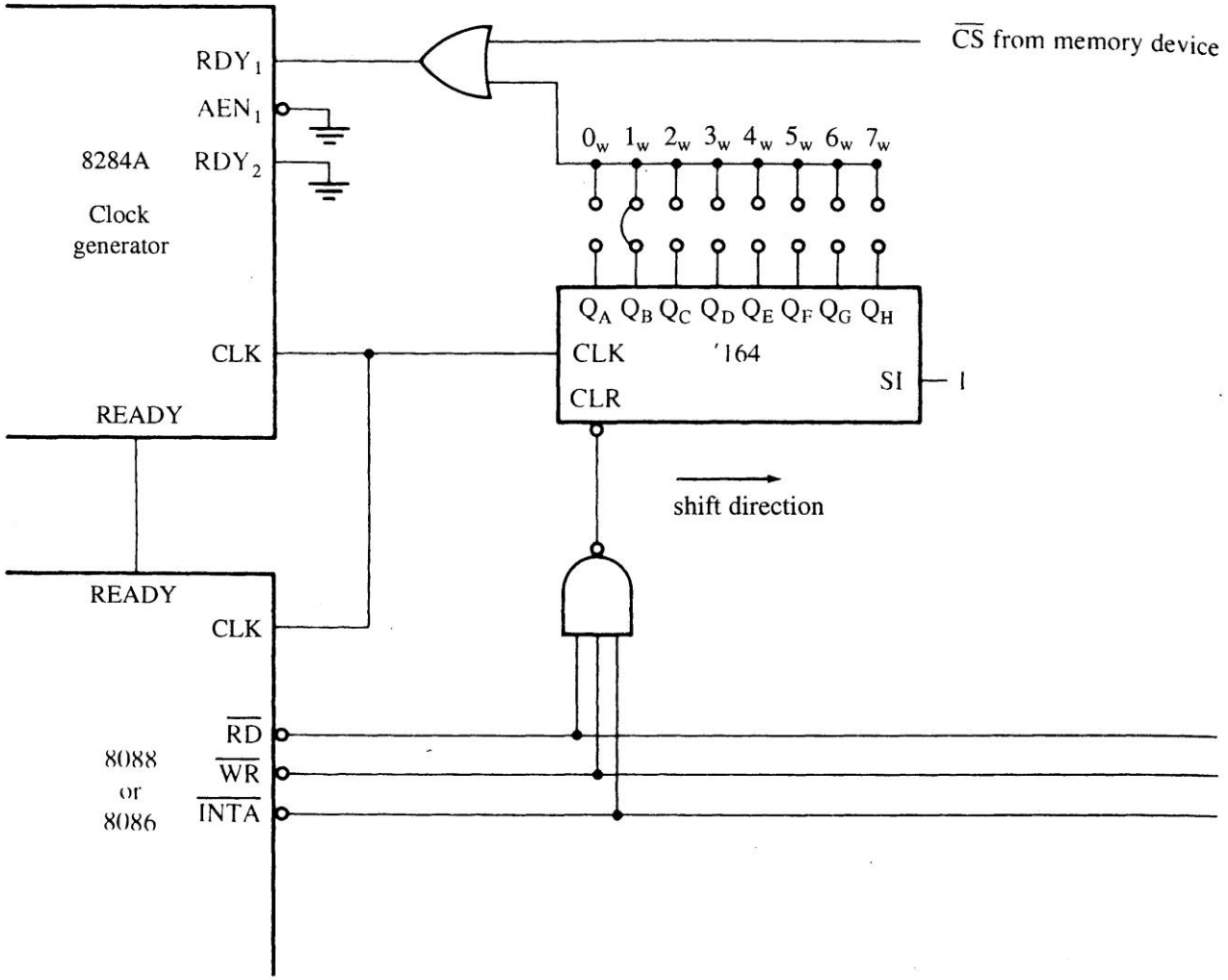


FIGURE 9–17 A CIRCUIT THAT WILL CAUSE BETWEEN 0 AND 7 WAIT STATES.

- An 8-bit serial shift register (74LS164) shifts a logic 0 for one or more clock periods from one of its Q outputs through to the RDY1 input of the 8284A.
- With appropriate strapping, this circuit can provide various numbers of wait states.



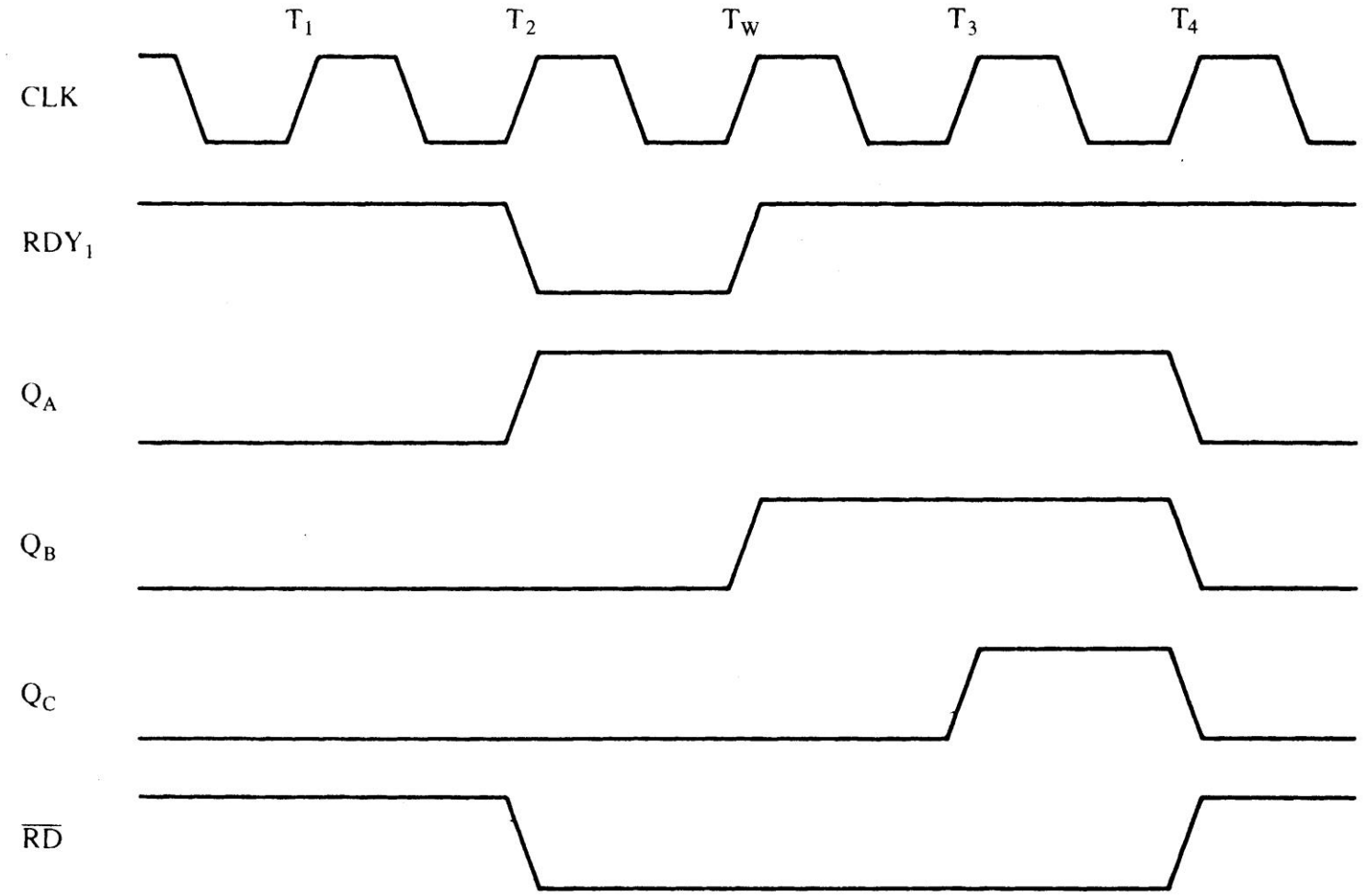
9–5 READY AND THE WAIT STATE

- Note in Fig 9–17 that this circuit is enabled only for devices that need insertion of waits.
  - if the selection signal is a logic 0, the device is selected and this circuit generates a wait state

- Figure 9–18 shows timing of this shift register wait state generator when wired to insert one wait state.

- In this example, one wait state is generated.

FIGURE 9–18 WAIT STATE GENERATION TIMING OF THE CIRCUIT OF FIGURE 9–17.



CH9: 8086/8088 HW SPECS

Bus Timing

Ready and the Wait State

Minimum vs Maximum Mode

9–6 MINIMUM VS MAXIMUM MODE

- Minimum mode is obtained by connecting the mode selection MN/$\overline{MX}$ pin to +5.0 V,
  - maximum mode selected by grounding the pin

- The mode of operation provided by **minimum mode** is similar to that of the **8085A**
  - the most recent Intel 8-bit microprocessor

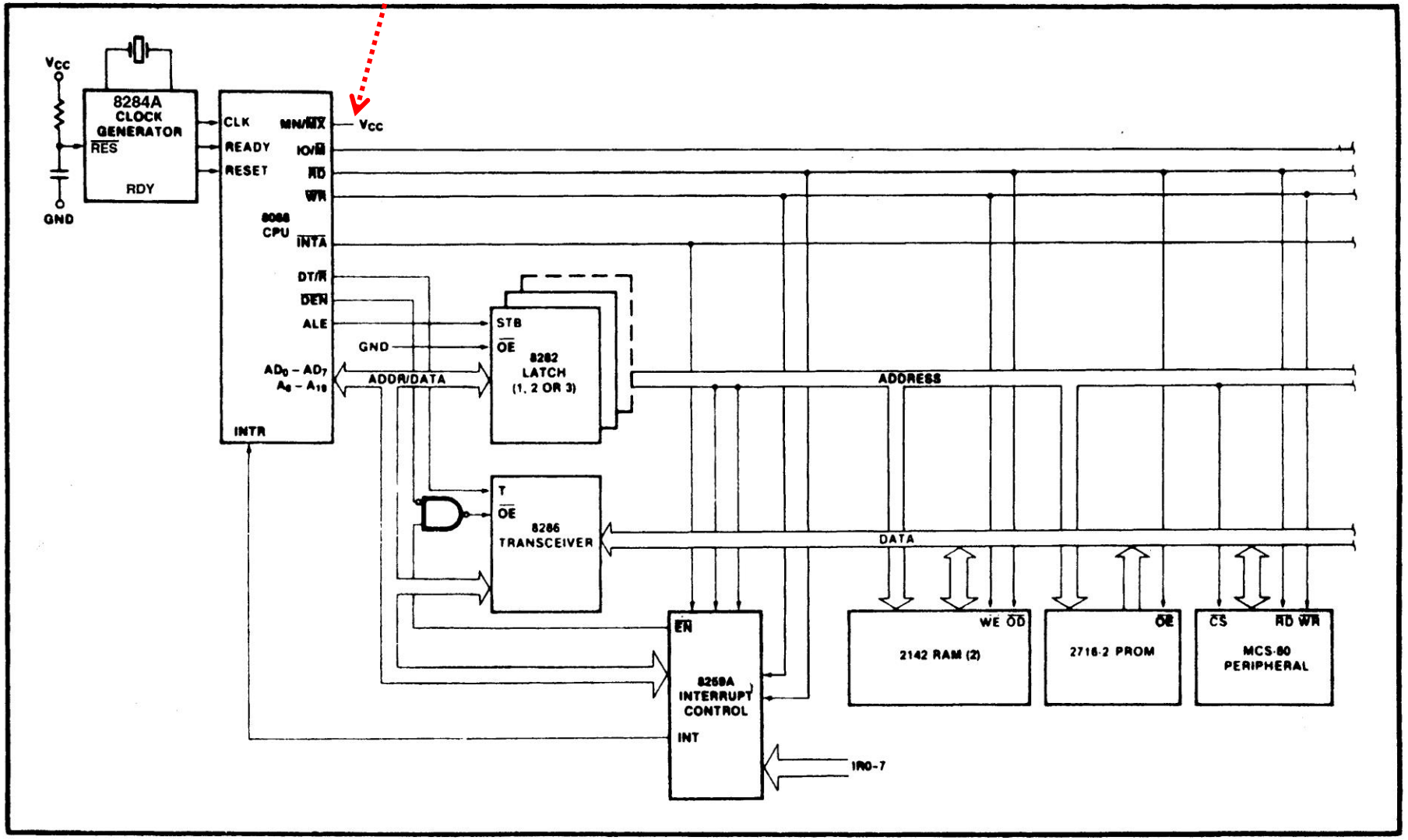
- Maximum mode is designed to be **used whenever a coprocessor exists in a system.**
  - maximum mode was dropped with 80286

9–6 MINIMUM VS MAXIMUM MODE

MINIMUM MODE OPERATION

- Least expensive way to operate 8086/8088.
  - because all control signals for the memory & I/O are generated by the microprocessor
- Control signals are identical to Intel 8085A.
- The minimum mode allows 8085A 8-bit peripherals to be used with the 8086/8088 without any special considerations.

FIGURE 9–19 MINIMUM MODE 8088 SYSTEM.



9–6 MINIMUM VS MAXIMUM MODE

MAXIMUM MODE OPERATION

- Differs from minimum mode in that **some control signals must be externally generated.**
  - requires addition of the **8288 bus controller**
- There are not enough pins on the 8086/8088 for bus control during maximum mode
  - new pins and features replaced some of them
- Maximum mode used only **when the system contains external coprocessors such as 8087.**

9–6 MINIMUM VS MAXIMUM MODE

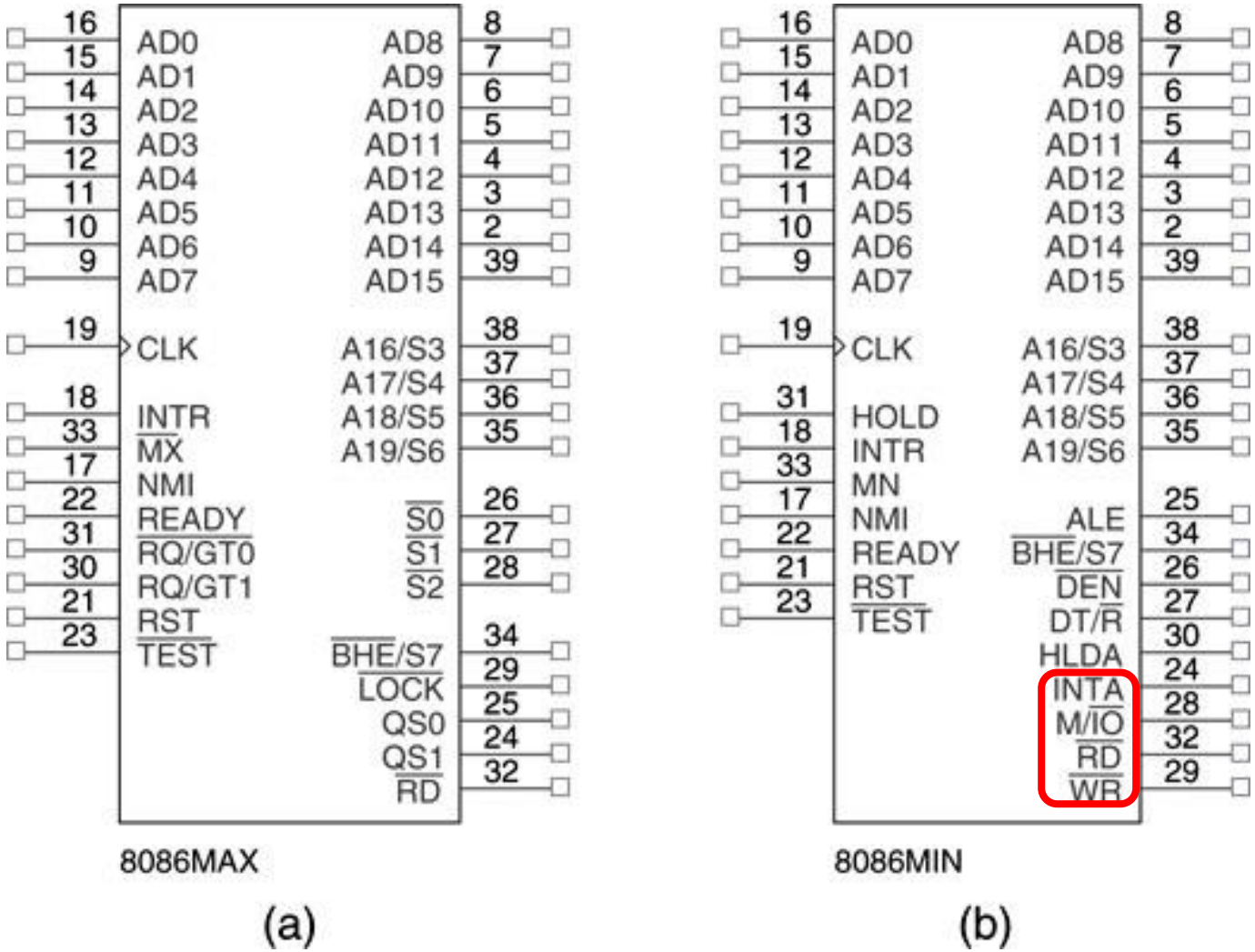
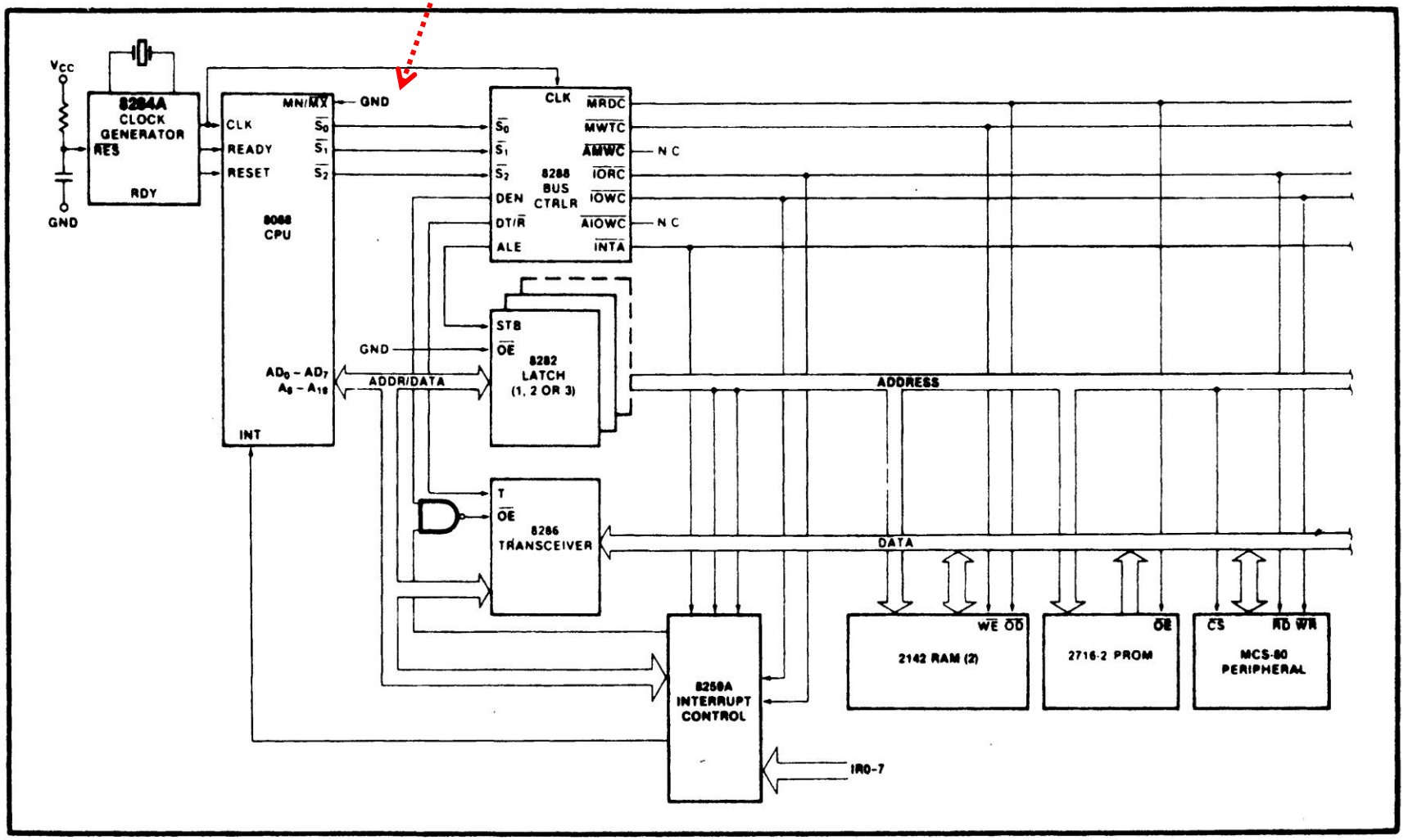


FIGURE 9–20 MAXIMUM MODE 8088 SYSTEM.



9–6 MINIMUM VS MAXIMUM MODE

THE 8288 BUS CONTROLLER

- Provides the signals eliminated from the 8086/8088 by the maximum mode operation.

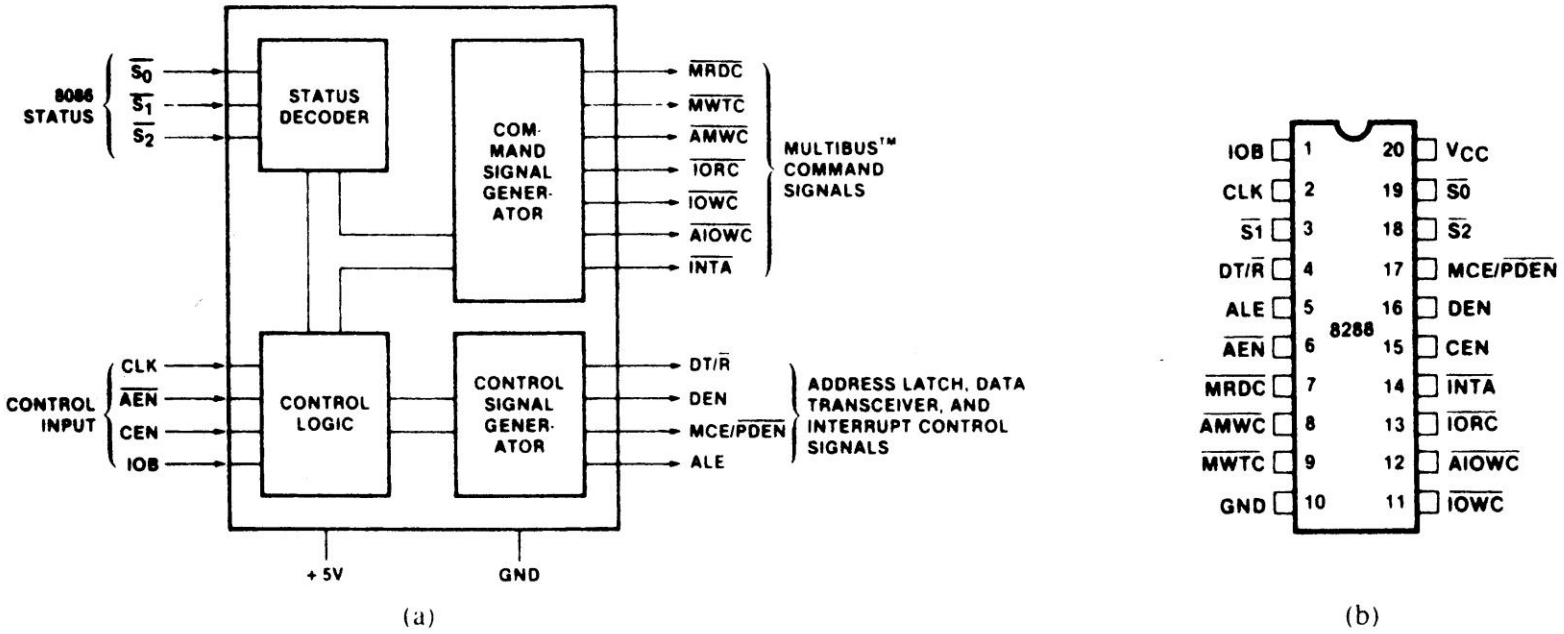


Figure 9–21 The 8288 bus controller; (a) block diagram and (b) pin-out.

9–6 MINIMUM VS MAXIMUM MODE

8288 BUS CONTROLLER *PIN FUNCTIONS* S_2, S_1, AND S_0

- Status inputs are connected to the status output pins on 8086/8088.
  - three signals decoded to generate timing signals

CLK

- The clock input provides internal timing.
  - must be connected to the CLK output pin of the 8284A clock generator

9–6 MINIMUM VS MAXIMUM MODE

8288 BUS CONTROLLER *PIN FUNCTIONS*

ALE

- The address latch enable output is used to demultiplex the address/data bus.

DEN

- The **data bus enable** pin controls the bidirectional data bus buffers in the system.

DT/$\overline{R}$

- **Data transmit/receive** signal output to control direction of the bidirectional data bus buffers.

9–6 MINIMUM VS MAXIMUM MODE

8288 BUS CONTROLLER *PIN FUNCTIONS*

$\overline{\text{AEN}}$

- The address enable input causes the 8288 to enable the memory control signals.

CEN

- The **control enable** input enables the command output pins on the 8288.

IOB

- The **I/O bus mode** input selects either I/O bus mode or system bus mode operation.

9–6 MINIMUM VS MAXIMUM MODE

8288 BUS CONTROLLER *PIN FUNCTIONS*

AIOWC

- Advanced I/O write is a command output to an advanced I/O write control signal.

IORC

- The **I/O read command** output provides I/O with its read control signal.

IOWC

- The **I/O write command** output provides I/O with its main write signal.

9–6 MINIMUM VS MAXIMUM MODE

8288 *PIN FUNCTIONS*

$\overline{\text{AMWT}}$

- Advanced memory write control pin provides memory with an early/advanced write signal.

MWTC

- The **memory write control** pin provides memory with its normal write control signal.

$\overline{\text{MRDC}}$

- The **memory read control** pin provides memory with a read control signal.

9–6 MINIMUM VS MAXIMUM MODE

8288 BUS CONTROLLER *PIN FUNCTIONS*

$\overline{\text{INTA}}$

- The interrupt acknowledge output acknowledges an interrupt request input applied to the INTR pin.

MCE/$\overline{\text{PDEN}}$

- The **master cascade/peripheral data output** selects cascade operation for an interrupt controller if IOB is grounded, and enables the I/O bus transceivers if IOB is tied high.

SUMMARY

✓8086/8088 HW Specs (Part2)

- Bus Timing
- Ready and the Wait State
- Minimum VS Maximum Mode

NEXT

✓Memory Interface (Part1)

- Memory Devices
- Addressing Decoding


THE
END