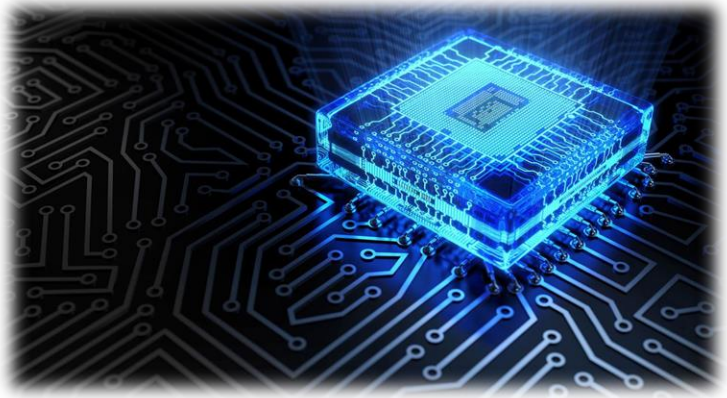


MICROPROCESSORS AND INTERFACING SYSTEMS

Dr. Amr Elkholy

Lecture 9: Memory Interface (Part1)

PREVIOUS

✓8086/8088 HW Specs (Ch9)

- Bus Timing
- Ready and The Wait State
- Minimum vs Maximum Mode

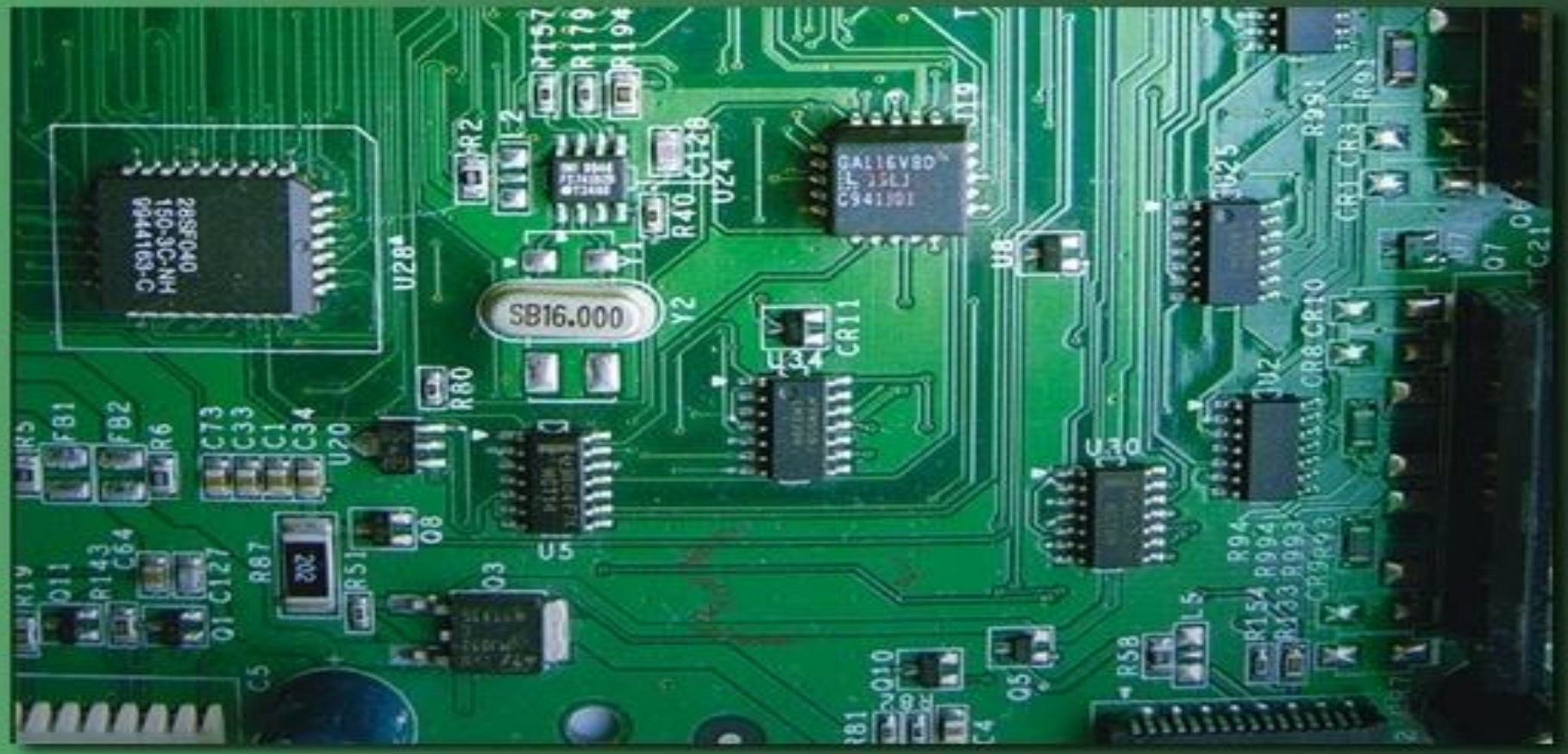
TODAY

✓Memory Interface (Ch10)

The Intel Microprocessors

8086/8088, 80186/80188, 80286, 80386, 80486 Pentium, Pentium Pro Processor, Pentium II, Pentium 4, and Core2 with 64-bit Extensions

Architecture, Programming, and Interfacing



EIGHTH EDITION

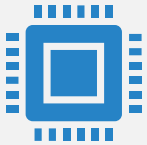
Barry B. Brey

PEARSON

CHAPTER 10: MEMORY INTERFACE (PART1)

CH10: MEMORY INTERFACE (PART1)

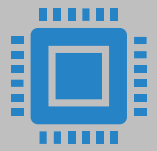
CH10: MEMORY INTERFACE



Memory Devices

Addressing Decoding

CH10: MEMORY INTERFACE



Memory Devices

Addressing Decoding

INTRODUCTION

- Simple or complex, every microprocessor-based system has a memory system.
- Almost all systems contain **two main types of memory**: read-only memory **(ROM)** and random access memory **(RAM)** or read/write memory.
- This chapter explains how to interface both memory types to the Intel family of microprocessors.

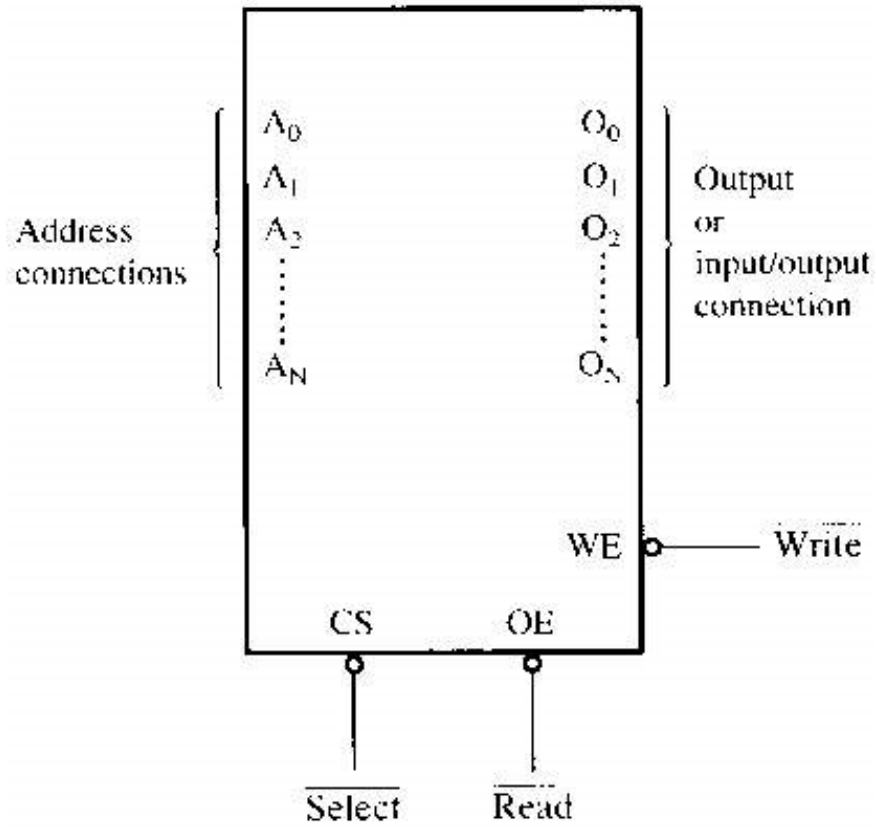
10-1 MEMORY DEVICES

- Before attempting to interface memory to the microprocessor, it is essential to **understand the operation of memory components**.

- In this section, we explain functions of the four common types of memory:
  - Read-only memory (ROM)
  - Flash memory (EEPROM)
  - Static random access memory (SRAM)
  - Dynamic random access memory (DRAM)

10-1 MEMORY DEVICES

Memory Pin Connections



- address inputs
- data outputs or input/outputs
- some type of selection input
- at least one control input to select a read or write operation

FIGURE 10–1 A PSEUDO MEMORY COMPONENT ILLUSTRATING THE ADDRESS, DATA, AND CONTROL CONNECTIONS.

10-1 MEMORY DEVICES

ADDRESS CONNECTIONS

- Memory devices have **address inputs to select a memory location within the device.**

- Almost always labeled from **A0**, the least significant address input, to **An**
  - where subscript n can be any value
  - always labeled as **one less than total number of address pins**

- A memory device with **10 address pins has its address pins labeled from A0 to A9**.

10-1 MEMORY DEVICES

ADDRESS SPACE (MAIN MEMORY: RAM)

- Address bus:10 bit →Address Space:1 Kbytes (2^{10})
- Address bus:11 bit →Address Space:2 Kbytes (2^{11})
- Address bus:16 bit →Address Space:64 KBytes (2^{16})
- Address bus:20 bit →Address Space:1 MBytes
- Address bus:32 bit →Address Space:4 GBytes
- Address bus:34 bit →Address Space:16GBytes
- Address bus:36 bit →Address Space:64GBytes
- Address bus:38 bit →Address Space:256GBytes
- Address bus:52 bit →Address Space:1015 Bytes

10-1 MEMORY DEVICES

- The number of address pins on a memory device is **determined by the number of memory locations found within it.**

- Today, common memory devices have between **1K (1024) to 1G (1,073,741,824) memory locations.**
  - with 4G and larger devices on the horizon

- A **1K memory device has 10 address pins**.
  - therefore, 10 address inputs are required to select any of its 1024 memory locations

10-1 MEMORY DEVICES

- It takes a 10-bit binary number to select any single location on a 1024-location device.
  - 1024 different combinations
  - if a device has 11 address connections, it has 2048 (2K) internal memory locations

- The number of memory locations can be **extrapolated from the number of pins.**

10-1 MEMORY DEVICES

DATA CONNECTIONS

- All memory devices have **a set of data outputs or input/outputs.**
  - today, many devices have **bidirectional common I/O pins**
  - data connections are **points at which data are entered for storage or extracted for reading**

- Data pins on memory devices are labeled **D0 through D7 for an 8-bit-wide memory device.**

10-1 MEMORY DEVICES

- An 8-bit-wide memory device is often called a **byte-wide memory.**
  - most devices are currently 8 bits wide,
  - some are 16 bits, 4 bits, or just 1 bit wide

- Catalog listings of memory devices often refer to **memory locations times bits per location.**
  - a memory device with **1K memory locations and 8 bits in each location is often listed as a 1K × 8** by the manufacturer

- Memory devices are often classified according to **total bit capacity.**

10-1 MEMORY DEVICES

SELECTION CONNECTIONS

- Each memory device **has an input that selects or enables the memory device.**
  - sometimes more than one

- This type of input is most often called a **chip select ($\overline{CS}$) chip enable ($\overline{CE}$) or simply select ($\overline{S}$)** input.

- RAM memory generally has **at least one or input, and ROM has at least one**

- If more than one $\overline{CE}$ connection is present, **all must be activated to read or write data.**

10-1 MEMORY DEVICES

CONTROL CONNECTIONS

- All memory devices have some form of control input or inputs.
  - ROM usually has **one control input**, while **RAM often has one or two control inputs**

- Control input often found on **ROM** is the **output enable or gate** connection, which **allows data flow from output data pins.**

- The $\overline{\textbf{OE}}$ connection **enables and disables a set of three-state buffers located in the device** and must be active to read data.

10-1 MEMORY DEVICES

- RAM has either one or two control inputs.
  - if one control input, it is often called **R/$\overline{W}$**

- If the RAM has two control inputs, they are usually labeled **$\overline{WE}$** (or **$\overline{W}$**), and **OE** (or **$\overline{G}$**).
  - write enable must be active to perform **memory write**, and $\overline{OE}$ active to perform a **memory read**
  - when the two controls are present, **they must never both be active at the same time**

- If both inputs are inactive, data are neither written nor read.
  - the connections are at their high-impedance state

10-1 MEMORY DEVICES

ROM MEMORY

- Read-only memory (ROM) permanently stores programs/data resident to the system.
  - and must not change when power disconnected

- Often called **nonvolatile memory**, because **its contents do not change even if power is disconnected**.

- A device we call a ROM is purchased in mass quantities from a manufacturer.
  - programmed during fabrication at the factory

10-1 MEMORY DEVICES

- The **EPROM (erasable programmable read-only memory)** is commonly used **when software must be changed often.**
  - or when low demand makes ROM uneconomical
  - for ROM to be practical at least 10,000 devices must be sold to recoup factory charges

- An **EPROM is programmed in the field on a device called an EPROM programmer.**

- Also **erasable if exposed to high-intensity ultraviolet light**.
  - depending on the type of EPROM

10-1 MEMORY DEVICES

- **PROM** memory devices are also available, although they **are not as common today.**

- The PROM (programmable read-only memory) is also programmed in the field by **burning open tiny NI-chrome or silicon oxide fuses.**

- Once it is programmed, **it cannot be erased.**

10-1 MEMORY DEVICES

- A newer type of **read-mostly memory (RMM)** is called the **flash memory.**
  - also often called an **EEPROM (electrically erasable programmable ROM)**
  - EAROM (electrically alterable ROM)
  - or a NOVRAM (nonvolatile RAM)

- Electrically erasable in the system, but they require **more time to erase than normal RAM.**

- The **flash memory device is used to store setup information for systems** such as the **video card** in the computer.

10-1 MEMORY DEVICES

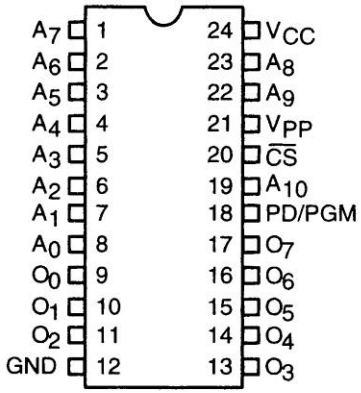
- Flash has all but **replaced the EPROM in most computer systems for the BIOS**.
  - some systems contain a password stored in the flash memory device

- Flash memory has **its biggest impact in memory cards for digital cameras and memory in MP3 audio players.**

- Figure 10–2 illustrates the 2716 EPROM, which is representative of most common EPROMs.

FIGURE 10–2 THE PIN-OUT OF THE 2716, 2K × 8 EPROM. (COURTESY OF INTEL CORPORATION.)

PIN CONFIGURATION



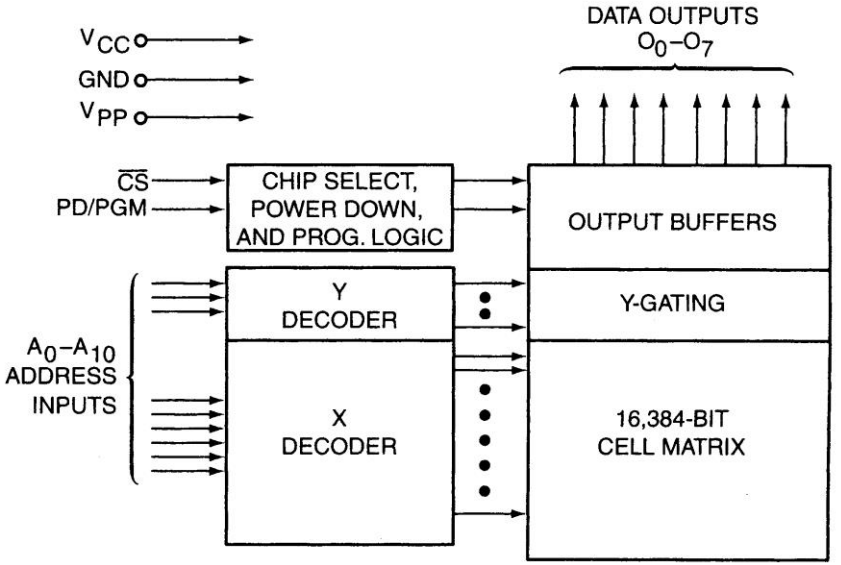
MODE SELECTION

MODE \ PINS	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

BLOCK DIAGRAM



10-1 MEMORY DEVICES

- Figure 10–3 illustrates the **timing diagram for the 2716 EPROM.**
- The **V_{PP} pin must be placed at a logic 1 level for data to be read from the EPROM.**-
- In some cases, the V_{PP} pin is in the same position as the $\overline{WE}$ pin on the SRAM.
- This will allow a single socket to hold either an EPROM or an SRAM.
  - an example is the 27256 EPROM and 62256 SRAM, both 32K × 8 devices with the same pin-out, except for V_{PP} on the EPROM and $\overline{WE}$ on the SRAM.

FIGURE 10–3 THE TIMING DIAGRAM OF AC CHARACTERISTICS OF THE 2716 EPROM. (COURTESY OF INTEL CORPORATION.)

A.C. Characteristics

T_A = 0°C to 70°C, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[4]	Max.		
t_{ACC1}	Address to Output Delay		250	450	ns	PD/PGM = $\overline{CS}$ = V_{IL}
t_{ACC2}	PD/PGM to Output Delay		280	450	ns	$\overline{CS}$ = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PF}	PD/PGM to Output Float	0		100	ns	$\overline{CS}$ = V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM = V_{IL}
t_{OH}	Address to Output Hold	0			ns	PD/PGM = $\overline{CS}$ = V_{IL}

Capacitance[5] T_A = 25°C, f = 1 MHz

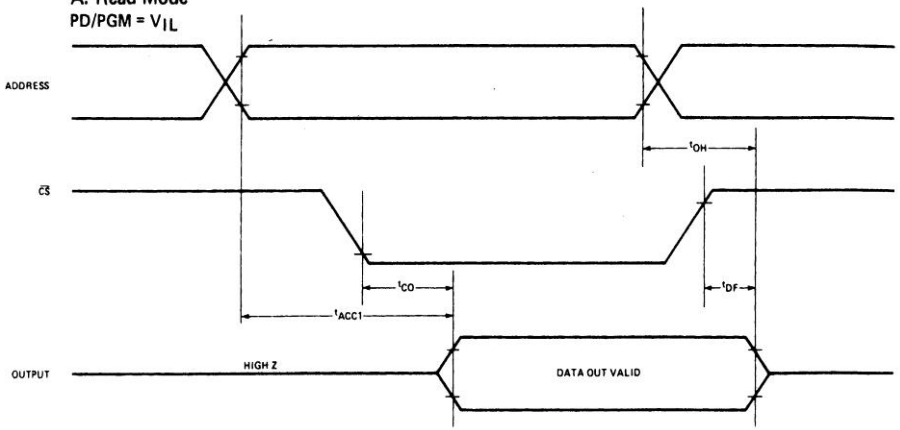
Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

A.C. Test Conditions:

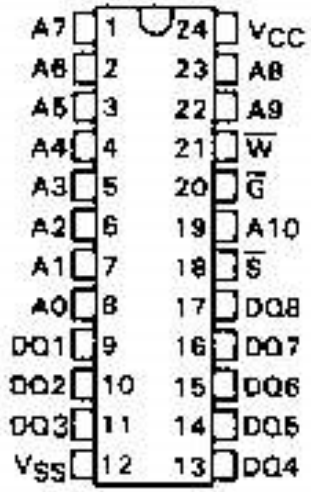
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

WAVEFORMS

A. Read Mode
PD/PGM = V_{IL}



TMS4018 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A10	Addresses
DQ1 DQ8	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

- One important piece of information provided by the timing diagram and data sheet is the memory access time
- that is the time it takes the memory to read information

10-1 MEMORY DEVICES

- The basic speed of this **EPROM is 450 ns.**
  - recall that 8086/8088 operated with a 5 MHz clock **allowed memory 460 ns to access data**

- This type of component requires wait states to operate properly with 8086/8088 because of **its rather long access time.**
  - if wait states are not desired, higher-speed EPROMs are available at additional cost
  - EPROM memory is available with **access times of as little as 100 ns**

- Obviously, wait states are required in modern microprocessors for any EPROM device.

10-1 MEMORY DEVICES

STATIC RAM (SRAM) DEVICES

- Static RAM memory devices **retain data for as long as DC power is applied.**

- Because **no special action is required to retain data, these devices are called static memory.**
  - also called **volatile memory** because they will not retain data without power

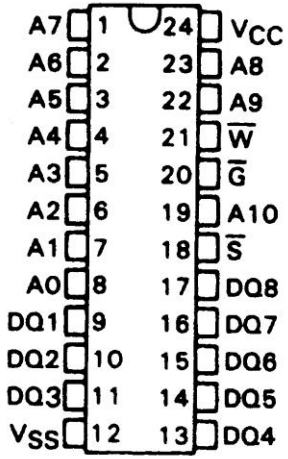
- The main difference between ROM and RAM is that RAM is **written under normal operation, whereas ROM is programmed** outside the computer and normally is only read.

10-1 MEMORY DEVICES

- Fig 10–4 illustrates the 4016 SRAM,
  - a 2K × 8 read/write memory
- This device is representative of all SRAM devices.
  - except for the number of address and data connections.
- The control inputs of this RAM are slightly different from those presented earlier.
  - however the control pins function exactly the same as those outlined previously
- Found under part numbers 2016 and 6116.

FIGURE 10–4 THE PIN-OUT OF THE TMS4016, 2K × 8 STATIC RAM (SRAM). (COURTESY OF TEXAS INSTRUMENTS INCORPORATED.)

TMS4016 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A10	Addresses
DQ1 – DQ8	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

- SRAM is used when the size of the read/write memory is relatively small
- today, a small memory is less than 1M byte

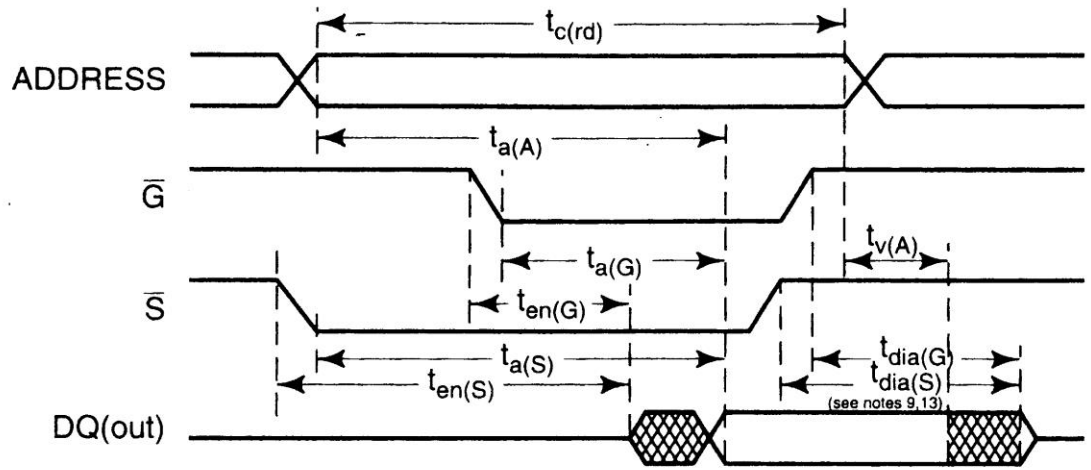
FIGURE 10-5 (A) THE AC CHARACTERISTICS OF THE TMS4016 SRAM. (B) THE TIMING DIAGRAMS OF THE TMS4016 SRAM. (COURTESY OF TEXAS INSTRUMENTS INCORPORATED.)

switching characteristics over recommended voltage range, T_A = 0°C to 70°C

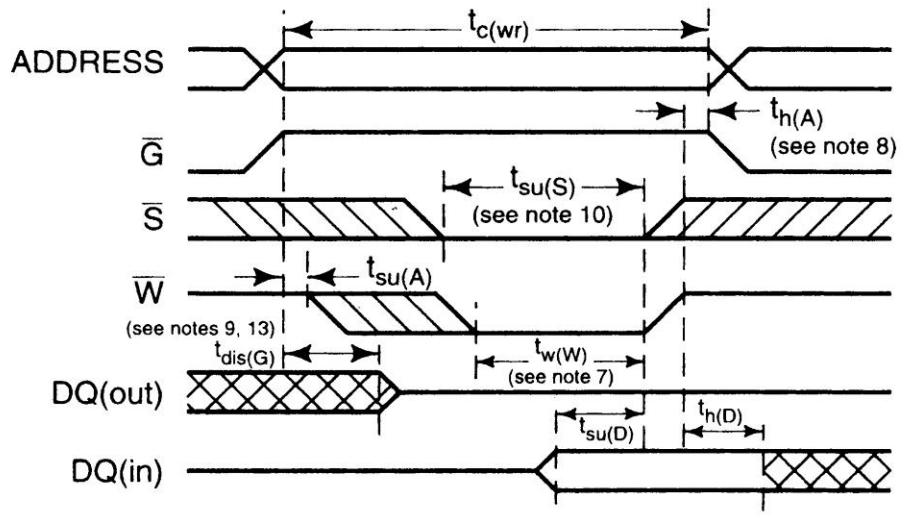
PARAMETER		TMS4016-12		TMS4016-15		TMS4016-20		TMS4016-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		120		150		200		250	ns
$t_{a(S)}$	Access time from chip select low		60		75		100		120	ns
$t_{a(G)}$	Access time from output enable low		50		60		80		100	ns
$t_{v(A)}$	Output data valid after address change	10		15		15		15		ns
$t_{dis(S)}$	Output disable time after chip select high		40		50		60		80	ns
$t_{dis(G)}$	Output disable time after output enable high		40		50		60		80	ns
$t_{dis(W)}$	Output disable time after write enable low		50		60		60		80	ns
$t_{en(S)}$	Output enable time after chip select low	5		5		10		10		ns
$t_{en(G)}$	Output enable time after output enable low	5		5		10		10		ns
$t_{en(W)}$	Output enable time after write enable high	5		5		10		10		ns

NOTES: 3. C_L = 100pF for all measurements except $t_{dis(W)}$ and $t_{en\ (W)}$.
C_L = 5 pF for $t_{dis(W)}$ and $t_{en(W)}$.
4. t_{dis} and t_{en} parameters are sampled and not 100% tested.

timing waveform of read cycle (see note 5)



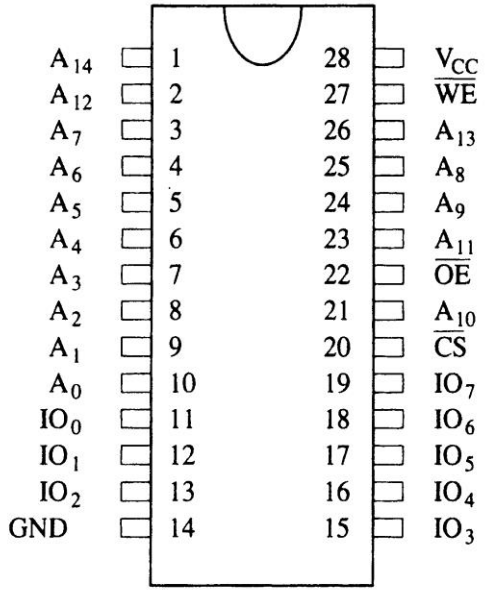
timing waveform of write cycle no. 1 (see note 6)



10-1 MEMORY DEVICES

- Figure 10–6 illustrates pin-outs of the **62256, 32K × 8 static RAM.**
- Packaged in a **28-pin integrated circuit**
- Available with access times of **120 or 150 ns**.
- Other common SRAM devices are
  - 8K × 8; 128K × 8; 256K × 8
  - 512K × 8; 1M × 8
- Access times can be as low as 1.0 ns for SRAM used in computer cache memory.

FIGURE 10–6 PIN DIAGRAM OF THE 62256, 32K × 8 STATIC RAM.



PIN FUNCTION

A_0 - A_{14}	Addresses
IO_0 - IO_7	Data connections
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V Supply
GND	Ground

10-1 MEMORY DEVICES

DYNAMIC RAM (DRAM) MEMORY

- Available up to **256M × 8 (2G bits)**.
- DRAM is essentially the same as SRAM, **except that it retains data for only 2 or 4 ms on an integrated capacitor**.
- **After 2 or 4 ms, the contents of the DRAM must be completely rewritten (refreshed)**.
  - because the capacitors, which store a logic 1 or logic 0, lose their charges

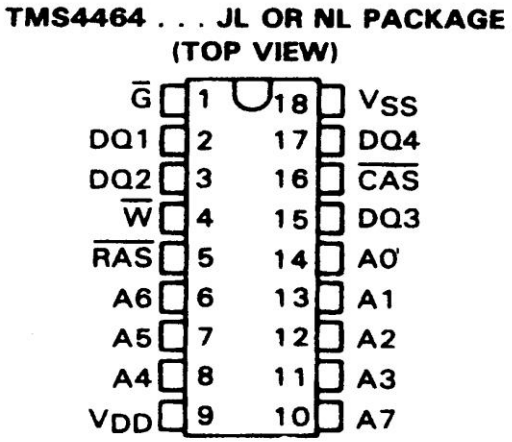
10-1 MEMORY DEVICES

- In DRAM, the entire contents are **refreshed with 256 reads in a 2- or 4-ms interval.**
  - also occurs during a write, a read, or during a special refresh cycle

- DRAM **requires so many address pins that manufacturers multiplexed address inputs.**

- Figure 10–7 illustrates a 64K × 4 DRAM, the TMS4464, which stores 256K bits of data.
  - note it contains only eight address inputs where it should contain 16—the number required to address 64K memory locations

FIGURE 10–7 THE PIN-OUT OF THE TMS4464, 64K × 4 DYNAMIC RAM (DRAM). (COURTESY OF TEXAS INSTRUMENTS INCORPORATED.)



(a)

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ4	Data-In/Data-Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

(b)

- 16 address bits can be forced into eight address pins in two 8-bit increments
- this requires two special pins: the **column address strobe** ($\overline{CAS}$) and **row address strobe** ($\overline{RAS}$)

10-1 MEMORY DEVICES

- First, A0–A7 are placed on the address pins and **strobed into an internal row latch by RAS as the row address.**
- Next, address bits A8-A15 are placed on the same eight address inputs and **strobed into an internal column latch by CAS as the column address**
- The 16-bit address in the internal latches addresses the contents of one of the 4-bit memory locations.
  - CAS also performs chip selection input to DRAM

FIGURE 10–8 $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ AND ADDRESS INPUT TIMING FOR THE TMS4464 DRAM. (COURTESY OF TEXAS INSTRUMENTS INCORPORATED.)

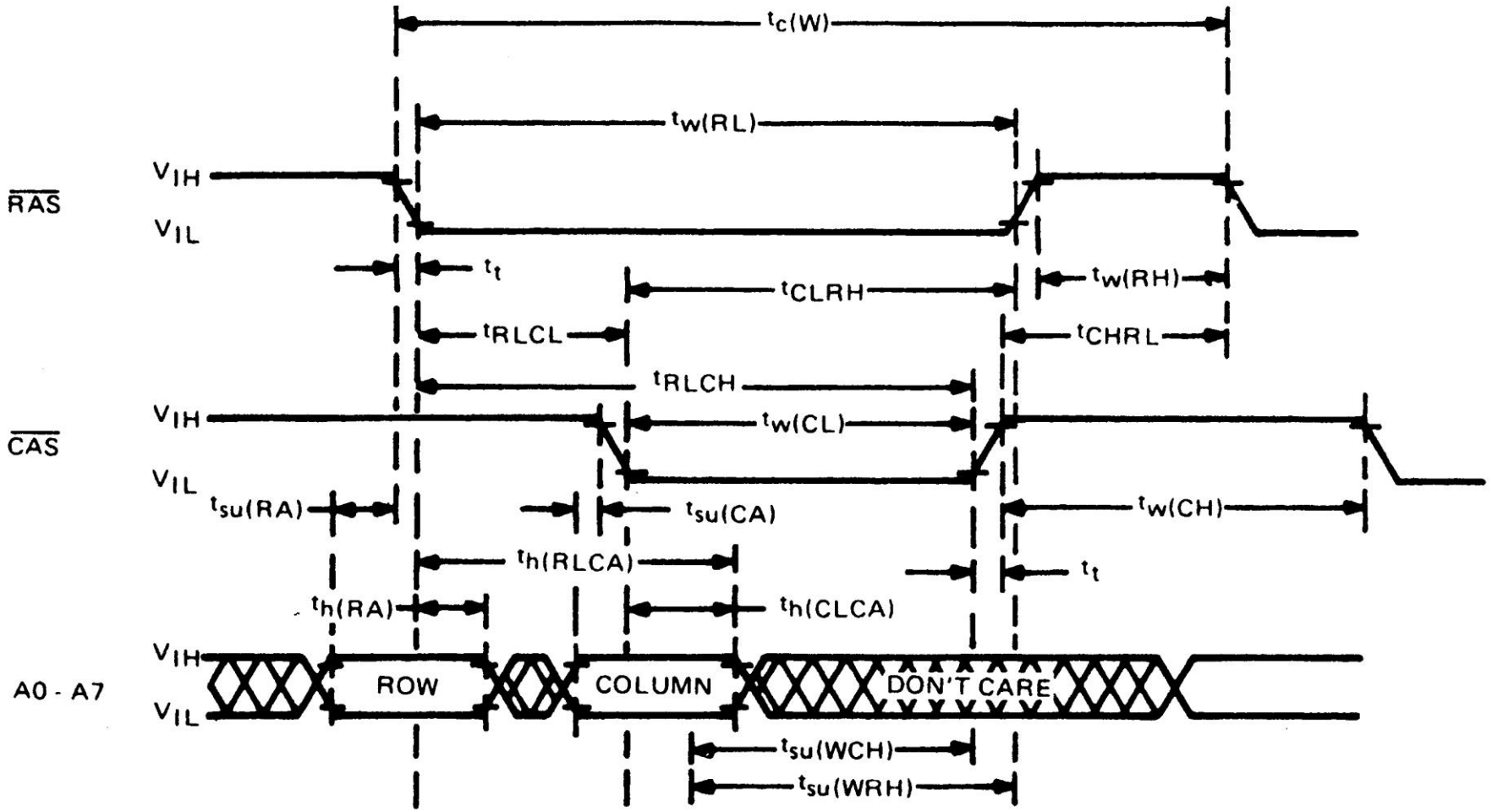
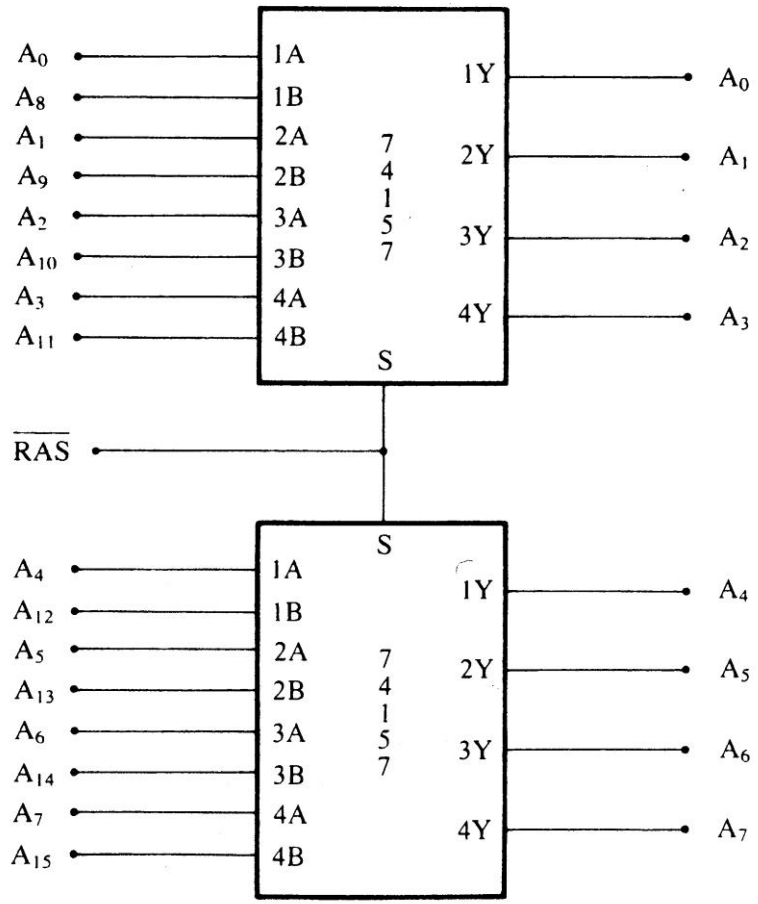
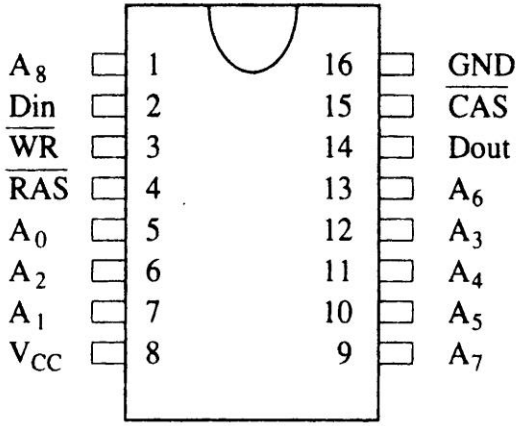


FIGURE 10–9 ADDRESS MULTIPLEXER FOR THE TMS4464 DRAM.



- multiplexers used to strobe column and row addresses into the address pins on a pair of TMS4464 DRAMs.
- the $\overline{\text{RAS}}$ signal not only strobes the row address into the DRAMs, but it also selects which part of the address is applied to the address inputs.

FIGURE 10–10 THE 41256 DYNAMIC RAM ORGANIZED AS A 256K × 1 MEMORY DEVICE.



PIN FUNCTIONS

A_0 - A_8	Addresses
Din	Data in
Dout	Data out
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{WR}$	Write enable
V_{CC}	+5V Supply
GND	Ground

- the pin-out of the 41256 dynamic RAM
- this device is organized as a 256K × 1 memory
- requires as little as 70 ns to access data

10-1 MEMORY DEVICES

- DRAM is often **placed on small boards called SIMMs (Single In-Line Memory Modules)**.

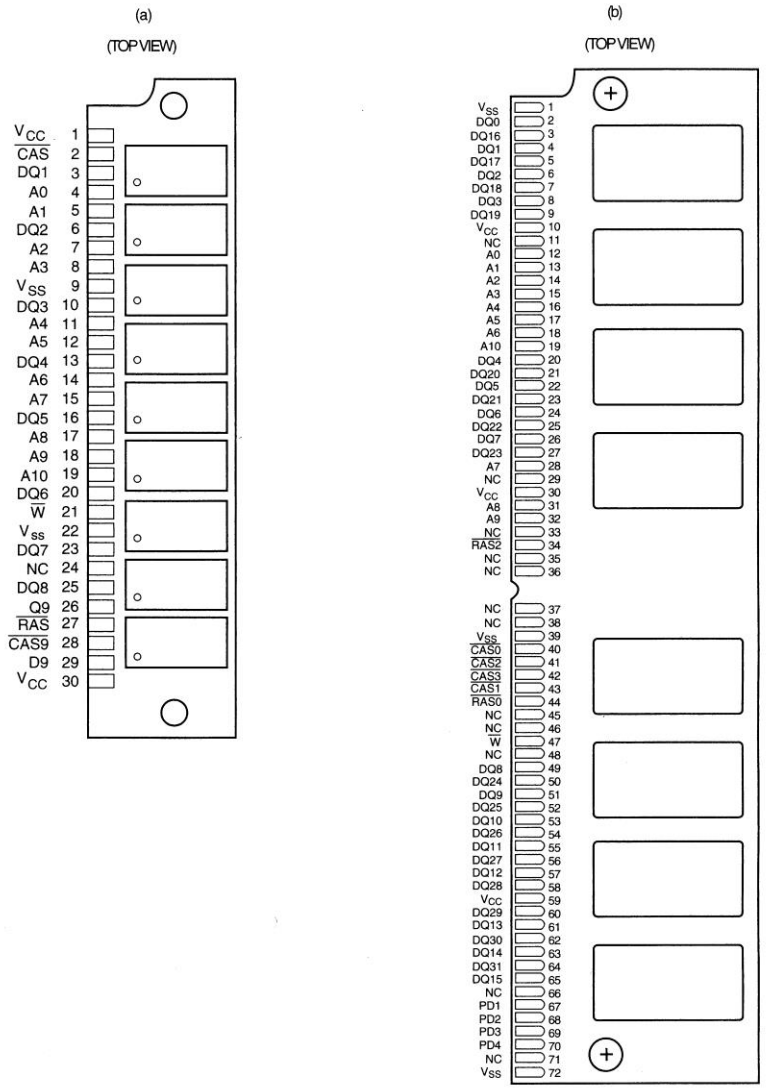
- The 30-pin SIMM is **organized most often as 1M × 8 or 1M × 9, and 4M × 8 or 4M × 9.**
  - illustrated in Fig 10–11 is a 4M × 9
  - **the ninth bit is the parity bit**

- Also shown is a newer 72 pin SIMM.

- 72-pin SIMMs are often organized as 1M × 32 or 1M × 36 (with parity).

- Fig 10–11 illustrates a 4M × 36 SIMM, which has 16M bytes of memory

FIGURE 10–11 THE PIN-OUTS OF THE 30-PIN AND 72-PIN SIMM. (A) A 30-PIN SIMM ORGANIZED AS 4M × 9 AND (B) A 72-PIN SIMM ORGANIZED AS 4M × 36.



10-1 MEMORY DEVICES

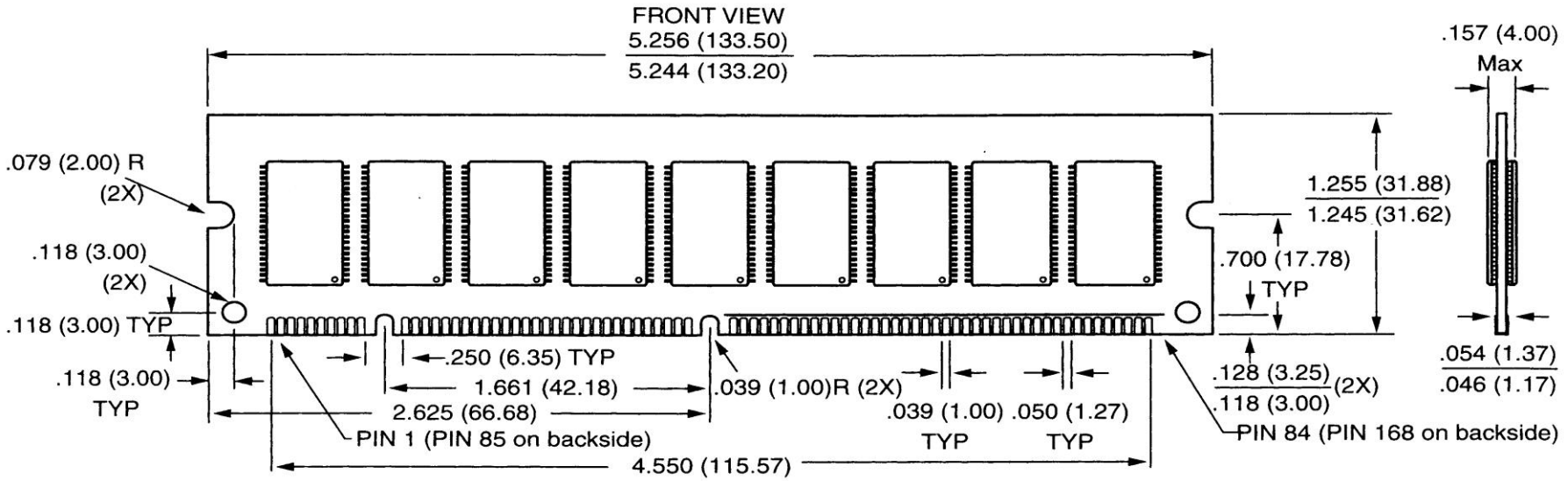
- Pentium–Pentium 4 microprocessors have a **64-bit wide data bus,** which precludes use of the **8-bit-wide SIMMs described here.**
  - 72-pin SIMMs are cumbersome as they must be paired to obtain a 64-bit-wide data connection

- 64-bit-wide DIMMs (Dual In-line Memory Modules) have become the standard.

- The memory on these modules is organized as 64 bits wide.

- Common sizes available are from 16M bytes (2M × 64) to 1G bytes (128M × 64).

FIGURE 10–12 THE PIN-OUT OF A 168-PIN DIMM.



- The DIMM module is available in DRAM, EDO, SDRAM, and DDR (double-data rate) forms, with or without an EPROM.

- The EPROM provides information to the system on the size and the speed of the memory device for plug-and-play applications.

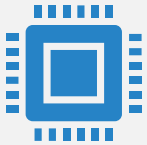
10-1 MEMORY DEVICES

- Another type is the RIMM memory module from RAMBUS Corporation,
  - this memory type has faded from the market

- The latest DRAM is the DDR (double-data rate) memory device and DDR2.
  - DDR transfers data at each edge of the clock, making it operate at twice the speed of SDRAM

- Many wait states are still required to operate this type of memory, but it can be much faster than normal SDRAM memory.

CH10: MEMORY INTERFACE



Memory Devices

Addressing Decoding

10-2 ADDRESS DECODING

- In order to attach a memory device to the microprocessor, **it is necessary to decode the address sent from the microprocessor.**

- **Decoding makes the memory function at a unique section or partition of the memory map.**

- **Without an address decoder, only one memory device can be connected to a microprocessor, which would make it virtually useless.**

10-2 ADDRESS DECODING

WHY DECODE MEMORY?

- The 8088 has **20 address connections** and the 2716 EPROM has 11 connections.

- The 8088 sends out a 20-bit memory address whenever it reads or writes data.
  - because the 2716 has only 11 address pins, there is a mismatch that must be corrected

- **The decoder corrects the mismatch by decoding address pins that do not connect to the memory component.**

10-2 ADDRESS DECODING

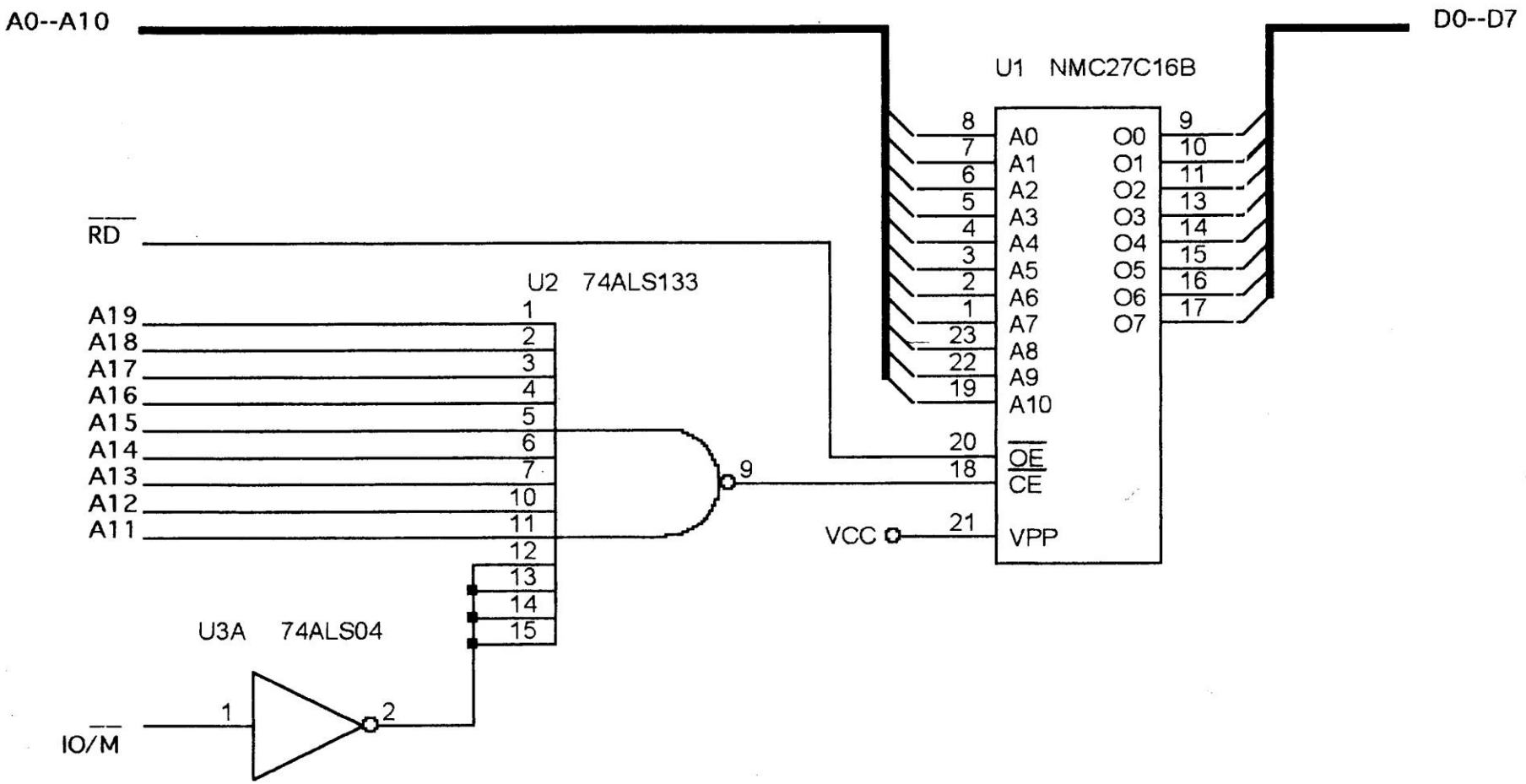
SIMPLE NAND GATE DECODER

- When the 2K × 8 EPROM is used, address connections A10–A0 of 8088 are connected to address inputs A10–A0 of the EPROM.
  - **the remaining nine address pins (A19–A11) are connected to a NAND gate decoder**

- The **decoder selects the EPROM from one of the 2K-byte sections of the 1M-byte memory system** in the 8088 microprocessor.

- In this circuit a NAND gate decodes the memory address, as seen in Figure 10-13.

FIGURE 10–13 A SIMPLE NAND GATE DECODER THAT SELECTS A 2716 EPROM FOR MEMORY LOCATION FF800H–FFFFFH.



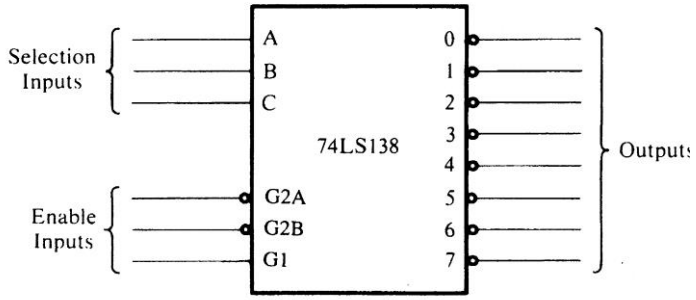
10-2 ADDRESS DECODING

- If the 20-bit binary address, decoded by the NAND gate, is written so that the **leftmost nine bits are 1s and the rightmost 11 bits are don't cares (X)**, the actual address range of the EPROM can be determined.
  - a don't care is a logic 1 or a logic 0, whichever is appropriate

- Because of the **excessive cost of the NAND gate decoder and inverters** often required, this option requires an alternate be found.

10-2 ADDRESS DECODING

The 3-to-8 Line Decoder (74LS138)



Inputs						Outputs							
Enable			Select										
$\overline{G2A}$	$\overline{G2B}$	G1	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

- a common integrated circuit decoder found in many systems is the 74LS138 3-to-8 line decoder.

FIGURE 10–14 THE 74LS138 3-TO-8 LINE DECODER AND FUNCTION TABLE.

10-2 ADDRESS DECODING

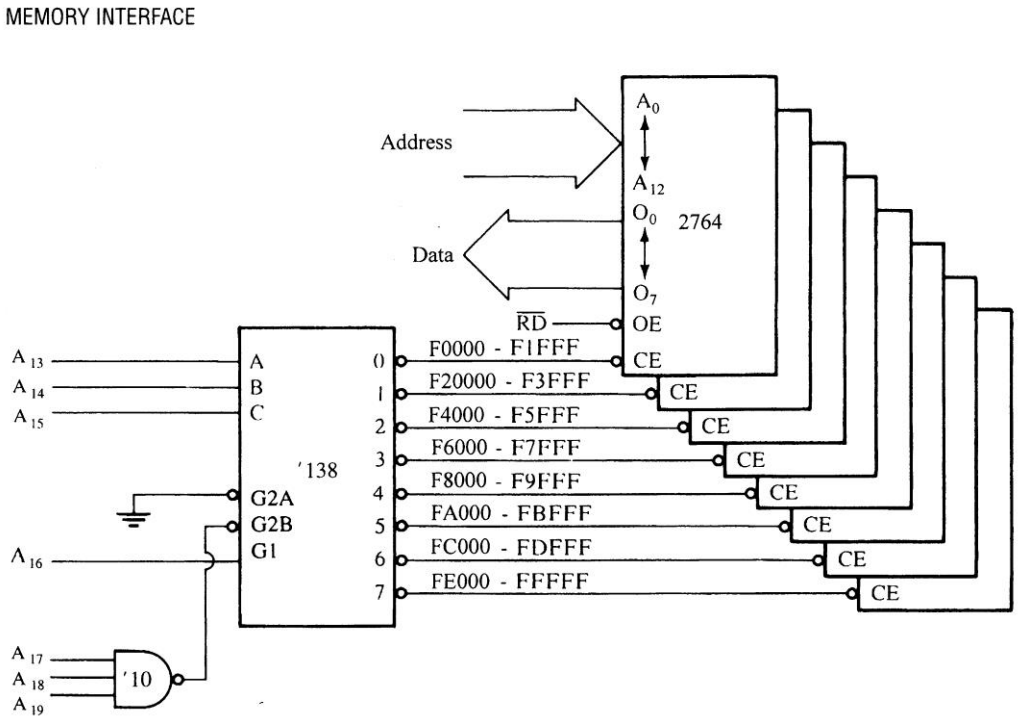
SAMPLE DECODER CIRCUIT

- The outputs of the decoder in Figure 10–15, are connected to eight different 2764 EPROM memory devices.

- The decoder selects eight 8K-byte blocks of memory for a total capacity of 64K bytes.

- This figure also illustrates the address range of each memory device and the common connections to the memory devices.

FIGURE 10–15 A CIRCUIT THAT USES EIGHT 2764 EPROMS FOR A 64K × 8 SECTION OF MEMORY IN AN 8088 MICROPROCESSOR-BASED SYSTEM. THE ADDRESSES SELECTED IN THIS CIRCUIT ARE F0000H–FFFFFH.



- all address connections from the 8088 are connected to this circuit.
- the decoder's outputs are connected to the $\overline{CE}$ inputs of the EPROMs,
- the RD signal from the 8088 is connected to the $\overline{OE}$ inputs of the EPROMs

10-2 ADDRESS DECODING

- In this circuit, a three-input NAND gate is connected to address bits A19–A17.
- When all three address inputs are high, the output of this NAND gate goes low and enables input $\overline{G2B}$ of the 74LS138.
- Input G1 is connected directly to A16.
- **In order to enable this decoder, the first four address connections (A19–A16) must all be high.**

10-2 ADDRESS DECODING

- Address inputs C, B, and A connect to microprocessor address pins A15–A13.

- These three address inputs **determine which output pin goes low and which EPROM is selected whenever 8088 outputs a memory address within this range to the memory system.**

10-2 ADDRESS DECODING

PLD PROGRAMMABLE DECODERS

- Three SPLD (simple PLD) devices function in the same manner but have different names:
  - PLA (programmable logic array)
  - PAL (programmable array logic)
  - GAL (gated array logic)

- In existence since the mid-70s, they have appeared in memory system and digital designs since the early 1990s.

10-2 ADDRESS DECODING

- PAL and PLA are fuse-programmed, and some PLD devices are erasable devices.
  - all are arrays of programmable logic elements

- Other PLDs available:
  - CPLDs (complex programmable logic devices)
  - FPGAs (field programmable gate arrays)
  - FPICs (field programmable interconnect)

- These PLDs are more complex than the SPLDs used more commonly in designing a complete system.

10-2 ADDRESS DECODING

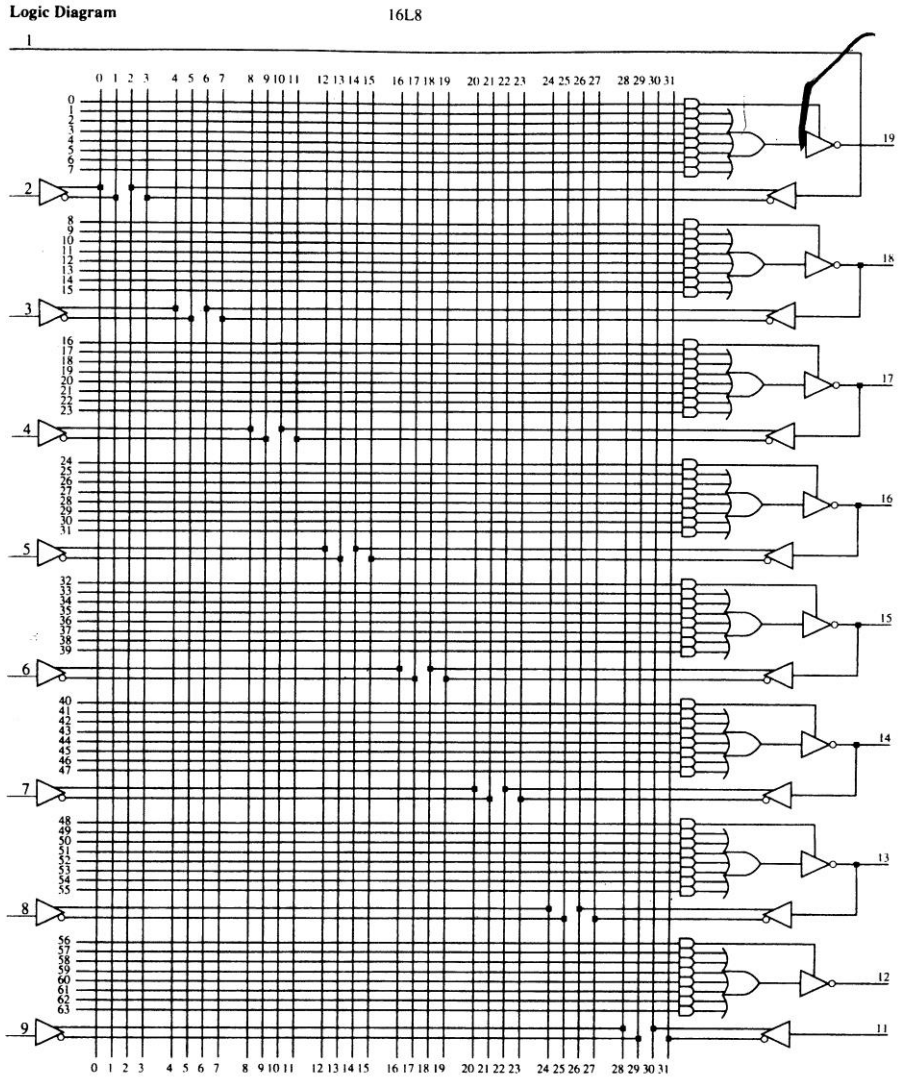
- **If the concentration is on decoding addresses, the SPLD is used.**
- **If the concentration is on a complete system, then the CPLD, FPLG, or FPIC is used to implement the design.**
- These devices are also referred to as an **ASIC (application-specific integrated circuit).**

10-2 ADDRESS DECODING

COMBINATORIAL PROGRAMMABLE LOGIC ARRAYS

- Fig 10–18 shows the internal structure of a PAL16L8 constructed with AND/OR gate logic.
- It has 10 fixed inputs, two fixed outputs, and six pins programmable as inputs or outputs.
- Programming is accomplished by blowing fuses to connect inputs to the OR gate array.
- It is ideal as a decoder because of its structure, also because outputs are active low.

FIGURE 10–18 THE PAL16L8. (COPYRIGHT ADVANCED MICRO DEVICES, INC., 1988. REPRINTED WITH PERMISSION OF COPYRIGHT OWNER. ALL RIGHTS RESERVED.)



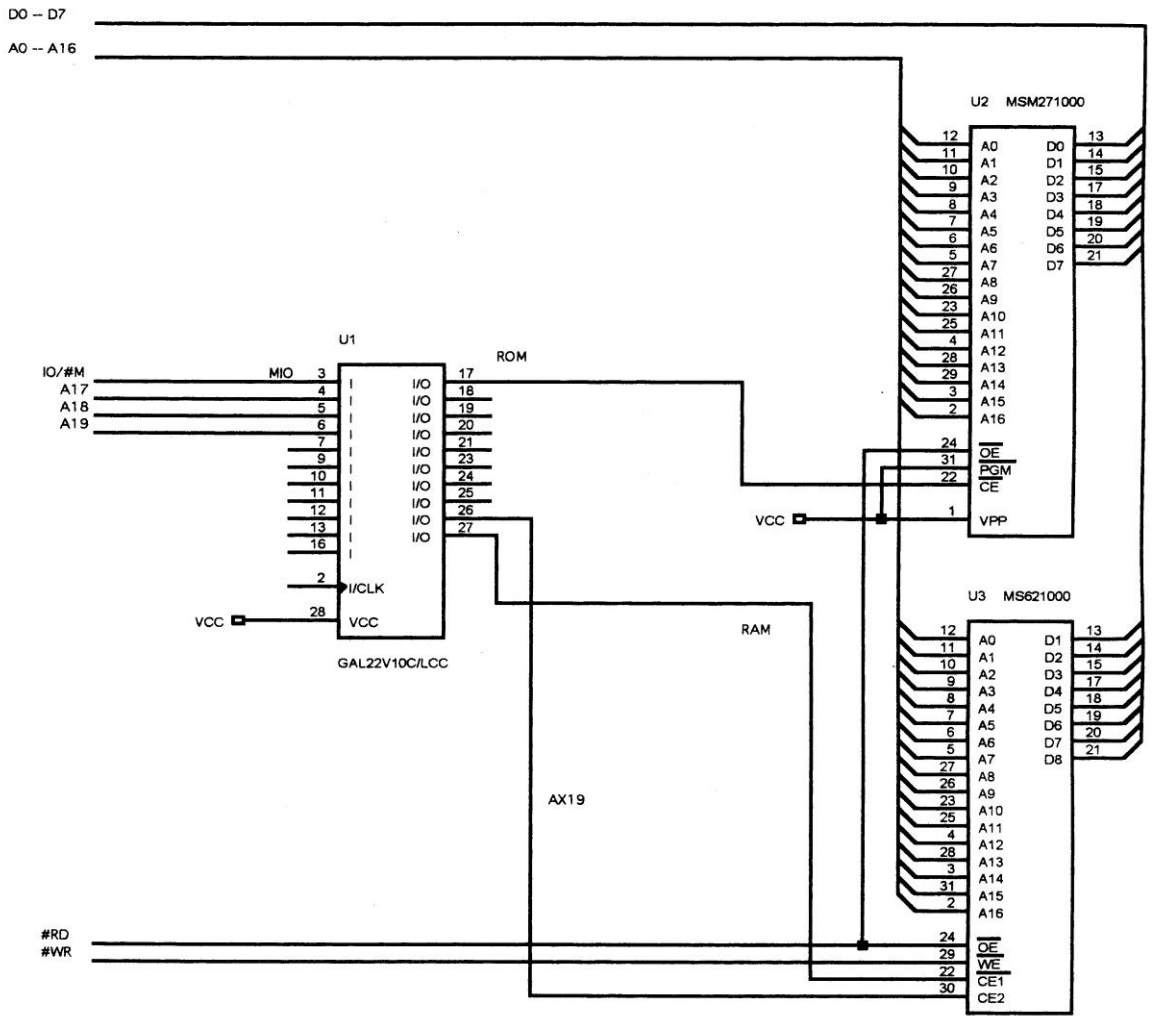
10-2 ADDRESS DECODING

- A PAL is programmed with software such as PALASM, the PAL assembler program.

- PLD design is accomplished using HDL (hardware description language) or VHDL (verilog HDL).
  - VHDL and its syntax are currently the industry standard for programming PLD devices

- Various editors attempt to ease the task of defining the pins.
  - the authors believe it is easier to use NotePad

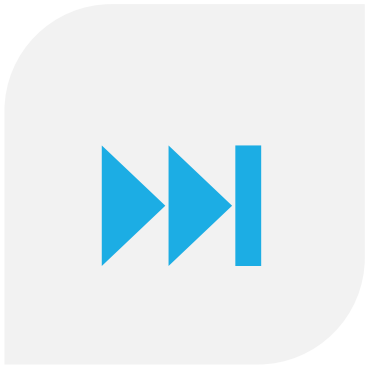
FIGURE 10–19 A RAM AND ROM INTERFACE USING A PROGRAMMABLE LOGIC DEVICE.



- the equation causes the ROM pin to become a logic zero only when the A_{19}, A_{18}, A_{17}, and M/IO are all logic zeros (00000H–1FFFFH)
- the RAM equation causes the RAM pin to become a logic zero when A_{18} and A_{17} are all ones at the same time that M/IO is logic zero
- RAM is selected for 60000H–7FFFFH

SUMMARY

- ✓Memory Interface (Part1)
  - Memory Devices
  - Addressing Decoding



NEXT

- ✓Memory Interface (Part2)
  - Memory Interface


THE
END