Release 14.7 - xst P.20131013 (nt)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.11 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.11 secs

--> Reading design: MipsPipelineTestBench.prj

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7) Low Level Synthesis

8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

===

* Synthesis Options Summary *

===

---- Source Parameters

Input File Name : "MipsPipelineTestBench.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "MipsPipelineTestBench"

Output Format : NGC

Target Device : xc3s400-4-pq208

---- Source Options

Top Module Name : MipsPipelineTestBench

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Keep Hierarchy : No

Netlist Hierarchy : As_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

```
=========================================================================



=========================================================================
*                    HDL Compilation                        *
=========================================================================
WARNING:HDLCompilers:176 - Include directory \githubFullCodeForTest\ does not exist
Compiling verilog file "G:/githubFullCodeForTest/SignExtend.v" in library work
Compiling verilog file "G:/githubFullCodeForTest/ShiftLeft2.v" in library work
Module <SignExtend> compiled
Compiling verilog file "G:/githubFullCodeForTest/RegisterFile.v" in library work
Module <ShiftLeft2> compiled
Compiling verilog file "G:/githubFullCodeForTest/PC.v" in library work
Module <RegisterFile> compiled
Compiling verilog file "G:/githubFullCodeForTest/Mux3x1_32Bits.v" in library work
Module <PC> compiled
Compiling verilog file "G:/githubFullCodeForTest/Mux2x1_5Bits.v" in library work
Module <Mux3x1_32Bits> compiled
Compiling verilog file "G:/githubFullCodeForTest/Mux2x1_32Bits.v" in library work
Module <Mux2x1_5Bits> compiled
Compiling verilog file "G:/githubFullCodeForTest/Mux2x1_10Bits.v" in library work
Module <Mux2x1_32Bits> compiled
Compiling verilog file "G:/githubFullCodeForTest/Mem_WbReg.v" in library work
Module <Mux2x1_10Bits> compiled
Compiling verilog file "G:/githubFullCodeForTest/InstructionMemory.v" in library work
```

Module <Mem_WbReg> compiled

Compiling verilog file "G:/githubFullCodeForTest/IF_IDReg.v" in library work

Module <InstructionMemory> compiled

Compiling verilog file "G:/githubFullCodeForTest/ID_EX_reg.v" in library work

Module <IF_ID_reg> compiled

Compiling verilog file "G:/githubFullCodeForTest/HazardDetectionUnit.v" in library work

Module <ID_EX_reg> compiled

Compiling verilog file "G:/githubFullCodeForTest/ForwardingUnit.v" in library work

Module <HazardDetectionUnit> compiled

Compiling verilog file "G:/githubFullCodeForTest/EX_MemReg.v" in library work

Module <ForwardingUnit> compiled

Compiling verilog file "G:/githubFullCodeForTest/DataMemory.v" in library work

Module <EX_MemReg> compiled

Compiling verilog file "G:/githubFullCodeForTest/ControlUnit.v" in library work

Module <DataMemory> compiled

Compiling verilog file "G:/githubFullCodeForTest/Comparator.v" in library work

Module <ControlUnit> compiled

Compiling verilog file "G:/githubFullCodeForTest/ALUControl.v" in library work

Module <Comparator> compiled

Compiling verilog file "G:/githubFullCodeForTest/ALU32Bit.v" in library work

Module <ALUControl> compiled

Compiling verilog file "G:/githubFullCodeForTest/MipsPipelineTestBench.v" in library work

Module <ALU32Bit> compiled

Module <MipsPipelineTestBench> compiled

No errors in compilation

Analysis of file <"MipsPipelineTestBench.prj"> succeeded.

==========

* Design Hierarchy Analysis *

==========

Analyzing hierarchy for module <MipsPipelineTestBench> in library <work>.

Analyzing hierarchy for module <PC> in library <work>.

Analyzing hierarchy for module <InstructionMemory> in library <work>.

Analyzing hierarchy for module <Adder> in library <work>.

Analyzing hierarchy for module <Mux2x1_32Bits> in library <work>.

Analyzing hierarchy for module <IF_ID_reg> in library <work>.

Analyzing hierarchy for module <ControlUnit> in library <work> with parameters.

R_type = "000000"

addi = "001000"

andi = "001100"

beq = "000100"

lw = "100011"

ori = "001101"

slti = "001010"

sw = "101011"

Analyzing hierarchy for module <RegisterFile> in library <work>.

Analyzing hierarchy for module <Mux3x1_32Bits> in library <work>.

Analyzing hierarchy for module <Comparator> in library <work>.

Analyzing hierarchy for module <SignExtend> in library <work>.

Analyzing hierarchy for module <ShiftLeft2> in library <work>.

Analyzing hierarchy for module <HazardDetectionUnit> in library <work> with parameters.

beqOPcode = "000100"

Analyzing hierarchy for module <Mux2x1_10Bits> in library <work>.

Analyzing hierarchy for module <ID_EX_reg> in library <work>.

Analyzing hierarchy for module <ALUControl> in library <work>.

Analyzing hierarchy for module <ALU32Bit> in library <work> with parameters.

ADD = "0000"

AND = "0010"

GREATER = "0111"

LESS = "1000"

NOR = "1001"

OR = "0011"

SHFT_L = "0100"

SHFT_R_A = "0110"

SHFT_R_L = "0101"

SUB = "0001"

Analyzing hierarchy for module <Mux2x1_5Bits> in library <work>.

Analyzing hierarchy for module <EX_MemReg> in library <work>.

Analyzing hierarchy for module <ForwardingUnit> in library <work>.

Analyzing hierarchy for module <DataMemory> in library <work>.

Analyzing hierarchy for module <Mem_WbReg> in library <work>.

===

* HDL Analysis *

===

Analyzing top module <MipsPipelineTestBench>.

WARNING:Xst:916 - "G:/githubFullCodeForTest/MipsPipelineTestBench.v" line 85: Delay is ignored for synthesis.

Module <MipsPipelineTestBench> is correct for synthesis.

Analyzing module <PC> in library <work>.

Module <PC> is correct for synthesis.

Analyzing module <InstructionMemory> in library <work>.

INFO:Xst:2546 - "G:/githubFullCodeForTest/InstructionMemory.v" line 10: reading initialization file "code.txt".

WARNING:Xst:2319 - "G:/githubFullCodeForTest/InstructionMemory.v" line 10: Signal Imemory in initial block is partially initialized. The initialization will be ignored.

INFO:Xst:1607 - Contents of array <Imemory> may be accessed with an index that does not cover the full array size.

WARNING:Xst:905 - "G:/githubFullCodeForTest/InstructionMemory.v" line 16: One or more signals are missing in the sensitivity list of always block. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:

  <Imemory>

Module <InstructionMemory> is correct for synthesis.

Analyzing module <Adder> in library <work>.

Module <Adder> is correct for synthesis.

Analyzing module <Mux2x1_32Bits> in library <work>.

Module <Mux2x1_32Bits> is correct for synthesis.

Analyzing module <IF_ID_reg> in library <work>.

Module <IF_ID_reg> is correct for synthesis.

Analyzing module <ControlUnit> in library <work>.

R_type = 6'b000000

addi = 6'b001000

andi = 6'b001100

beq = 6'b000100

lw = 6'b100011

ori = 6'b001101

slti = 6'b001010

sw = 6'b101011

Module <ControlUnit> is correct for synthesis.

Analyzing module <RegisterFile> in library <work>.

WARNING:Xst:2319 - "G:/githubFullCodeForTest/RegisterFile.v" line 16: Signal memory in initial block is partially initialized. The initialization will be ignored.

WARNING:Xst:905 - "G:/githubFullCodeForTest/RegisterFile.v" line 21: One or more signals are missing in the sensitivity list of always block. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:

<memory>

Module <RegisterFile> is correct for synthesis.

Analyzing module <Mux3x1_32Bits> in library <work>.

Module <Mux3x1_32Bits> is correct for synthesis.

Analyzing module <Comparator> in library <work>.

Module <Comparator> is correct for synthesis.

Analyzing module <SignExtend> in library <work>.

Module <SignExtend> is correct for synthesis.

Analyzing module <ShiftLeft2> in library <work>.

Module <ShiftLeft2> is correct for synthesis.

Analyzing module <HazardDetectionUnit> in library <work>.

beqOPcode = 6'b000100

WARNING:Xst:905 - "G:/githubFullCodeForTest/HazardDetectionUnit.v" line 17: One or more signals are missing in the sensitivity list of always block. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:

<holdPC>, <holdIF_ID>

Module <HazardDetectionUnit> is correct for synthesis.

Analyzing module <Mux2x1_10Bits> in library <work>.

Module <Mux2x1_10Bits> is correct for synthesis.

Analyzing module <ID_EX_reg> in library <work>.

Module <ID_EX_reg> is correct for synthesis.

Analyzing module <ALUControl> in library <work>.

Module <ALUControl> is correct for synthesis.

Analyzing module <ALU32Bit> in library <work>.

ADD = 4'b0000

AND = 4'b0010

GREATER = 4'b0111

LESS = 4'b1000

NOR = 4'b1001

OR = 4'b0011

SHFT_L = 4'b0100

SHFT_R_A = 4'b0110

SHFT_R_L = 4'b0101

SUB = 4'b0001

WARNING:Xst:905 - "G:/githubFullCodeForTest/ALU32Bit.v" line 29: One or more signals are missing in the sensitivity list of always block. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:

<neg_data2>, <shiftAmount>

Module <ALU32Bit> is correct for synthesis.

Analyzing module <Mux2x1_5Bits> in library <work>.

Module <Mux2x1_5Bits> is correct for synthesis.

Analyzing module <EX_MemReg> in library <work>.

Module <EX_MemReg> is correct for synthesis.

Analyzing module <ForwardingUnit> in library <work>.

Module <ForwardingUnit> is correct for synthesis.

Analyzing module <DataMemory> in library <work>.

INFO:Xst:1607 - Contents of array <memory> may be accessed with an index that does not cover the full array size.

INFO:Xst:1607 - Contents of array <memory> may be accessed with an index that does not cover the full array size.

WARNING:Xst:905 - "G:/githubFullCodeForTest/DataMemory.v" line 14: One or more signals are missing in the sensitivity list of always block. To enable synthesis of FPGA/CPLD hardware, XST will assume that all necessary signals are present in the sensitivity list. Please note that the result of the synthesis may differ from the initial design specification. The missing signals are:

  <memory>

Module <DataMemory> is correct for synthesis.

Analyzing module <Mem_WbReg> in library <work>.

Module <Mem_WbReg> is correct for synthesis.

===

*   HDL Synthesis   *

===

Performing bidirectional port resolution...

Synthesizing Unit <PC>.

  Related source file is "G:/githubFullCodeForTest/PC.v".

WARNING:Xst:647 - Input <Reset> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

  Found 32-bit register for signal <outPC>.

  Summary:

        inferred 32 D-type flip-flop(s).

Unit <PC> synthesized.

Synthesizing Unit <InstructionMemory>.

Related source file is "G:/githubFullCodeForTest/InstructionMemory.v".

WARNING:Xst:647 - Input <clk> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:647 - Input <pc<1:0>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:653 - Signal <Imemory> is used but never assigned. This sourceless signal will be automatically connected to value 00000000000000000000000000000000.

Unit <InstructionMemory> synthesized.

Synthesizing Unit <Adder>.

Related source file is "G:/githubFullCodeForTest/Adder.v".

Found 32-bit adder for signal <out>.

Summary:

inferred 1 Adder/Subtractor(s).

Unit <Adder> synthesized.

Synthesizing Unit <Mux2x1_32Bits>.

Related source file is "G:/githubFullCodeForTest/Mux2x1_32Bits.v".

Unit <Mux2x1_32Bits> synthesized.

Synthesizing Unit <IF_ID_reg>.

Related source file is "G:/githubFullCodeForTest/IF_IDReg.v".

Found 32-bit register for signal <instrOut>.

Found 32-bit register for signal <PCplus4Out>.

Summary:

inferred 64 D-type flip-flop(s).

Unit <IF_ID_reg> synthesized.

Synthesizing Unit <ControlUnit>.

Related source file is "G:/githubFullCodeForTest/ControlUnit.v".

WARNING:Xst:647 - Input <reset> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:737 - Found 1-bit latch for signal <RegDst>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.

WARNING:Xst:737 - Found 1-bit latch for signal <branch>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.

WARNING:Xst:737 - Found 1-bit latch for signal <Memread>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a

result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.

WARNING:Xst:737 - Found 1-bit latch for signal <MemWrite>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.

WARNING:Xst:737 - Found 1-bit latch for signal <AluSrc>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.

WARNING:Xst:737 - Found 1-bit latch for signal <RegWrite>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.

WARNING:Xst:737 - Found 4-bit latch for signal <ALUop>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.

Unit <ControlUnit> synthesized.

Synthesizing Unit <RegisterFile>.

Related source file is "G:/githubFullCodeForTest/RegisterFile.v".

WARNING:Xst:647 - Input <reset> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Found 32x32-bit dual-port RAM <Mram_memory> for signal <memory>.

Found 32x32-bit dual-port RAM <Mram_memory_ren> for signal <memory>.

Summary:

inferred 2 RAM(s).

Unit <RegisterFile> synthesized.

Synthesizing Unit <Mux3x1_32Bits>.

Related source file is "G:/githubFullCodeForTest/Mux3x1_32Bits.v".

Found 32-bit 3-to-1 multiplexer for signal <out>.

Summary:

inferred 32 Multiplexer(s).

Unit <Mux3x1_32Bits> synthesized.

Synthesizing Unit <Comparator>.

Related source file is "G:/githubFullCodeForTest/Comparator.v".

Found 32-bit comparator equal for signal <equalFlag$cmp_eq0000> created at line 7.

Summary:

inferred 1 Comparator(s).

Unit <Comparator> synthesized.

Synthesizing Unit <SignExtend>.

Related source file is "G:/githubFullCodeForTest/SignExtend.v".

Unit <SignExtend> synthesized.

Synthesizing Unit <ShiftLeft2>.

Related source file is "G:/githubFullCodeForTest/ShiftLeft2.v".

WARNING:Xst:647 - Input <in<31:30>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Unit <ShiftLeft2> synthesized.

Synthesizing Unit <HazardDetectionUnit>.

Related source file is "G:/githubFullCodeForTest/HazardDetectionUnit.v".

WARNING:Xst:647 - Input <EX_MemMemRead> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:647 - Input <IF_ID_Instr<14:0>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Register <holdPC> equivalent to <holdIF_ID> has been removed

Register <muxSelector> equivalent to <holdIF_ID> has been removed

WARNING:Xst:737 - Found 1-bit latch for signal <holdIF_ID>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

Found 5-bit comparator equal for signal <holdIF_ID$cmp_eq0000> created at line 20.

Found 6-bit comparator equal for signal <holdIF_ID$cmp_eq0001> created at line 20.

Summary:

inferred 2 Comparator(s).

Unit <HazardDetectionUnit> synthesized.

Synthesizing Unit <Mux2x1_10Bits>.

Related source file is "G:/githubFullCodeForTest/Mux2x1_10Bits.v".

Unit <Mux2x1_10Bits> synthesized.

Synthesizing Unit <ID_EX_reg>.

Related source file is "G:/githubFullCodeForTest/ID_EX_reg.v".

Found 1-bit register for signal <MemWriteOut>.

Found 1-bit register for signal <ALUSrcOut>.

Found 5-bit register for signal <rsOut>.

Found 4-bit register for signal <ALUOpOut>.

Found 1-bit register for signal <MemtoRegOut>.

Found 32-bit register for signal <ReadData1_out>.

Found 5-bit register for signal <rdOut>.

Found 32-bit register for signal <SignExtendResult_out>.

Found 32-bit register for signal <ReadData2_out>.

Found 1-bit register for signal <RegWriteOut>.

Found 1-bit register for signal <MemReadOut>.

Found 5-bit register for signal <rtOut>.

Found 1-bit register for signal <RegDstOut>.

Found 32-bit register for signal <PCplus4out>.

Summary:

inferred 153 D-type flip-flop(s).

Unit <ID_EX_reg> synthesized.

Synthesizing Unit <ALUControl>.

Related source file is "G:/githubFullCodeForTest/ALUControl.v".

WARNING:Xst:647 - Input <clk> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Found 4-bit 6-to-1 multiplexer for signal <ALUControl>.

Summary:

inferred 4 Multiplexer(s).

Unit <ALUControl> synthesized.

Synthesizing Unit <ALU32Bit>.

Related source file is "G:/githubFullCodeForTest/ALU32Bit.v".

WARNING:Xst:647 - Input <reset> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:737 - Found 32-bit latch for signal <ALUResult>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.

WARNING:Xst:737 - Found 1-bit latch for signal <overFlow>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate enable inputs of this latch share common terms. This situation will potentially lead to setup/hold violations and, as a result, to simulation problems. This situation may come from an incomplete case statement (all selector values are not covered). You should carefully review if it was in your intentions to describe such a latch.

Found 32-bit adder for signal <ALUResult$addsub0000>.

Found 32-bit comparator greater for signal <ALUResult$cmp_gt0000> created at line 73.

Found 32-bit comparator less for signal <ALUResult$cmp_lt0000> created at line 81.

Found 32-bit 10-to-1 multiplexer for signal <ALUResult$mux0001>.

Found 32-bit shifter logical left for signal <ALUResult$shift0000> created at line 63.

Found 32-bit shifter logical right for signal <ALUResult$shift0001> created at line 66.

Found 32-bit shifter arithmetic right for signal <ALUResult$shift0002> created at line 69.

Found 32-bit adder for signal <neg_data2>.

Found 1-bit xor2 for signal <overFlow$xor0000> created at line 41.

Found 1-bit xor2 for signal <overFlow$xor0001> created at line 41.

Found 1-bit xor2 for signal <overFlow$xor0002> created at line 50.

Found 32-bit comparator equal for signal <zero$cmp_eq0000> created at line 31.

Summary:

inferred 2 Adder/Subtractor(s).

inferred 3 Comparator(s).

inferred 32 Multiplexer(s).

inferred 3 Combinational logic shifter(s).

Unit <ALU32Bit> synthesized.

Synthesizing Unit <Mux2x1_5Bits>.

Related source file is "G:/githubFullCodeForTest/Mux2x1_5Bits.v".

Unit <Mux2x1_5Bits> synthesized.

Synthesizing Unit <EX_MemReg>.

Related source file is "G:/githubFullCodeForTest/EX_MemReg.v".

Found 1-bit register for signal <MemWriteOut>.

Found 1-bit register for signal <MemtoRegOut>.

Found 5-bit register for signal <writeRegOut>.

Found 32-bit register for signal <writedataOut>.

Found 1-bit register for signal <RegWriteOut>.

Found 1-bit register for signal <MemReadOut>.

Found 32-bit register for signal <ALUresultOut>.

Summary:

inferred 73 D-type flip-flop(s).

Unit <EX_MemReg> synthesized.

Synthesizing Unit <ForwardingUnit>.

Related source file is "G:/githubFullCodeForTest/ForwardingUnit.v".

Found 5-bit comparator equal for signal <lowerMux_sel$cmp_eq0000> created at line 25.

Found 5-bit comparator equal for signal <lowerMux_sel$cmp_eq0001> created at line 53.

Found 5-bit comparator equal for signal <upperMux_sel$cmp_eq0000> created at line 13.

Found 5-bit comparator equal for signal <upperMux_sel$cmp_eq0001> created at line 40.

Found 5-bit comparator not equal for signal <upperMux_sel$cmp_ne0002> created at line 40.

Summary:

inferred 5 Comparator(s).

Unit <ForwardingUnit> synthesized.

Synthesizing Unit <DataMemory>.

Related source file is "G:/githubFullCodeForTest/DataMemory.v".

WARNING:Xst:647 - Input <address<31:5>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Found 32x32-bit single-port RAM <Mram_memory> for signal <memory>.

WARNING:Xst:737 - Found 32-bit latch for signal <readData>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

Summary:

inferred 1 RAM(s).

Unit <DataMemory> synthesized.

Synthesizing Unit <Mem_WbReg>.

Related source file is "G:/githubFullCodeForTest/Mem_WbReg.v".

Found 1-bit register for signal <MemtoRegOut>.

Found 32-bit register for signal <readDataOut>.

Found 5-bit register for signal <writeRegOut>.

Found 1-bit register for signal <RegWriteOut>.

Found 32-bit register for signal <ALUresultOut>.

Summary:

inferred 71 D-type flip-flop(s).

Unit <Mem_WbReg> synthesized.

Synthesizing Unit <MipsPipelineTestBench>.

Related source file is "G:/githubFullCodeForTest/MipsPipelineTestBench.v".

WARNING:Xst:646 - Signal <zero> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:653 - Signal <reset> is used but never assigned. This sourceless signal will be automatically connected to value 0.

WARNING:Xst:646 - Signal <overFlow> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <controlSignalsID> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <PCPlus4EX> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Unit <MipsPipelineTestBench> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations in this design can share the same physical resources for reduced device utilization. For improved clock frequency you may try to disable resource sharing.

WARNING:Xst:524 - All outputs of the instance <ID_EXRegMux> of the block <Mux2x1_10Bits> are unconnected in block <MipsPipelineTestBench>.

This instance will be removed from the design along with all underlying logic

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HDL Synthesis Report

Macro Statistics

RAMs : 3

32x32-bit dual-port RAM : 2

32x32-bit single-port RAM : 1

Adders/Subtractors : 4

32-bit adder : 4

Registers : 29

1-bit register : 12

32-bit register : 11

4-bit register : 1

5-bit register : 5

Latches : 11

1-bit latch : 8

32-bit latch : 2

4-bit latch : 1

Comparators : 11

32-bit comparator equal : 2

32-bit comparator greater : 1

32-bit comparator less : 1

5-bit comparator equal : 5

5-bit comparator not equal : 1

6-bit comparator equal : 1

Multiplexers : 6

32-bit 10-to-1 multiplexer : 1

32-bit 3-to-1 multiplexer : 4

4-bit 6-to-1 multiplexer : 1

Logic shifters : 3

32-bit shifter arithmetic right : 1

32-bit shifter logical left : 1

32-bit shifter logical right : 1

Xors : 3

1-bit xor2 : 3

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* Advanced HDL Synthesis *

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WARNING:Xst:1290 - Hierarchical block <PCRegister> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <instructionMemory> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <PCAdder> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <nextPCMux> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <IF_ID> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <controlUnit> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <regiterFile> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <comparatorMux1> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <comparatorMux2> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <comparator> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <signExtend> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <shiftLeft2> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <branchAdder> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <hazardUnit> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <ID_EX> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <ALUData1Mux> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <ALUData2Mux_1> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <ALUData2Mux_2> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <AluControl> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <ALU> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <regDstMux> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <EX_MEM> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <forwardingUnit> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <dataMemory> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <MEM_WB> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

WARNING:Xst:1290 - Hierarchical block <writeBackMux> is unconnected in block <MipsPipelineTestBench>.

It will be removed from the design.

Synthesizing (advanced) Unit <MipsPipelineTestBench>.

The following registers are absorbed into accumulator <PCRegister/outPC>: 1 register on signal <PCRegister/outPC>.

INFO:Xst:3226 - The RAM <regiterFile/Mram_memory_ren> will be implemented as a BLOCK RAM, absorbing the following register(s): <IF_ID/instrOut>

ram_type	Block		
Port A			
aspect ratio	32-word x 32-bit		
mode	write-first		
clkA	connected to signal <clk>	fall	
weA	connected to signal <RegWriteWB>	high	
addrA	connected to signal <writeRegWB>		
diA	connected to signal <regWriteDataMEM>		
optimization	speed		
Port B			
aspect ratio	32-word x 32-bit		
mode	write-first		
clkB	connected to signal <clk>	rise	
enB	connected to signal <IF_ID/PCplus4Out_not0001>	high	
addrB	connected to internal node		
doB	connected to signal <registerData2ID>		
optimization	speed		

INFO:Xst:3226 - The RAM <regiterFile/Mram_memory> will be implemented as a BLOCK RAM, absorbing the following register(s): <IF_ID/instrOut>

| ram_type | Block | |

| Port A | | |

| aspect ratio | 32-word x 32-bit | |

| mode | write-first | |

| clkA | connected to signal <clk> | fall |

| weA | connected to signal <RegWriteWB> | high |

| addrA | connected to signal <writeRegWB> | |

| diA | connected to signal <regWriteDataMEM> | |

| optimization | speed | |

| Port B | | |

| aspect ratio | 32-word x 32-bit | |

| mode | write-first | |

| clkB | connected to signal <clk> | rise |

| enB | connected to signal <IF_ID/PCplus4Out_not0001> | high |

| addrB | connected to internal node | |

| doB | connected to signal <registerData1ID> | |

| optimization | speed | |

Unit <MipsPipelineTestBench> synthesized (advanced).

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Advanced HDL Synthesis Report

Macro Statistics

RAMs : 3

32x32-bit dual-port block RAM : 2

32x32-bit single-port distributed RAM : 1

Adders/Subtractors : 4

32-bit adder : 4

Accumulators : 1

32-bit up loadable accumulator : 1

Registers : 361

Flip-Flops : 361

Latches : 11

1-bit latch : 8

32-bit latch : 2

4-bit latch : 1

Comparators : 11

32-bit comparator equal : 2

32-bit comparator greater : 1

32-bit comparator less : 1

5-bit comparator equal : 5

5-bit comparator not equal : 1

6-bit comparator equal : 1

Multiplexers : 6

32-bit 10-to-1 multiplexer : 1

32-bit 3-to-1 multiplexer : 4

4-bit 6-to-1 multiplexer : 1

Logic shifters : 3

32-bit shifter arithmetic right : 1

32-bit shifter logical left : 1

32-bit shifter logical right : 1

Xors : 3

1-bit xor2 : 3

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* Low Level Synthesis *

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INFO:Xst:2261 - The FF/Latch <IF_ID/instrOut_0> in Unit <MipsPipelineTestBench> is equivalent to the following 31 FFs/Latches, which will be removed : <IF_ID/instrOut_1> <IF_ID/instrOut_2> <IF_ID/instrOut_3> <IF_ID/instrOut_4> <IF_ID/instrOut_5> <IF_ID/instrOut_6> <IF_ID/instrOut_7> <IF_ID/instrOut_8> <IF_ID/instrOut_9> <IF_ID/instrOut_10> <IF_ID/instrOut_11> <IF_ID/instrOut_12> <IF_ID/instrOut_13> <IF_ID/instrOut_14> <IF_ID/instrOut_15> <IF_ID/instrOut_16> <IF_ID/instrOut_17> <IF_ID/instrOut_18> <IF_ID/instrOut_19> <IF_ID/instrOut_20> <IF_ID/instrOut_21> <IF_ID/instrOut_22> <IF_ID/instrOut_23> <IF_ID/instrOut_24> <IF_ID/instrOut_25> <IF_ID/instrOut_26> <IF_ID/instrOut_27> <IF_ID/instrOut_28> <IF_ID/instrOut_29> <IF_ID/instrOut_30> <IF_ID/instrOut_31>

INFO:Xst:2261 - The FF/Latch <SignExtendResult_out_15> in Unit <ID_EX_reg> is equivalent to the following 17 FFs/Latches, which will be removed : <SignExtendResult_out_16> <SignExtendResult_out_17> <SignExtendResult_out_18> <SignExtendResult_out_19> <SignExtendResult_out_20> <SignExtendResult_out_21> <SignExtendResult_out_22> <SignExtendResult_out_23> <SignExtendResult_out_24> <SignExtendResult_out_25> <SignExtendResult_out_26> <SignExtendResult_out_27> <SignExtendResult_out_28> <SignExtendResult_out_29> <SignExtendResult_out_30> <SignExtendResult_out_31> <rdOut_4>

WARNING:Xst:1293 - FF/Latch <ALUop_3> has a constant value of 0 in block <ControlUnit>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1710 - FF/Latch <IF_ID/instrOut_0> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

Optimizing unit <MipsPipelineTestBench> ...

Optimizing unit <HazardDetectionUnit> ...

Optimizing unit <ID_EX_reg> ...

Optimizing unit <ControlUnit> ...

Optimizing unit <ALU32Bit> ...

WARNING:Xst:1426 - The value init of the FF/Latch controlUnit/RegWrite hinder the constant cleaning in the block MipsPipelineTestBench.

You should achieve better results by setting this init to 1.

WARNING:Xst:1426 - The value init of the FF/Latch controlUnit/RegDst hinder the constant cleaning in the block MipsPipelineTestBench.

You should achieve better results by setting this init to 1.

WARNING:Xst:1426 - The value init of the FF/Latch controlUnit/ALUop_1 hinder the constant cleaning in the block MipsPipelineTestBench.

You should achieve better results by setting this init to 1.

WARNING:Xst:1293 - FF/Latch <hazardUnit/holdIF_ID> has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1293 - FF/Latch <controlUnit/ALUop_2> has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1293 - FF/Latch <controlUnit/ALUop_0> has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1293 - FF/Latch <controlUnit/AluSrc> has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1293 - FF/Latch <controlUnit/MemWrite> has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1293 - FF/Latch <controlUnit/branch> has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1293 - FF/Latch <controlUnit/Memread> has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rdOut_3> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rsOut_0> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rsOut_1> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rsOut_2> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rsOut_3> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rsOut_4> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rtOut_0> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rtOut_1> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rtOut_2> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rtOut_3> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rtOut_4> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/MemtoRegOut> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/MemWriteOut> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/MemReadOut> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/ALUSrcOut> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/ALUOpOut_0> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/ALUOpOut_2> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_0> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_1> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_2> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_3> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_4> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_5> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_6> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_7> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_8> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_9> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_10> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_11> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_12> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_13> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_14> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/SignExtendResult_out_15> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rdOut_0> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rdOut_1> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/rdOut_2> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <EX_MEM/writeRegOut_3> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <EX_MEM/writeRegOut_4> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <EX_MEM/writeRegOut_0> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <EX_MEM/writeRegOut_1> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <EX_MEM/writeRegOut_2> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <EX_MEM/MemtoRegOut> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <EX_MEM/MemWriteOut> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <EX_MEM/MemReadOut> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/writeRegOut_4> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/writeRegOut_3> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/writeRegOut_2> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/writeRegOut_1> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/writeRegOut_0> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_22> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_23> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_24> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_25> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_26> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_27> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_28> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_29> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_30> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_31> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/MemtoRegOut> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_0> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_1> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_2> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_3> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_4> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_5> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_6> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_7> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_8> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_9> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_10> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_21> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_20> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_19> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_18> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_17> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_16> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_15> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_14> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_13> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_12> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <dataMemory/readData_11> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_0> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_1> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_2> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_3> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_4> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_5> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_6> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_7> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_8> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_29> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_30> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_31> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_28> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_27> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_26> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_25> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_24> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_23> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_22> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_21> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_20> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_19> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_18> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_17> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_16> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_15> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_14> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_13> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_12> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_11> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_10> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/readDataOut_9> (without init value) has a constant value of 0 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_0> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_1> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_2> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_3> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_4> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_5> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_6> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_7> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_8> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_9> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_10> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_11> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_12> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_13> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_14> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_15> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_16> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_17> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_18> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_19> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_20> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_21> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_22> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_23> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_24> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_25> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_26> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_27> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_28> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_29> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_30> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <IF_ID/PCplus4Out_31> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_0> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_1> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_2> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_3> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_4> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_5> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_6> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_7> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_8> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_9> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_10> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_11> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_12> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_13> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_14> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_15> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_16> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_17> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_18> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_19> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_20> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_21> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_22> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_23> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_24> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_25> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_26> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_27> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_28> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_29> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_30> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <PCRegister/outPC_31> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ALUOpOut_3> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_31> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_30> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_29> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_28> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_27> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_26> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_25> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_24> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_23> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_22> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_21> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_20> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_19> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_18> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_17> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_16> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_15> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_14> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_13> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_12> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_11> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_10> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_9> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_8> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_7> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_6> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_5> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_4> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_3> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_2> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_1> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/PCplus4out_0> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ALU/overFlow> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <controlUnit/RegDst> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <ID_EX/RegDstOut> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:638 - in unit MipsPipelineTestBench Conflict on KEEP property on signal N0 and writeRegWB<0> writeRegWB<0> signal will be lost.

WARNING:Xst:638 - in unit MipsPipelineTestBench Conflict on KEEP property on signal N0 and writeRegWB<1> writeRegWB<1> signal will be lost.

WARNING:Xst:638 - in unit MipsPipelineTestBench Conflict on KEEP property on signal N0 and writeRegWB<2> writeRegWB<2> signal will be lost.

WARNING:Xst:638 - in unit MipsPipelineTestBench Conflict on KEEP property on signal N0 and writeRegWB<3> writeRegWB<3> signal will be lost.

WARNING:Xst:638 - in unit MipsPipelineTestBench Conflict on KEEP property on signal N0 and writeRegWB<4> writeRegWB<4> signal will be lost.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_0> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory1> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_1> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory2> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_2> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory3> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_3> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory4> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_4> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory5> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_5> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory6> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_6> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory7> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_7> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory8> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_8> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory9> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_9> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory10> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_10> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory11> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_11> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory12> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_12> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory13> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_13> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory14> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_14> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory15> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_15> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory16> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_16> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory17> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_17> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory18> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_18> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory19> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_19> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory20> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_20> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory21> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_21> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory22> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_22> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory23> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_23> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory24> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_24> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory25> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_25> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory26> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_26> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory27> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_27> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory28> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_28> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory29> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_29> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory30> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_30> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory31> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <EX_MEM/writedataOut_31> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <dataMemory/Mram_memory32> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:638 - in unit MipsPipelineTestBench Conflict on KEEP property on signal N1 and IF_ID/PCplus4Out_not0001 IF_ID/PCplus4Out_not0001 signal will be lost.

WARNING:Xst:1294 - Latch <controlUnit/ALUop_1> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <controlUnit/RegWrite> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_31> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_30> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_29> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_28> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_27> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_26> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_25> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_24> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_23> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_22> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_21> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_20> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_19> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_18> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_17> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_16> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_15> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_14> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_13> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_12> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_11> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_10> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_9> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_8> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_7> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_6> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_5> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_4> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_3> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_2> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_1> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1294 - Latch <ALU/ALUResult_0> is equivalent to a wire in block <MipsPipelineTestBench>.

WARNING:Xst:1710 - FF/Latch <ID_EX/ALUOpOut_1> (without init value) has a constant value of 1 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <ID_EX/RegWriteOut> (without init value) has a constant value of 1 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <EX_MEM/RegWriteOut> (without init value) has a constant value of 1 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch <MEM_WB/RegWriteOut> (without init value) has a constant value of 1 in block <MipsPipelineTestBench>. This FF/Latch will be trimmed during the optimization process.

WARNING:Xst:638 - in unit MipsPipelineTestBench Conflict on KEEP property on signal IF_ID/PCplus4Out_not0001 and RegWriteWB RegWriteWB signal will be lost.

Mapping all equations...

Building and optimizing final netlist ...

WARNING:Xst:1898 - Due to constant pushing, FF/Latch <ID_EX/ReadData2_out_31> is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_30> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_29> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_28> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_27> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_26> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_25> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_24> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_23> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_22> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_21> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_20> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_19> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_18> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_17> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_16> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_15> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_14> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_13> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_12> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_11> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_10> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_9> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_8> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_7> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_6> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_5> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_4> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_3> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_2> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_1> of sequential type is unconnected in block <MipsPipelineTestBench>.

WARNING:Xst:2677 - Node <ID_EX/ReadData2_out_0> of sequential type is unconnected in block <MipsPipelineTestBench>.

Found area constraint ratio of 100 (+ 5) on block MipsPipelineTestBench, actual ratio is 1.

Final Macro Processing ...

Processing Unit <MipsPipelineTestBench> :

Found 3-bit shift register for signal <regWriteDataMEM<0>>.

Found 3-bit shift register for signal <regWriteDataMEM<1>>.

Found 3-bit shift register for signal <regWriteDataMEM<2>>.

Found 3-bit shift register for signal <regWriteDataMEM<3>>.

Found 3-bit shift register for signal <regWriteDataMEM<4>>.

Found 3-bit shift register for signal <regWriteDataMEM<5>>.

Found 3-bit shift register for signal <regWriteDataMEM<6>>.

Found 3-bit shift register for signal <regWriteDataMEM<7>>.

Found 3-bit shift register for signal <regWriteDataMEM<8>>.

Found 3-bit shift register for signal <regWriteDataMEM<9>>.

Found 3-bit shift register for signal <regWriteDataMEM<10>>.

Found 3-bit shift register for signal <regWriteDataMEM<11>>.

Found 3-bit shift register for signal <regWriteDataMEM<12>>.

Found 3-bit shift register for signal <regWriteDataMEM<13>>.

Found 3-bit shift register for signal <regWriteDataMEM<14>>.

Found 3-bit shift register for signal <regWriteDataMEM<15>>.

Found 3-bit shift register for signal <regWriteDataMEM<16>>.

Found 3-bit shift register for signal <regWriteDataMEM<17>>.

Found 3-bit shift register for signal <regWriteDataMEM<18>>.

Found 3-bit shift register for signal <regWriteDataMEM<19>>.

Found 3-bit shift register for signal <regWriteDataMEM<20>>.

Found 3-bit shift register for signal <regWriteDataMEM<21>>.

Found 3-bit shift register for signal <regWriteDataMEM<22>>.

Found 3-bit shift register for signal <regWriteDataMEM<23>>.

Found 3-bit shift register for signal <regWriteDataMEM<24>>.

Found 3-bit shift register for signal <regWriteDataMEM<25>>.

Found 3-bit shift register for signal <regWriteDataMEM<26>>.

Found 3-bit shift register for signal <regWriteDataMEM<27>>.

Found 3-bit shift register for signal <regWriteDataMEM<28>>.

Found 3-bit shift register for signal <regWriteDataMEM<29>>.

Found 3-bit shift register for signal <regWriteDataMEM<30>>.

Found 3-bit shift register for signal <regWriteDataMEM<31>>.

Unit <MipsPipelineTestBench> processed.

==========

Final Register Report

Macro Statistics

Shift Registers : 32

3-bit shift register : 32

==========

==========

* Partition Report *

==========

Partition Implementation Status

No Partitions were found in this design.

==========

* Final Report *

==========

Final Results

RTL Top Level Output File Name : MipsPipelineTestBench.ngr

Top Level Output File Name : MipsPipelineTestBench

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

IOs : 1

Cell Usage :

BELS : 5

GND : 2

INV : 2

VCC : 1

FlipFlops/Latches : 32

FD : 32

RAMS : 1

```
#      RAMB16                : 1
# Shift Registers             : 32
#      SRL16                 : 32
# Clock Buffers               : 1
#      BUFGP                 : 1
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s400pq208-4

 Number of Slices:                  16  out of   3584     0%
 Number of Slice Flip Flops:        32  out of   7168     0%
 Number of 4 input LUTs:            34  out of   7168     0%
    Number used as logic:           2
    Number used as Shift registers: 32
 Number of IOs:                     1
 Number of bonded IOBs:             1  out of    141     0%
 Number of BRAMs:                   1  out of     16     6%
 Number of GCLKs:                   1  out of      8    12%

---------------------------
Partition Resource Summary:
---------------------------
```

No Partitions were found in this design.

==========

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	66

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -4

Minimum period: 4.010ns (Maximum Frequency: 249.377MHz)

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

===

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 4.010ns (frequency: 249.377MHz)

Total number of paths / destination ports: 64 / 64

Delay: 2.005ns (Levels of Logic = 1)

Source: regWriteDataMEM_31 (FF)

Destination: regiterFile/Mram_memory/regiterFile/Mram_memory (RAM)

Source Clock: clk rising

Destination Clock: clk falling

Data Path: regWriteDataMEM_31 to regiterFile/Mram_memory/regiterFile/Mram_memory

```
                      Gate     Net
   Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
   ----------------------------------------  ------------
    FD:C->Q             1   0.720   0.801  regWriteDataMEM_31 (regWriteDataMEM<31>)
    begin scope: 'regiterFile/Mram_memory'
    RAMB16:DIA31                0.484         regiterFile/Mram_memory
   ----------------------------------------
   Total                    2.005ns (1.204ns logic, 0.801ns route)
                               (60.0% logic, 40.0% route)

========================================================================


Total REAL time to Xst completion: 13.00 secs
Total CPU time to Xst completion: 12.56 secs

-->


Total memory usage is 251804 kilobytes


Number of errors   :    0 (   0 filtered)
Number of warnings :  431 (   0 filtered)
Number of infos    :   18 (   0 filtered)
```