Report

Memory instructions

 T_0 : $AR \leftarrow PC$

 T_1 : $IR \leftarrow M[AR]$, $PC \leftarrow PC + 1$

 T_2 : $D_0, \ldots, D_7 \leftarrow \text{Decode } IR(12-14), AR \leftarrow IR(0-11), I \leftarrow IR(15)$

(T_0 , T_1 and T_2 are common signals between all instructions)

LDA

 D_2T_4 : $DR \leftarrow M[AR]$

 D_2T_5 : $AC \leftarrow DR$, $SC \leftarrow 0$

ADD

 D_1T_4 : $DR \leftarrow M[AR]$

 D_1T_5 : $AC \leftarrow AC + DR$, $E \leftarrow C_{out}$, $SC \leftarrow 0$

AND

$$D_0T_4$$
: $DR \leftarrow M[AR]$

$$D_0T_5$$
: $AC \leftarrow AC \land DR$, $SC \leftarrow 0$

STA

$$D_3T_4$$
: $M[AR] \leftarrow AC$, $SC \leftarrow 0$

SUB

D₅T₄: DR \leftarrow M[AR]

D₅T₅: AC \leftarrow DR , DR \leftarrow AC

D₅T₆: AC \leftarrow DR-AC, E \leftarrow Cout, SC \leftarrow 0

SZA

 $D_7T_3B_2$: if(AC=0) then PC \leftarrow PC+1, SC \leftarrow 0

INC

D₇T₃B₅: DR← AC

 $D_7T_4B_5$: AC \leftarrow DR+1, SC \leftarrow 0

control signals

en AR

 T_0+T_2

en TR

0

en DR

 $D_2T_4+D_1T_4+D_5T_4+D_5T_5+D_7T_3B_5+D_0T_4=$ $D_5(T_4+T_5)+D_2T_4+D_1T_4+D_7T_3B_5+D_0T_4$

en AC

 $D_2T_5+D_1T_5+D_5T_5+D_5T_6+D_7T_4B_5+D_0T_5 = D_2T_5+D_1T_5+D_5(T_5+T_6)+D_7T_4B_5+D_0T_5$

en PC

D4T4

inc PC

 $T_1+D_7T_3B_2(OR(AC(0-15))')$

en IR

T1

Clr SC

$$D_2T_5+D_1T_5+D_5T_6+D_7T_3B_2+D_4T_4$$

+ $D_7T_4B_5+D_0T_5+D_3T_4=$
 $T_5(D_0+D_{1+}D_2)+T_4(D_3+D_4)+$
+ $D_5T_6+D_7T_3B_2+D_7T_4B_5$

en Write(Memory)

 D_3T_4

en Read(Memory)

$$T_1+ D_2T_4+ D_1T_4+ D_5T_4+ D_0T_4 =$$
 $T_1+ T_4 (D_2+ D_1+ D_5+ D_0)$

ALU Selection lines signal

000	0
001 (SUM)	D_1T_5
010 (SUB)	D_5T_6
011(Transfer)	$D_2T_5+D_5T_5=$
	$T_5(D_5+D_2)$
100 (AND)	D_0T_5
101 (OR)	0
110 (XOR)	0
111	D ₇ T ₄ B ₅
(Increment by 1)	

BUS Selection lines signal

000 (Mem)	$T_1+ T_4 (D_2+ D_1+ D_5+ D_0)=$ en Read
001 (AR)	D ₄ T ₄
010 (TR)	0
011 (DR)	0
100 (AC)	$D_7T_4B_5+D_3T_4+D_5T_5$
101 (PC)	T_0
110 (IR)	T ₂
111	
(Nothing)	