Report

Firstly, we are trying to implement a smart car which is controlled mainly by using 2 sensors which are the IR sensors and the land detector sensor (LN).

We implemented the code as follows to cover all cases for of both sensors. which are:

- 1- Both sensors read an input so the motor is stopped and the word ALERT gets displayed on the 7-Segment display.
- 2-the IR sensor reads an input so the motor is stopped and nothing is displayed on the 7-Segment display.
- 3- the LN sensor reads an input so the word ALERT gets displayed on the 7-Segment display and the motor will still operate .
- 4-if both sensors does not read any input the motor will still operate and nothing is displayed on the 7-Segment display.

Not: Both sensors are triggered by the negative edge so we they are 0 that means that they read an input.

Here is the VHDL code:

```
| Tibrary IEEE: use IEEE. STDLOGIC_1164.ALL;
|-- Declare the input and output signals Bentity Car in STD_LOGIC; infrared_sensor: in STD_LOGIC; in STD_LOGIC
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Here id the Pin assignment for the FBGA:

Node Name	Direction	Location	I/O Bank	/REF Group	tter Locatic	'O Standarı	Reserved	rent Stren	Slew Rate	fferential P	ct Preserva
🚣 infrarsensor	Input	PIN_V9	3	B3_N0	PIN_V9	2.5 V		12mAult)			
lane_sensor	Input	PIN_V10	3	B3_N0	PIN_V10	2.5 V		12mAult)			
motor_control	Output	PIN_V8	3	B3_N0	PIN_V8	2.5 V		12mAult)	2 (default)		
seg1[0]	Output	PIN_J20	6	B6_N0	PIN_J20	2.5 V		12mAult)	2 (default)		
seg1[1]	Output	PIN_K20	6	B6_N0	PIN_K20	2.5 V		12mAult)	2 (default)		
seg1[2]	Output	PIN_L18	6	B6_N0	PIN_L18	2.5 V		12mAult)	2 (default)		
seg1[3]	Output	PIN_N18	6	B6_N0	PIN_N18	2.5 V		12mAult)	2 (default)		
seg1[4]	Output	PIN_M20	6	B6_N0	PIN_M20	2.5 V		12mAult)	2 (default)		
seg1[5]	Output	PIN_N19	6	B6_N0	PIN_N19	2.5 V		12mAult)	2 (default)		
seg1[6]	Output	PIN_N20	6	B6_N0	PIN_N20	2.5 V		12mAult)	2 (default)		
seg2[0]	Output	PIN_F18	6	B6_N0	PIN_F18	2.5 V		12mAult)	2 (default)		
seg2[1]	Output	PIN_E20	6	B6_N0	PIN_E20	2.5 V		12mAult)	2 (default)		
seg2[2]	Output	PIN_E19	6	B6_N0	PIN_E19	2.5 V		12mAult)	2 (default)		
seg2[3]	Output	PIN J18	6	B6 N0	PIN J18	2.5 V		12mAult)	2 (default)		
seg2[4]	Output	PIN H19	6	B6 N0	PIN H19	2.5 V		12mAult)	2 (default)		
seg2[5]	Output	PIN F19	6	B6_N0	PIN F19	2.5 V		12mAult)	2 (default)		
seg2[6]	Output	PIN F20	6	B6 N0	PIN F20	2.5 V		12mAult)	2 (default)		
seg3[0]	Output	PIN F21	6	B6 N0	PIN F21	2.5 V		12mAult)	2 (default)		
¥ seg3[1]	Output	PIN E22	6	B6_N0	PIN E22	2.5 V		12mAult)			
seg3[2]	Output	PIN E21	6	B6 N0	PIN E21	2.5 V		12mAult)	2 (default)		
seg3[3]	Output	PIN C19	7	B7 N0	PIN C19	2.5 V		12mAult)	2 (default)		
¥ seg3[4]	Output	PIN C20	6	B6 N0	PIN C20	2.5 V		12mAult)			
¥ seg3[5]	Output	PIN D19	6	B6 N0	PIN D19	2.5 V		12mAult)	2 (default)		
seg3[6]	Output	PIN E17	6	B6 N0	PIN E17	2.5 V		12mAult)	2 (default)		
≌ seg4[0]	Output	PIN B20	6	B6 N0	PIN B20	2.5 V		12mAult)	2 (default)		
≅ seg4[1]	Output	PIN A20	7	B7 N0	PIN A20	2.5 V		12mAult)			
seg4[2]	Output	PIN B19	7	B7 N0	PIN B19	2.5 V		12mAult)			
≤ seg4[3]	Output	PIN A21	6	B6 N0	PIN A21	2.5 V		12mAult)			
seg4[4]	Output	PIN_B21	6	B6_N0	PIN_B21	2.5 V		12mAult)			
seg4[5]	Output	PIN C22	6	B6 N0	PIN C22	2.5 V		12mAult)			
≤ seg4[6]	Output	PIN B22	6	B6 N0	PIN_B22	2.5 V		12mAult)			
≅ seg5[0]	Output	PIN_C18	7	B7_N0	PIN C18	2.5 V		12mAult)			
seg5[1]	Output	PIN D18	6	B6 N0	PIN D18	2.5 V		12mAult)			
≝ seg5[2]	Output	PIN E18	6	B6 N0	PIN E18	2.5 V		12mAult)			
seg5[3]	Output	PIN_B16	7	B7_N0	PIN B16	2.5 V		12mAult)			
seg5[4]	Output	PIN A17	7	B7 N0	PIN A17	2.5 V		12mAult)			
seg5[5]	Output	PIN A18	7	B7 N0	PIN A18	2.5 V		12mAult)			
≅ seg5[6]	Output	PIN B17	7	B7 N0	PIN B17	2.5 V		12mAult)			
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