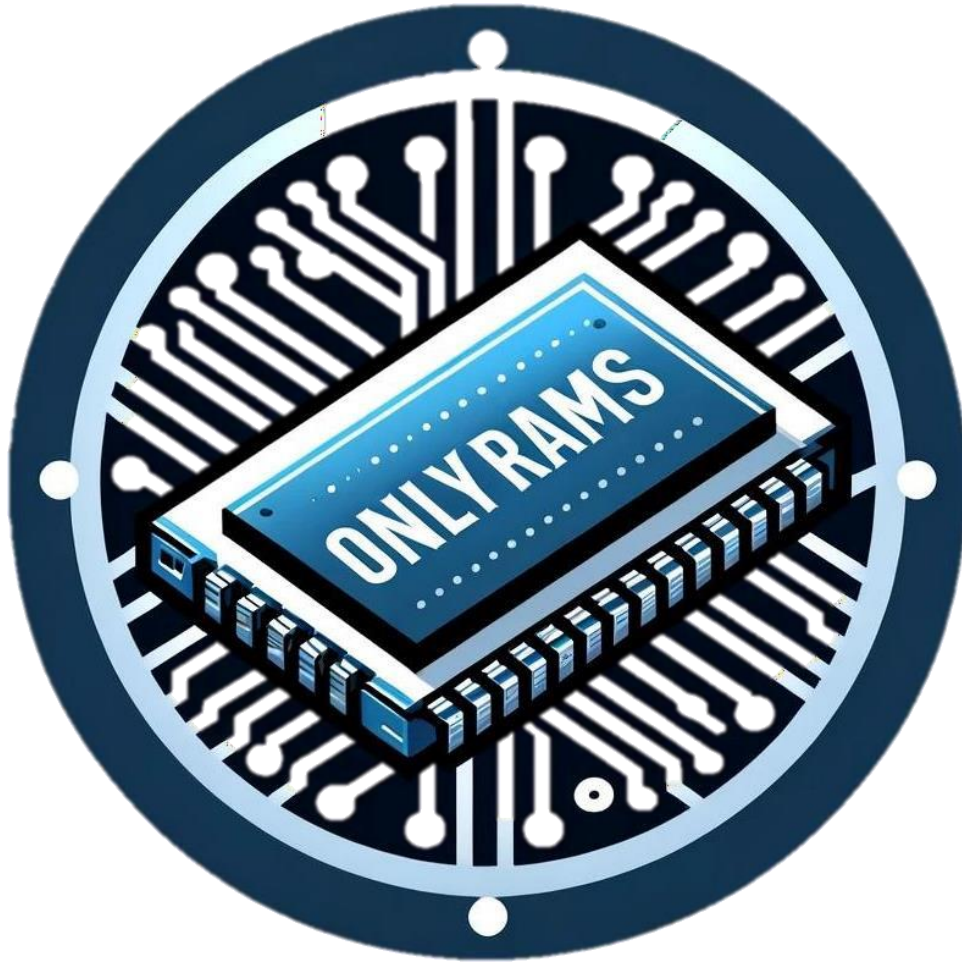


Project 1: DSP

Team: OnlyRAMs



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RTL Code:

```
module sel_reg(D,clk,E,rst,out);
parameter size=18;
parameter z=1;
parameter RSTTYPE="SYNC";
input [size-1:0] D;
input clk,rst,E;
output [size-1:0]out;
reg [size-1:0]temp;
generate
    if (z) begin
        if(RSTTYPE=="SYNC")begin
            always @(posedge clk ) begin
                if(rst)temp<=0;
                else if(E)temp<=D;
            end
        end
        else begin
            always @(posedge clk or posedge rst) begin
                if(rst)temp<=0;
                else if(E)temp<=D;
            end
        end
        assign out = temp;
    end
else assign out=D;
endgenerate
endmodule
```

```
module DSP48A1(A,B,Bcin,C,D,carryin,M,P,carryout,
carryoutF,clk,opmode,ceA,ceB,ceC,cecarryin,ceD,ceM,ceopmode
,ceP,rstA,rstB,rstC,rstcarryin,rstD,rstM,rstopmode,rstP,Bcout,Pcin,Pcout);
```

```
//parameters
parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;
parameter CREG = 1;
parameter DREG = 1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE = "SYNC";
```

```
//inputs
input [17:0] A,B,D;
input [47:0] C,Pcin;
input [17:0] Bcin;
input clk,carryin;
input [7:0] opmode;
input rstA,rstB,rstM,rstP,rstC,rstD,rstcarryin,rstopmode;
input ceA,ceB,ceM,ceP,ceC,ceD,cecarryin,ceopmode;
```

```
//outputs
output [17:0] Bcout;
output [47:0] Pcout,P;
output [35:0] M;
output carryout,carryoutF;
```

```
//wires
wire [17:0] Bmux_out;
wire [17:0] A0REG_out,B0REG_out,DREG_out,A1REG_out,adder1,adder1_mux_out,B1REG_out;
wire [47:0] CREG_out,PREG_out;
wire [35:0] multiply_out,MREG_out,M_buff;
wire carryin_MUX_out,CIN;
wire [7:0] opmode_reg_out;
wire [47:0] DAB_conc;
wire [47:0] Xmux_out,Zmux_out,adder2_out;
```

```

//reg
reg [47:0] reg_X_temp, reg_Z_temp;

//
// verilog design
//

assign Bmux_out=(B_INPUT == "DIRECT")? B : (B_INPUT == "CASCADE")? Bcin:0;

sel_reg #(18,A0REG,RSTTYPE) _A0REG(A,clk,ceA,rstA,A0REG_out);//A0REG
sel_reg #(18,A1REG,RSTTYPE) _A1REG(A0REG_out,clk,ceA,rstA,A1REG_out);//A1REG
sel_reg #(18,B0REG,RSTTYPE) _B0REG(Bmux_out,clk,ceB,rstB,B0REG_out);//B0REG
sel_reg #(48,CREG,RSTTYPE) _CREG(C,clk,ceC,rstC,CREG_out);//CREG
sel_reg #(18,DREG,RSTTYPE) _DREG(D,clk,ceD,rstD,DREG_out);//DREG
sel_reg #(8,OPMODEREG,RSTTYPE) _OPMODEREG(opmode,clk,ceopmode,rstopmode,opmode_reg_out);//opcodereg

assign adder1=(opmode_reg_out[6])? (DREG_out-B0REG_out) : (DREG_out+B0REG_out);//first adder
assign adder1_mux_out=(opmode_reg_out[4])? adder1 : B0REG_out;

sel_reg #(18,B1REG,RSTTYPE) _B1REG(adder1_mux_out,clk,ceB,rstB,B1REG_out); //B1REG

assign Bcout=B1REG_out;

assign multiply_out=A1REG_out*B1REG_out;

sel_reg #(36,MREG,RSTTYPE) _MREG(multiply_out,clk,ceM,rstM,MREG_out);//MREG
assign M_buff=MREG_out;
assign M=M_buff;
assign carryin_MUX_out=(CARRYINSEL == "OPMODE5")? opmode_reg_out[5]:(CARRYINSEL == "CARRYIN")? carryin : 0;

sel_reg #(1,CARRYINREG,RSTTYPE) _CYI(carryin_MUX_out,clk,cecarryin,rstcarryin,CIN);
//

```

```

//
//
always @(*) begin
    case (opmode_reg_out[1:0])
        0: reg_X_temp=0;
        1: reg_X_temp={12'b0,MREG_out};
        2: reg_X_temp=Pcout;
        3: reg_X_temp=DAB_conc;
    endcase
end
assign DAB_conc={DREG_out[11:0],A1REG_out,B1REG_out};
assign Xmux_out=reg_X_temp;
//
//
always @(*) begin
    case (opmode_reg_out[3:2])
        0: reg_Z_temp=0;
        1: reg_Z_temp=Pcin;
        2: reg_Z_temp=Pcout;
        3: reg_Z_temp=CREG_out;
    endcase
end
assign Zmux_out=reg_Z_temp;
assign {carry,adder2_out}=(opmode_reg_out[7])?(Zmux_out-(Xmux_out+carryin)):(Zmux_out+Xmux_out+carryin);

sel_reg #(48,PREG,RSTTYPE) _PREG(adder2_out,clk,ceP,rstP,P);

assign Pcout=P;

sel_reg #(1,CARRYOUTREG,RSTTYPE) _CARRYOUTREG(carry,clk,cecarryin,rstcarryin,carryout);
assign carryoutF=carryout;
assign Pcout=P;
endmodule

```

Testbench Code:

```
module DSP_TB();
    reg [17:0] A,B,D;
    reg [47:0] C,Pcin;
    reg [17:0] Bcin;
    reg clk,carryin;
    reg [7:0] opmode;
    reg rstA,rstB,rstM,rstP,rstC,rstD,rstcarryin,rstopmode;
    reg ceA,ceB,ceM,ceP,ceC,ceD,cecarryin,ceopmode;

    wire [17:0] Bcout_dut;
    wire [47:0] Pcout_dut,P_dut;
    wire [35:0] M_dut;
    wire carryout_dut,carryoutF_dut;

    DSP48A1 dut(A,B,Bcin,C,D,carryin,M_dut,P_dut,carryout_dut,carryoutF_dut,
        clk,opmode,ceA,ceB,ceC,cecarryin,ceD,ceM,ceopmode,ceP,rstA,
        rstB,rstC,rstcarryin,rstD,rstM,rstopmode
        ,rstP,Bcout_dut,Pcin,Pcout_dut);

    initial begin
        clk=0;
        forever begin
            #5;
            clk=~clk;
        end
    end
end
```

```

initial begin
    rstA=1;
    rstB=1;
    rstM=1;
    rstP=1;
    rstC=1;
    rstD=1;
    rstcarryin=1;
    rstopmode=1;
    repeat(50)begin
        ceA=$random;
        ceB=$random;
        ceM=$random;
        ceP=$random;
        ceC=$random;
        ceD=$random;
        cecarryin=$random;
        ceopmode=$random;
        A=$random;
        B=$random;
        D=$random;
        C=$random;
        Pcin=$random;
        Bcin=$random;
        carryin=$random;
        opmode=$random;
        @(negedge clk);
        if(M_dut!=0 || P_dut!=0 || Bcout_dut!=0 || carryout_dut!=0 || carryoutF_dut!=0 || P_dut!=0)begin
            $display("Error");
            $stop;
        end
    end
end

```



```

rstA=0;
rstB=0;
rstM=0;
rstP=0;
rstC=0;
rstD=0;
rstcarryin=0;
rstopmode=0;
ceA=1;
ceB=1;
ceM=1;
ceP=1;
ceC=1;
ceD=1;
cecarryin=1;
ceopmode=1;
A=2;
C=0;
D=1;
B=1;
opmode[6] = 0; //adder1 = D+B
opmode[4] = 1; //adder1_mux_out
opmode[1:0] = 1;
opmode[3:2] = 0;
opmode[7] = 0;
carryin = 0;
@(negedge clk);
//output Bcout = 2 , p=2 , M = 2 , PCout = 2
repeat(100) begin
    A=$random;
    B=$random;
    D=$random;
    C=$random;
    Pcin=$random;
    Bcin=$random;
    carryin=$random;
    opmode=$random;
    @(negedge clk);
end
$stop;
end

```

```

initial begin
    $monitor("input: A = %d\t B = %d\t C = %d\t D = %d\t PCin = %d\t carryin = %d\t opmode = %d\t \n output: Bcout = %d\t PCout = %d\t P = %d\t M = %d\t Carry_Out = %d\t Carry_OutF = %d",
    A,B,C,D,PCin,carryin,opmode,Bcout_dut,PCout_dut,P_dut,M_dut,carryout_dut,carryoutF_dut);
end
endmodule

```

Do file:

```
run_dsp_tb.do
1  vlib work
2  vlog DSP48A1.v sel_reg.v DSP_TB.v
3  vsim -voptargs=+acc work.DSP_TB
4  add wave *
5  run -all
```

QuestaSim Snippets:

POP: 75A	00000004	11004	12004	13004	14004	15004	16004	17004	18004	19004	20004	21004	22004	23004	24004	25004	26004	27004	28004	29004	30004	31004	32004	33004	34004	35004	36004	37004	38004	39004	40004	41004	42004	43004	44004	45004	46004	47004	48004	49004	50004	51004	52004	53004	54004	55004	56004	57004	58004	59004	60004	61004	62004	63004	64004	65004	66004	67004	68004	69004	70004	71004	72004	73004	74004	75004	76004	77004	78004	79004	80004	81004	82004	83004	84004	85004	86004	87004	88004	89004	90004	91004	92004	93004	94004	95004	96004	97004	98004	99004	100004	101004	102004	103004	104004	105004	106004	107004	108004	109004	110004	111004	112004	113004	114004	115004	116004	117004	118004	119004	120004	121004	122004	123004	124004	125004	126004	127004	128004	129004	130004	131004	132004	133004	134004	135004	136004	137004	138004	139004	140004	141004	142004	143004	144004	145004	146004	147004	148004	149004	150004	151004	152004	153004	154004	155004	156004	157004	158004	159004	160004	161004	162004	163004	164004	165004	166004	167004	168004	169004	170004	171004	172004	173004	174004	175004	176004	177004	178004	179004	180004	181004	182004	183004	184004	185004	186004	187004	188004	189004	190004	191004	192004	193004	194004	195004	196004	197004	198004	199004	200004	201004	202004	203004	204004	205004	206004	207004	208004	209004	210004	211004	212004	213004	214004	215004	216004	217004	218004	219004	220004	221004	222004	223004	224004	225004	226004	227004	228004	229004	230004	231004	232004	233004	234004	235004	236004	237004	238004	239004	240004	241004	242004	243004	244004	245004	246004	247004	248004	249004	250004	251004	252004	253004	254004	255004	256004	257004	258004	259004	260004	261004	262004	263004	264004	265004	266004	267004	268004	269004	270004	271004	272004	273004	274004	275004	276004	277004	278004	279004	280004	281004	282004	283004	284004	285004	286004	287004	288004	289004	290004	291004	292004	293004	294004	295004	296004	297004	298004	299004	300004	301004	302004	303004	304004	305004	306004	307004	308004	309004	310004	311004	312004	313004	314004	315004	316004	317004	318004	319004	320004	321004	322004	323004	324004	325004	326004	327004	328004	329004	330004	331004	332004	333004	334004	335004	336004	337004	338004	339004	340004	341004	342004	343004	344004	345004	346004	347004	348004	349004	350004	351004	352004	353004	354004	355004	356004	357004	358004	359004	360004	361004	362004	363004	364004	365004	366004	367004	368004	369004	370004	371004	372004	373004	374004	375004	376004	377004	378004	379004	380004	381004	382004	383004	384004	385004	386004	387004	388004	389004	390004	391004	392004	393004	394004	395004	396004	397004	398004	399004	400004	401004	402004	403004	404004	405004	406004	407004	408004	409004	410004	411004	412004	413004	414004	415004	416004	417004	418004	419004	420004	421004	422004	423004	424004	425004	426004	427004	428004	429004	430004	431004	432004	433004	434004	435004	436004	437004	438004	439004	440004	441004	442004	443004	444004	445004	446004	447004	448004	449004	450004	451004	452004	453004	454004	455004	456004	457004	458004	459004	460004	461004	462004	463004	464004	465004	466004	467004	468004	469004	470004	471004	472004	473004	474004	475004	476004	477004	478004	479004	480004	481004	482004	483004	484004	485004	486004	487004	488004	489004	490004	491004	492004	493004	494004	495004	496004	497004	498004	499004	500004	501004	502004	503004	504004	505004	506004	507004	508004	509004	510004	511004	512004	513004	514004	515004	516004	517004	518004	519004	520004	521004	522004	523004	524004	525004	526004	527004	528004	529004	530004	531004	532004	533004	534004	535004	536004	537004	538004	539004	540004	541004	542004	543004	544004	545004	546004	547004	548004	549004	550004	551004	552004	553004	554004	555004	556004	557004	558004	559004	560004	561004	562004	563004	564004	565004	566004	567004	568004	569004	570004	571004	572004	573004	574004	575004	576004	577004	578004	579004	580004	581004	582004	583004	584004	585004	586004	587004	588004	589004	590004	591004	592004	593004	594004	595004	596004	597004	598004	599004	600004	601004	602004	603004	604004	605004	606004	607004	608004	609004	610004	611004	612004	613004	614004	615004	616004	617004	618004	619004	620004	621004	622004	623004	624004	625004	626004	627004	628004	629004	630004	631004	632004	633004	634004	635004	636004	637004	638004	639004	640004	641004	642004	643004	644004	645004	646004	647004	648004	649004	650004	651004	652004	653004	654004	655004	656004	657004	658004	659004	660004	661004	662004	663004	664004	665004	666004	667004	668004	669004	670004	671004	672004	673004	674004	675004	676004	677004	678004	679004	680004	681004	682004	683004	684004	685004	686004	687004	688004	689004	690004	691004	692004	693004	694004	695004	696004	697004	698004	699004	700004	701004	702004	703004	704004	705004	706004	707004	708004	709004	710004	711004	712004	713004	714004	715004	716004	717004	718004	719004	720004	721004	722004	723004	724004	725004	726004	727004	728004	729004	730004	731004	732004	733004	734004	735004	7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# input: A = 178975 B = 112491 C = 1263109014 D = 196221 PCin = 281472921665547 carryin = 1 opmode = 63
# output: Bcout = 92077 PCout = 281474706953440 P = 281474706953440 M = 17205382324 Carry_Out = 0 Carry_OutF = 0
# input: A = 178975 B = 112491 C = 1263109014 D = 196221 PCin = 281472921665547 carryin = 1 opmode = 63
# output: Bcout = 83987 PCout = 281474706953441 P = 281474706953441 M = 11727018797 Carry_Out = 0 Carry_OutF = 0
# input: A = 120586 B = 146043 C = 281474488630981 D = 243245 PCin = 281474970659583 carryin = 0 opmode = 215
# output: Bcout = 83987 PCout = 281474706953441 P = 281474706953441 M = 11727018797 Carry_Out = 0 Carry_OutF = 0
# input: A = 120586 B = 146043 C = 281474488630981 D = 243245 PCin = 281474970659583 carryin = 0 opmode = 215
# output: Bcout = 80120 PCout = 254928719629225 P = 254928719629225 M = 15031573325 Carry_Out = 0 Carry_OutF = 0
# input: A = 239421 B = 202205 C = 281474802871019 D = 72474 PCin = 1766210002 carryin = 1 opmode = 38
# output: Bcout = 80120 PCout = 254928719629225 P = 254928719629225 M = 15031573325 Carry_Out = 0 Carry_OutF = 0
# input: A = 239421 B = 202205 C = 281474802871019 D = 72474 PCin = 1766210002 carryin = 1 opmode = 38
# output: Bcout = 41040 PCout = 172799639224537 P = 172799639224537 M = 9661350320 Carry_Out = 1 Carry_OutF = 1
# input: A = 35357 B = 75990 C = 281474026841742 D = 166898 PCin = 281474061863058 carryin = 0 opmode = 69
# output: Bcout = 41040 PCout = 172799639224537 P = 172799639224537 M = 9661350320 Carry_Out = 1 Carry_OutF = 1
# input: A = 35357 B = 75990 C = 281474026841742 D = 166898 PCin = 281474061863058 carryin = 0 opmode = 69
# output: Bcout = 75990 PCout = 172798724376939 P = 172798724376939 M = 9825837840 Carry_Out = 1 Carry_OutF = 1
# input: A = 57854 B = 86125 C = 281472867536900 D = 222375 PCin = 281473120009250 carryin = 0 opmode = 141
# output: Bcout = 75990 PCout = 172798724376939 P = 172798724376939 M = 9825837840 Carry_Out = 1 Carry_OutF = 1
# input: A = 57854 B = 86125 C = 281472867536900 D = 222375 PCin = 281473120009250 carryin = 0 opmode = 141
# output: Bcout = 86125 PCout = 7969136434 P = 7969136434 M = 2686778430 Carry_Out = 1 Carry_OutF = 1
# input: A = 67845 B = 28987 C = 281473470335052 D = 199119 PCin = 1703015371 carryin = 0 opmode = 227
# output: Bcout = 86125 PCout = 7969136434 P = 7969136434 M = 2686778430 Carry_Out = 1 Carry_OutF = 1
# input: A = 67845 B = 28987 C = 281473470335052 D = 199119 PCin = 1703015371 carryin = 0 opmode = 227
# output: Bcout = 28987 PCout = 281470180758470 P = 281470180758470 M = 4982675750 Carry_Out = 0 Carry_OutF = 0
# input: A = 92012 B = 223247 C = 1749545424 D = 55643 PCin = 397528367 carryin = 0 opmode = 238
# output: Bcout = 28987 PCout = 281470180758470 P = 281470180758470 M = 4982675750 Carry_Out = 0 Carry_OutF = 0
# input: A = 92012 B = 223247 C = 1749545424 D = 55643 PCin = 397528367 carryin = 0 opmode = 238
# output: Bcout = 223247 PCout = 108902585437893 P = 108902585437893 M = 1966623015 Carry_Out = 1 Carry_OutF = 1
# input: A = 152613 B = 202610 C = 39102212 D = 12980 PCin = 281474173692064 carryin = 1 opmode = 31
# output: Bcout = 223247 PCout = 108902585437893 P = 108902585437893 M = 1966623015 Carry_Out = 1 Carry_OutF = 1
# input: A = 152613 B = 202610 C = 39102212 D = 12980 PCin = 281474173692064 carryin = 1 opmode = 31
# output: Bcout = 202610 PCout = 172574140818186 P = 172574140818186 M = 20541402964 Carry_Out = 1 Carry_OutF = 1
# input: A = 14300 B = 23572 C = 281474749205732 D = 30773 PCin = 1730128334 carryin = 1 opmode = 164
# output: Bcout = 202610 PCout = 172574140818186 P = 172574140818186 M = 20541402964 Carry_Out = 1 Carry_OutF = 1
# input: A = 14300 B = 23572 C = 281474749205732 D = 30773 PCin = 1730128334 carryin = 1 opmode = 164
# output: Bcout = 36552 PCout = 47593923788407 P = 47593923788407 M = 30920919930 Carry_Out = 0 Carry_OutF = 0
# input: A = 224346 B = 6157 C = 711689044 D = 68102 PCin = 281474683005660 carryin = 0 opmode = 55
# output: Bcout = 36552 PCout = 47593923788407 P = 47593923788407 M = 30920919930 Carry_Out = 0 Carry_OutF = 0
# input: A = 224346 B = 6157 C = 711689044 D = 68102 PCin = 281474683005660 carryin = 0 opmode = 55
# output: Bcout = 6157 PCout = 281474683005660 P = 281474683005660 M = 522693600 Carry_Out = 0 Carry_OutF = 0
# input: A = 21579 B = 207623 C = 793864030 D = 83545 PCin = 1797362134 carryin = 1 opmode = 202
# output: Bcout = 6157 PCout = 281474683005660 P = 281474683005660 M = 522693600 Carry_Out = 0 Carry_OutF = 0
# input: A = 21579 B = 207623 C = 793864030 D = 83545 PCin = 1797362134 carryin = 1 opmode = 202
# output: Bcout = 13581 PCout = 176394785630692 P = 176394785630692 M = 1381298322 Carry_Out = 0 Carry_OutF = 0
# input: A = 216923 B = 161096 C = 686430545 D = 36096 PCin = 281473877244540 carryin = 1 opmode = 25
# output: Bcout = 13581 PCout = 176394785630692 P = 176394785630692 M = 1381298322 Carry_Out = 0 Carry_OutF = 0
# input: A = 216923 B = 161096 C = 686430545 D = 36096 PCin = 281473877244540 carryin = 1 opmode = 25
# output: Bcout = 161096 PCout = 281474976710655 P = 281474976710655 M = 293064399 Carry_Out = 1 Carry_OutF = 1
# input: A = 48319 B = 186257 C = 281474460383938 D = 147055 PCin = 281473902609535 carryin = 1 opmode = 24
# output: Bcout = 161096 PCout = 281474976710655 P = 281474976710655 M = 293064399 Carry_Out = 1 Carry_OutF = 1
# input: A = 48319 B = 186257 C = 281474460383938 D = 147055 PCin = 281473902609535 carryin = 1 opmode = 24
# output: Bcout = 222353 PCout = 293064399 P = 293064399 M = 34945427608 Carry_Out = 1 Carry_OutF = 1
# input: A = 65047 B = 77806 C = 281473701604455 D = 113169 PCin = 281472941495309 carryin = 1 opmode = 66
# output: Bcout = 222353 PCout = 293064399 P = 293064399 M = 34945427608 Carry_Out = 1 Carry_OutF = 1
# input: A = 65047 B = 77806 C = 281473701604455 D = 113169 PCin = 281472941495309 carryin = 1 opmode = 66
# output: Bcout = 224861 PCout = 293064400 P = 293064400 M = 10743874607 Carry_Out = 0 Carry_OutF = 0
# ** Note: $stop : DSP_TB.v(102)
# Time: 1510 ns Iteration: 1 Instance: /DSP_TB
# Break in Module DSP_TB at DSP_TB.v line 102

```

Constraint File:

```

6  ## Clock signal
7  set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVCMOS33 } [get_ports clk]
8  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
9
10

```

Tcl Console Messages x Log Reports Design Runs Find Results

Warning (65) Info (53) Status (24) Show All

Vivado Commands (3 infos)

- General Messages (3 infos)
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- Elaborated Design (22 warnings, 18 infos)
 - General Messages (22 warnings, 18 infos)
 - [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]
 - [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (6 more like this)



Tcl Console | **Messages** | Log | Reports | Design Runs

☒ Warning (43)
 ☒ Info (41)
 ☐ Status (21)
 Show All

- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- Synthesis (43 warnings, 32 infos)
 - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
 - [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]
 - > [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (6 more like this)
 - > [Synth 8-6155] done synthesizing module 'sel_reg' (1#1) [sel_reg.v:1] (6 more like this)
 - > [Synth 8-3331] design sel_reg has unconnected port clk (38 more like this)
 - [Device 21-403] Loading part xc7a200tffg1156-3

Tcl Console Messages Log Reports Design Runs Utilization x Timing						
Hierarchy						
Hierarchy						
Summary						
v Slice Logic						
v Slice LUTs (<1%)						
LUT as Logic (<1%)						
v Slice Registers (<1%)						
Register as Flip Flop (<1%)						
Memory						
v DSP						
v DSPs (<1%)						
DSP48E1 only						
v IO and GT Specific						
v Bonded IOB (65%)						
IOB Master Pads						
v Clocking						
BUFGCTRL (3%)						
Specific Feature						
Primitives						
Black Boxes						
Hierarchy						
Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	
v DSP48A1	229	158	1	327	1	
I _A1REG (sel_reg_pa...	0	18	0	0	0	
I _B1REG (sel_reg_pa...	0	18	0	0	0	
I _CARRYOUTREG (sel...	0	1	0	0	0	
I _CREG (sel_reg_par...	0	48	0	0	0	
I _DREG (sel_reg_par...	0	18	0	0	0	
I _MREG (sel_reg_par...	0	0	1	0	0	
I _OPMODEREG (sel_f...	228	7	0	0	0	
I _PREG (sel_reg_par...	0	48	0	0	0	

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General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (329)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

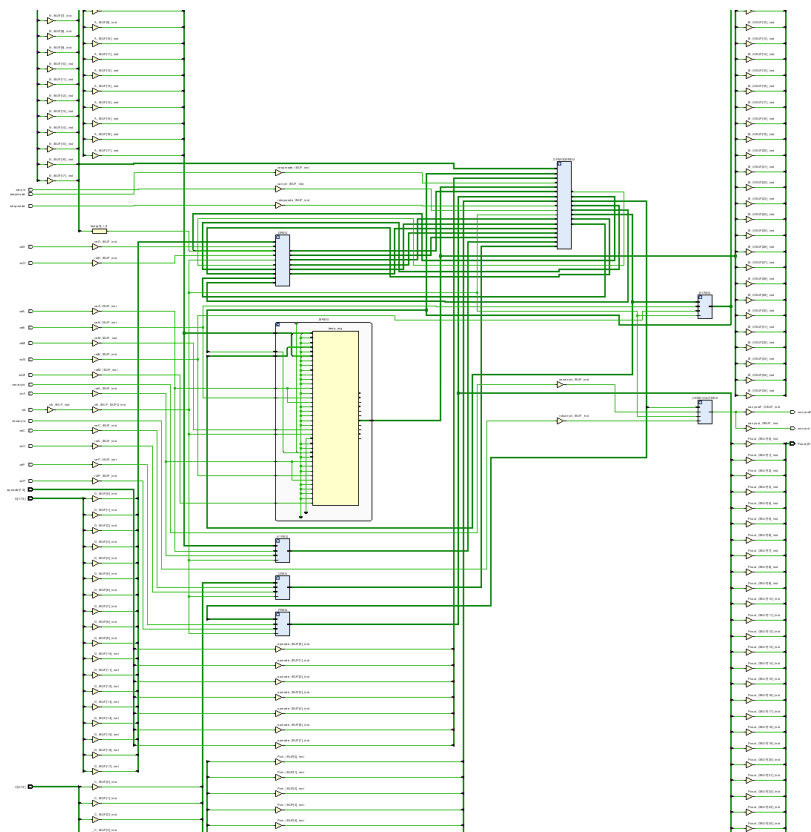
User Ignored Paths

Unconstrained Paths

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.168 ns	Worst Hold Slack (WHS): 0.339 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 86	Total Number of Endpoints: 86	Total Number of Endpoints: 160

All user specified timing constraints are met.



Tcl ConsoleMessagesLogReportsDesign RunsPowerDRCMethodologyTimingUtilization

HierarchySummary

Slice Logic

- Slice LUTs (<1%)
 - LUT as Logic (<1%)
- Slice Registers (<1%)
 - Register as Flip Flop (<1%)

Slice Logic Distribution

- Slice (1%)
 - SLICEM
 - SLICEL
- LUT Flip Flop Pairs (<1%)
 - LUT-FF pairs with one unused LUT output
 - LUT-FF pairs with one unused Flip Flop
- LUT as Logic (<1%)
 - using O5 and O6
 - using O6 output only

Memory

- DSP
 - DSPs (<1%)
 - DSP48E1 only
- IO and GT Specific
 - Bonded IOB (65%)
 - IOB Slave Pads
 - IOB Master Pads
- Clocking
 - BUFGCTRL (3%)
- Specific Feature
- Primitives
- Black Boxes
- Instantiated Netlists

Hierarchy

Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSP s (740)	Bonded IOB (500)	BUFGCTRL (32)
▼ DSP48A1	228	177	103	228	51	1	327	1
A1REG (sel_reg_pa...	0	18	5	0	0	0	0	0
B1REG (sel_reg_pa...	0	36	15	0	0	0	0	0
CARRYOUTREG (sel...	0	2	2	0	0	0	0	0
CREG (sel_reg_par...	0	48	17	0	0	0	0	0
DREG (sel_reg_par...	0	18	9	0	0	0	0	0
MREG (sel_reg_par...	0	0	0	0	0	1	0	0
OPMODEREG (sel_f...	228	7	70	228	0	0	0	0
PREG (sel_reg_par...	0	48	12	0	0	0	0	0

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General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (326)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

Unconstrained Paths

Design Timing Summary

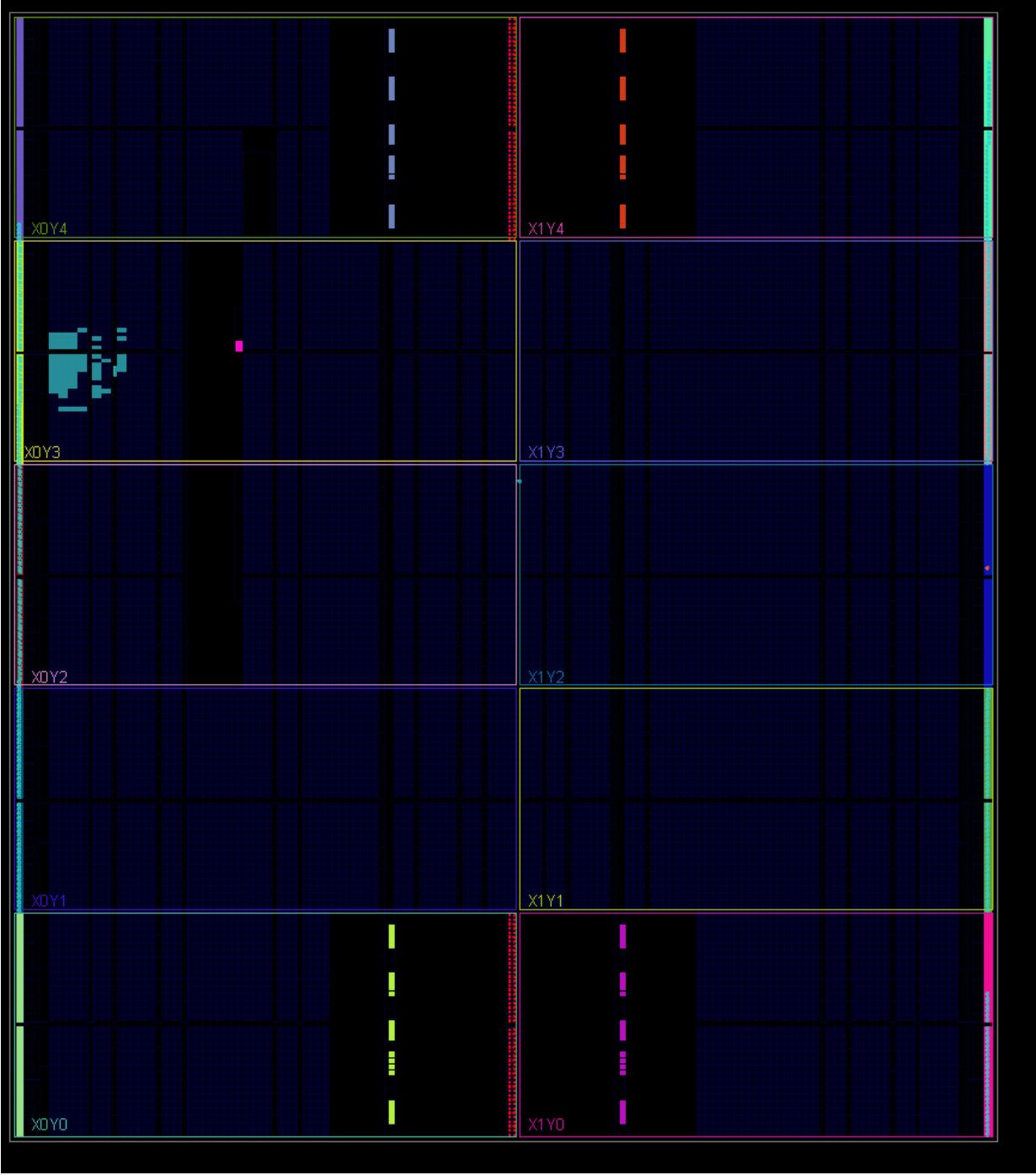
Setup

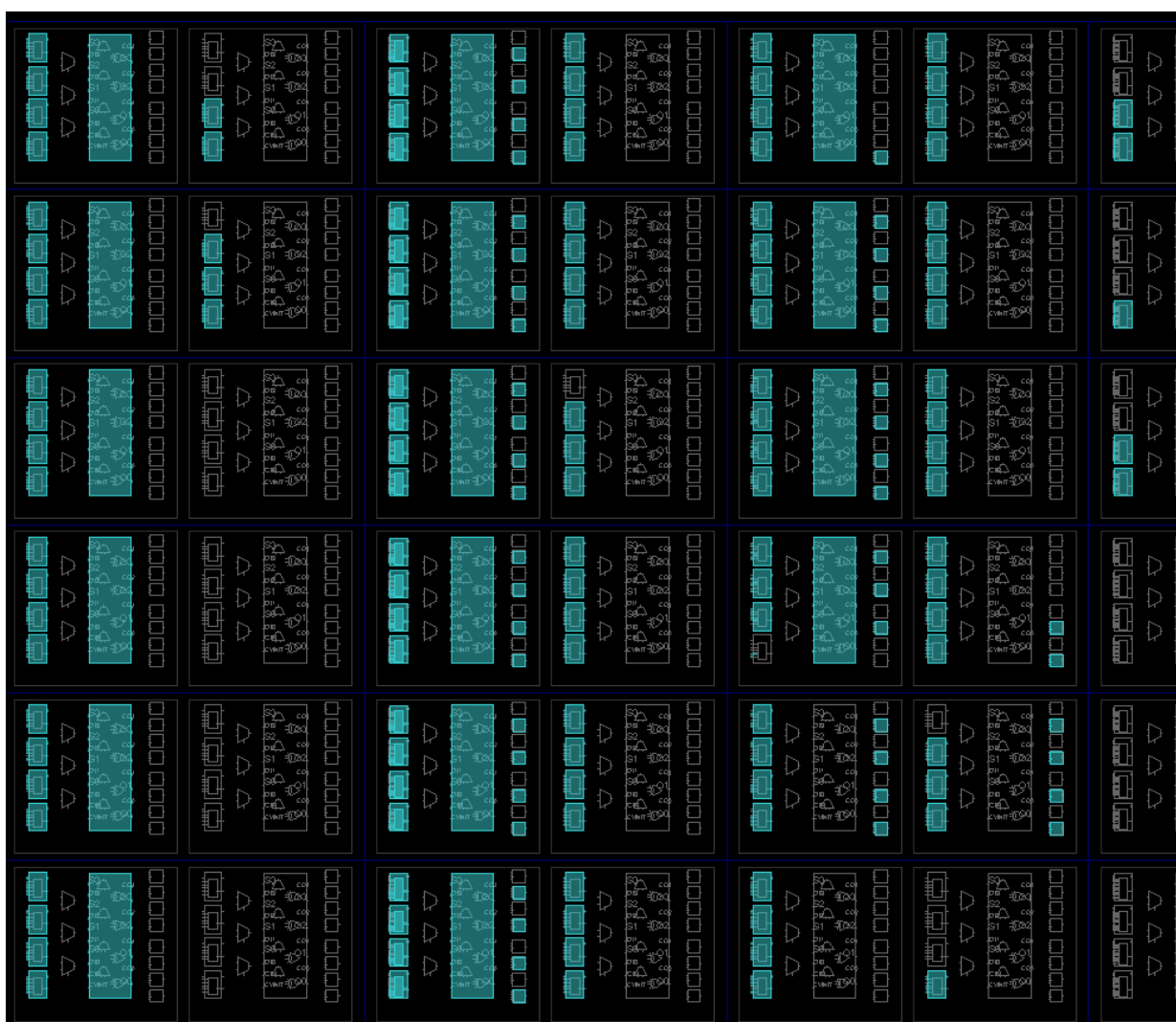
Hold

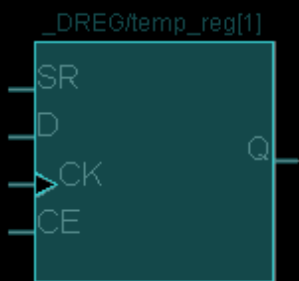
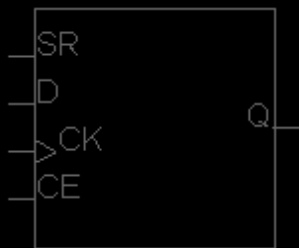
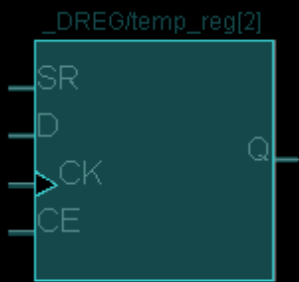
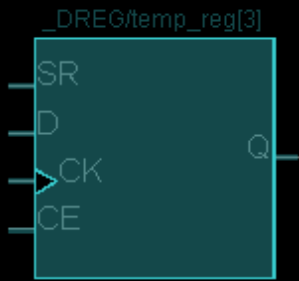
Pulse Width

Worst Negative Slack (WNS): 4.136 ns	Worst Hold Slack (WHS): 0.435 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 105	Total Number of Endpoints: 105	Total Number of Endpoints: 179

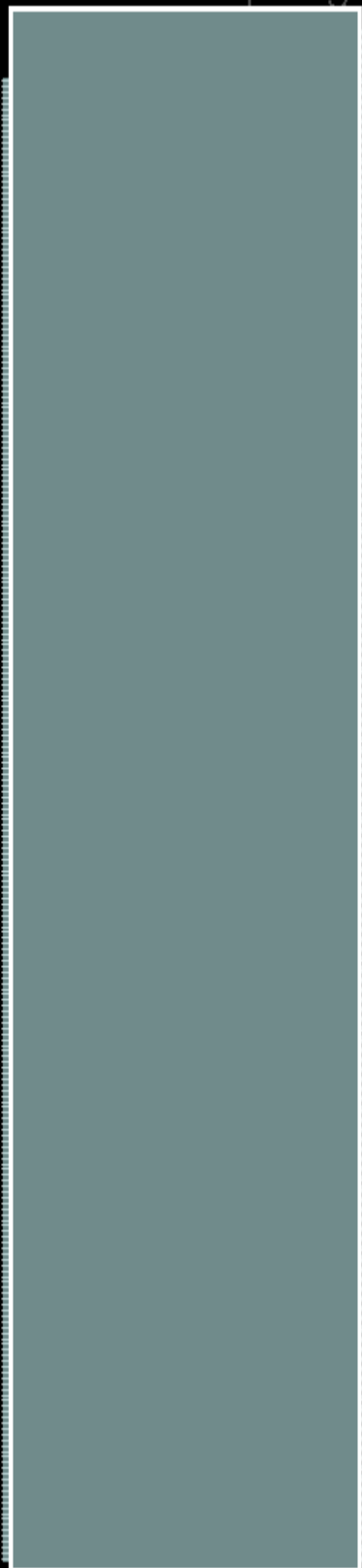
All user specified timing constraints are met.







MREG/temp_reg



MREG/temp_reg

