Counter

```verilog
module counter (clk,rst,pcount ,pci , pco , ef , ff, H );


input clk , rst , pci ,pco ;


output [2:0] pcount ;

output ef ,ff ,H ;


reg [2:0] pcount = 3'b000;


reg ef_1 = 1;

reg ff_1 = 0;


reg H ;

reg add;


always @(posedge clk, rst )

begin

H <= (~pci & ~pco) | (pco & pci) | (pco & ef_1) | (pci & ff_1);

add <= (pci & ~pco);

if(rst)

        begin

        pcount <= 0;

        ff_1 <= 0;
```

```verilog
            ef_1<= 1;


end


else if (H==1 )
pcount <= pcount ;


else if (add == 1)
begin


        if (pcount <= 3'b110 || ef_1==1)
        begin
        pcount <= pcount +1 ;
        ff_1 <= 1'b0;
        ef_1<=  1'b0;
        end
        else if( 3'b110 < pcount )
        begin
        pcount <= pcount;
        ff_1 <=1;
        ef_1 <=0;
        end
end
```

```verilog
        else if (add == 0)
        begin

                if(3'b000 < pcount <= 3'b111)

                begin

                pcount <= pcount-1;

                ff_1=0;

                ef_1=0;

                end

                if (pcount == 3'b000)

                begin

                ef_1 <= 1'b1 ;

                ff_1=0;

                pcount <= pcount;

                end

        end


        end

assign ef = ef_1;

assign ff = ff_1;



endmodule
```

FSM

```verilog
module FSM (clk,rst,in,out);

input clk,rst,in;

output out;

reg state;

reg out;


always @(posedge clk,posedge rst)

begin


if(rst)begin

        state <= 1'b0;

        out <= 0;

        end

else

begin

        case(state)

    1'b0:

        begin

        if(in) begin

        state <= 1'b0;

        out <=0; end

        else begin

        state <= 1'b1;
```

```verilog
                out <=1; end
            end
            1'b1:
            begin
            if(in) begin
            state <= 1'b0;
            out <=1; end
            else begin
            state <= 1'b1;
            out <=0; end
            end
            default: begin
            state<= 1'b0;
            out<=0; end
        endcase
    end
end
endmodule
```

Rom

```verilog
module new_rom(index,clk,ef,ff,reset,wtime);

input [4:0] index;//index is a five-bit number - the 2-MSBs is tcount | the 3-LSBs is pcount

input clk,ef,ff,reset;

output [4:0] wtime;

function [4:0] wait_time;

input [4:0] fn_input,empty_flag,full_flag,reset_;


begin

        //reset

        if(reset==1) begin

        fn_input=0;

        wait_time=5'b0000;

        end

        //empty flag check

        else if (ef==1)//no of people ==1, no of teller==1

        wait_time=5'b0000;

        //full flag check

        else if (ff==1) wait_time=5'b11111;


//tcount=1

        else if (1==1)

        begin

        case (fn_input)
```

```
        5'b01001: wait_time=5'b00011; //pcount =1 --wtime=3

        5'b01010: wait_time=5'b00110; //pcount =2 --wtime=6

        5'b01011: wait_time=5'b01001; //pcount =3 --wtime=9

        5'b01100: wait_time=5'b01100; //pcount =4 --wtime=12

        5'b01101: wait_time=5'b01111; //pcount =5 --wtime=15

        5'b01110: wait_time=5'b10010; //pcount =6 --wtime=18

        5'b01111: wait_time=5'b10101; //pcount =7 --wtime=21
//tcount=2


        5'b10001: wait_time=5'b00011;  //pcount =1 --wtime=3

        5'b10010: wait_time=5'b00101;  //pcount =2 --wtime=5

        5'b10011: wait_time=5'b00110;  //pcount =3 --wtime=6

        5'b10100: wait_time=5'b01000;  //pcount =4 --wtime=8

        5'b10101: wait_time=5'b01001;  //pcount =5 --wtime=9

        5'b10110: wait_time=5'b01011;  //pcount =6 --wtime=11

        5'b10111: wait_time=5'b01100;  //pcount =7 --wtime=12
//tcount=3


        5'b11001: wait_time=5'b00011;  //pcount =1 --wtime=3

        5'b11010: wait_time=5'b00100;  //pcount =1 --wtime=4

        5'b11011: wait_time=5'b00101;  //pcount =1 --wtime=5

        5'b11100: wait_time=5'b00110;  //pcount =1 --wtime=6

        5'b11101: wait_time=5'b00111;  //pcount =1 --wtime=7

        5'b11110: wait_time=5'b01000;  //pcount =1 --wtime=8

        5'b11111: wait_time=5'b01001;  //pcount =1 --wtime=9
```

```verilog
//default
        default: wait_time=5'b0000;

endcase
end


end
endfunction


assign wtime=wait_time(index,ef,ff,reset);
endmodule
```

Mini Prioject

module mini_project (clk, reset, Tcount, Pcount, empty_flag, full_flag,Hold, Wtime, inx , iny);

input clk, reset,inx,iny;

input [1:0] Tcount;

output [2:0] Pcount;

output empty_flag ,full_flag ;

output [4:0] Wtime;

output Hold;

wire pci , pco;

wire inx = 1;

wire iny = 1;

FSM x1 (.clk(clk), .rst(reset) , .in(inx) , .out(pci)); // for queue back sensor

FSM y1 (.clk(clk), .rst(reset) , .in(iny) , .out(pco)); // for queue forward sensor

counter st1 (.clk(clk), .rst(reset) , .pcount(Pcount) , .pci(pci) , .pco(pco) , .ef(empty_flag) , .ff(full_flag), .H(Hold));

wire [4:0] index;

assign index = {Tcount , Pcount};

```verilog
new_rom st2 (.index(index), .clk(clk) , .ef(empty_flag) , .ff(full_flag) , .reset(reset), .wtime(Wtime));


endmodule




module mini_project_test;


reg reset_t, inx_t, iny_t ;

reg [1:0] Tcount_t;

reg clk_t = 1;

wire empty_flag_t, full_flag_t;

wire [4:0] Wtime_t;

wire [2:0] Pcount_t;

wire Hold_t;

mini_project g0  (.clk(clk_t), .reset(reset_t) , .Tcount(Tcount_t) , .Pcount(Pcount_t),
.empty_flag(empty_flag_t), . full_flag( full_flag_t) , .Wtime(Wtime_t), .inx(inx_t), .iny(iny_t),
.Hold(Hold_t) );



initial

begin

forever begin
```

```verilog
clk_t=clk_t;

#10 clk_t <=~clk_t;

end

end


initial begin


reset_t=0;Tcount_t=2'b01;inx_t=1;iny_t=1; // 000

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);


#150 Tcount_t=2'b01;inx_t=0;iny_t=1; //001

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);


#150 Tcount_t=2'b01;inx_t=1;iny_t=1; //010

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);


#150 Tcount_t=2'b01;inx_t=1;iny_t=0; //001

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);
```

```verilog
#150 Tcount_t=2'b01;inx_t=1;iny_t=1; //000

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);



#150 Tcount_t=2'b10;inx_t=0;iny_t=1; //001

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);



#150 Tcount_t=2'b10;inx_t=1;iny_t=1; //010

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);



#150 Tcount_t=2'b10;inx_t=1;iny_t=0; //001

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);



#150 Tcount_t=2'b10;inx_t=1;iny_t=1; // 000

if ( Pcount_t<3'b001 && empty_flag_t==1 && Hold_t == 1  ) $display("there is no one to go out of the
queue");

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);



#150 Tcount_t=2'b10;inx_t=1;iny_t=0;//test no one in queue
```

if (Pcount_t<3'b001 && empty_flag_t==1 && Hold_t == 1) $display("there is no one to go out of the queue");

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is %b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);

#150 Tcount_t=2'b10;inx_t=0;iny_t=0; //001

if (Pcount_t<3'b001 && empty_flag_t==1 && Hold_t == 1) $display("there is no one to go out of the queue");

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is %b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);

#150 Tcount_t=2'b10;inx_t=1;iny_t=0; //010

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is %b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);

#150 Tcount_t=2'b10;inx_t=0;iny_t=0;

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is %b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);

```
#150 Tcount_t=2'b10;inx_t=1;iny_t=0;
```

```
$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);
```

```
$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);
```

```
#150 Tcount_t=2'b10;inx_t=0;iny_t=0;
```

```
$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);
```

```
$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);
```

```
#150 Tcount_t=2'b10;inx_t=1;iny_t=0;
```

```
$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);
```

```
$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);
```

```
#150 Tcount_t=2'b10;inx_t=0;iny_t=0; // before full queue
```

```
if ( Pcount_t<3'b001 && empty_flag_t==1 && Hold_t == 1  ) $display("there is no one to go out of the
queue");
```

```
else if ( Pcount_t>3'b110 && full_flag_t==1 && Hold_t == 1) $display("the queue is full");
```

```
$display("the wating time for the next person is %d and the empty flag is %b and the full flag is
%b",Wtime_t,empty_flag_t,full_flag_t);
```

```
$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);
```

```verilog
#150 Tcount_t=2'b10;inx_t=1;iny_t=0;// test full queue



if ( Pcount_t<3'b001 && empty_flag_t==1 && Hold_t == 1  ) $display("there is no one to go out of the queue");

else if ( Pcount_t==3'b111 && full_flag_t==1 && Hold_t == 1) $display("the queue is full");

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is %b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);



#150 Tcount_t=2'b10;inx_t=1;iny_t=1;// test full queue 2



if ( Pcount_t<3'b001 && empty_flag_t==1 && Hold_t == 1  ) $display("there is no one to go out of the queue");

else if (Pcount_t==3'b111 && full_flag_t==1 && Hold_t == 1) $display("the queue is full");

$display("the wating time for the next person is %d and the empty flag is %b and the full flag is %b",Wtime_t,empty_flag_t,full_flag_t);

$display("the Pcount is %b the Tcount is %b",Pcount_t,Tcount_t);




end



endmodule
```