7 BIT DIGITAL TO ANALOG CONVERTOR

MOHAMED MOHAIDEEN A - BANNARI AMMAN INSTITUTE OF TECHNOLOGY,ERODE

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Abstract

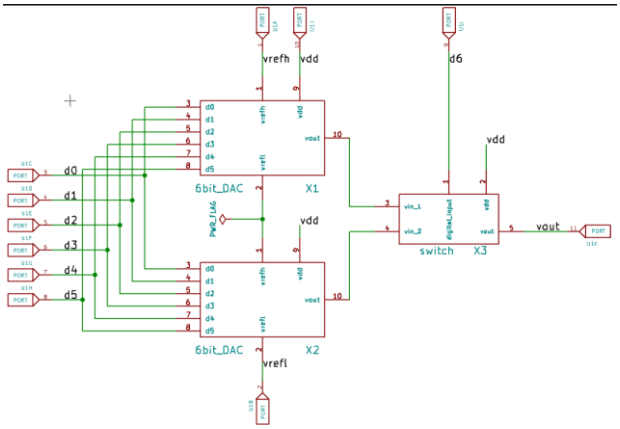
The application of time-interleaved structure leads to new amplitude and time errors while reducing many static and dynamic errors. In this case, both amplitude and time error are decreased by circuit structures integrated into a 7-bit DAC. In the present study, a new structure was proposed based on the randomization of two-interleaved paths in order to reduce the amplitude error, which can be extended to the N-channels-interleaved. In order to reduce the cycle-duty-error, a self-correction structure based on calculating the amplitude of the error before and measuring the time of this error along with the passage of the main signal through the output multiplexer is provided. The advantage of this method compared to the previous ones is that it does not require any calibration. This approach improves SFDR up to 37.8 dB at the 3 GHz signal bandwidth. The Post-Layout-Simulation for a 7-bit Hybrid-Time-Interleaved DAC confirmed the above. The performance of these converters depends on two types of static and dynamic errors. Static errors are created due to a mismatch between current sources or the output resistance of each current source, while dynamic errors are mostly caused by time errors in switching.

In other words, data switches do not operate at the right times,

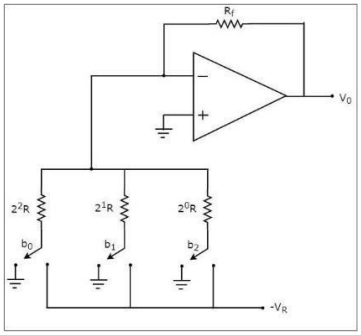
This 7-bit 16MS/s CMOS pipeline ADC for the application of ZigBee receiver. A 2.5bit/stage Multiplying DAC (MDAC) is designed to realize the pipeline ADC. Sample-and-hold amplifier (SHA)-less and operational trans conductance amplifier (OTA)-sharing technique is adopted to save power dissipation. Dynamic comparator can be chosen to reduce the power dissipation. Designed in a TSMC 0.18µm CMOS process, a power dissipation of only 3.7 mw from a 1.8-V supply is achieved. The area of ADC core is 0.65mm×0.38mm, the post-simulation shows that SNDR and SFDR are 40.9dB and 48.6dB, when sampling 3.015625MHz sinusoid input signal at 16MHz sampling clock.

Block diagram

7 BIT DAC



7bit digital top analog convertor block diagram



analog convertor block diagram

APPLICATION

- General Purpose Power Systems
- Telecom Systems
- Industrial applications

REFERENCE

A 10-bit 20 MS/s successive approximation register Analog-to-digital converter using single-sided DAC switching method for control application

In this paper 10-bit 20MS/s successive approximation register (SAR) Analog-to-digital converter (ADC) implemented in TSMC 0.18-um CMOS process is presented control application as a part of the biological signal acquisition system. By applying single-sided switching method that reduces DAC switching energy, the proposed SAR ADC achieves less power consumption

An N-bit DAC with adjustable Precision and Range

Now some special circuits need higher precision in relatively fixed range. While the precision of a common digital-to-Analog converter (DAC) is equidistant, which means the higher the precision is, the greater the number of bits. The increase of number of bits will slow down the speed of converter. This architecture we present here aims at finding a way of solving the problem

8-bit folding ADC based on switched capacitor

This paper presents an 8-bit folding Analog digital converter (ADC) using switched capacitors. In this architecture, the conversion is achieved when the signal crosses a determined voltage level and at this time, a voltage value is added or subtracted from the Analog input signal. The ADC proposed consists of eight identical stages that perform the conversion of one bit at a time