**Name :** Mohamed Mohamed ramadan

**B.N:** 790

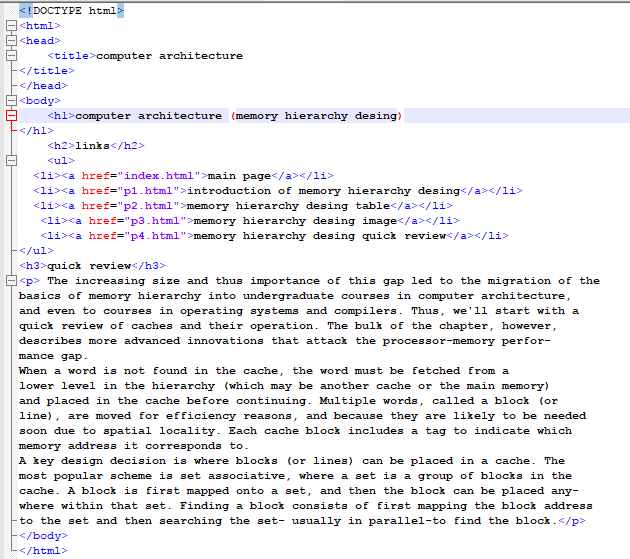
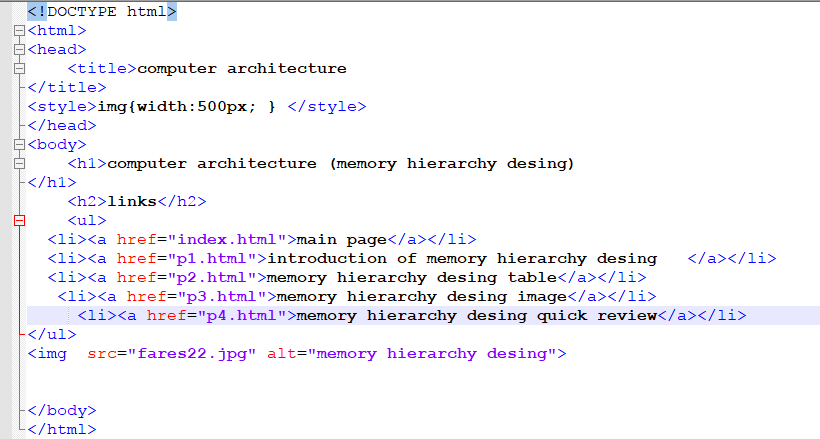
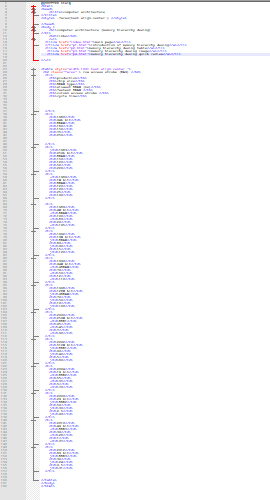
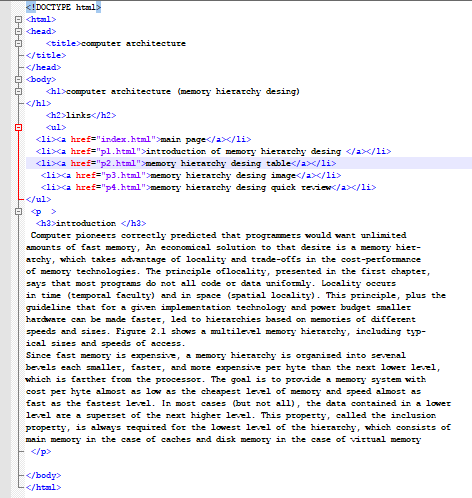
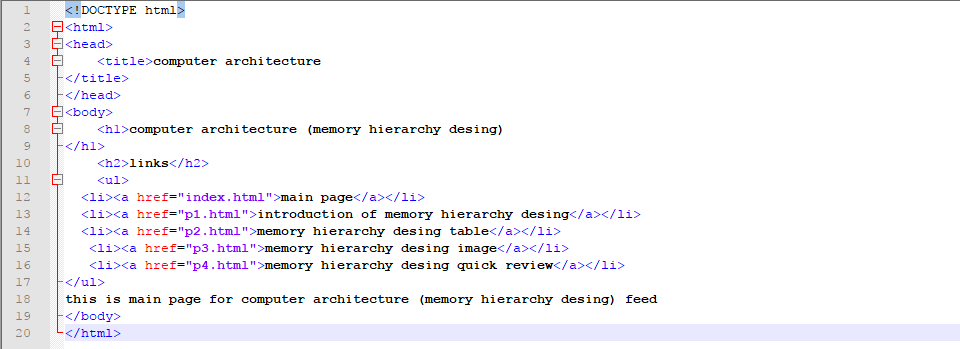
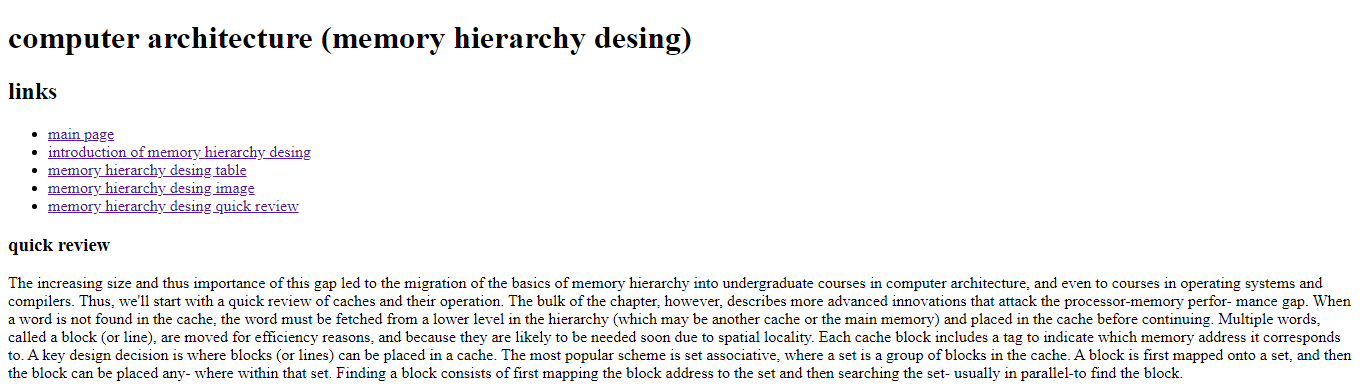
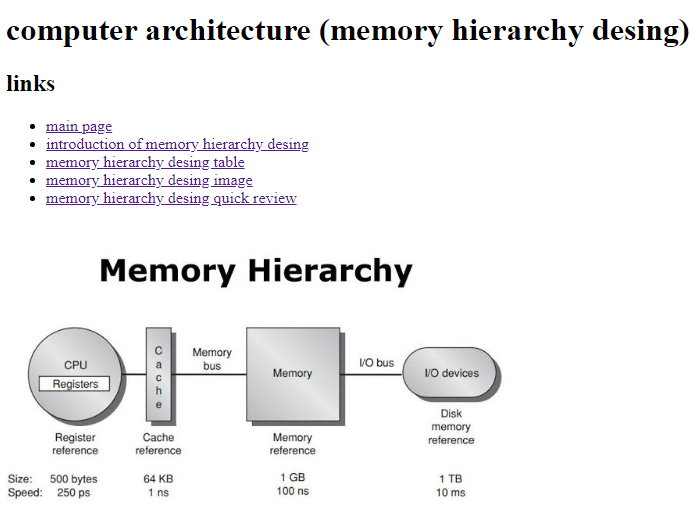
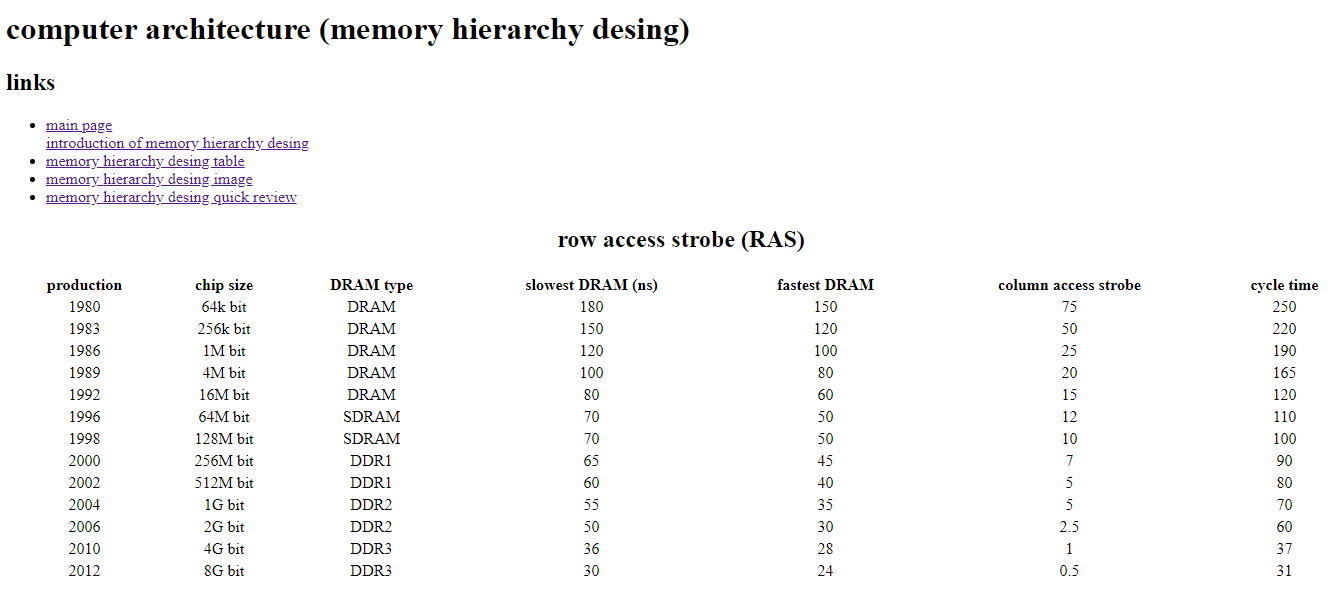
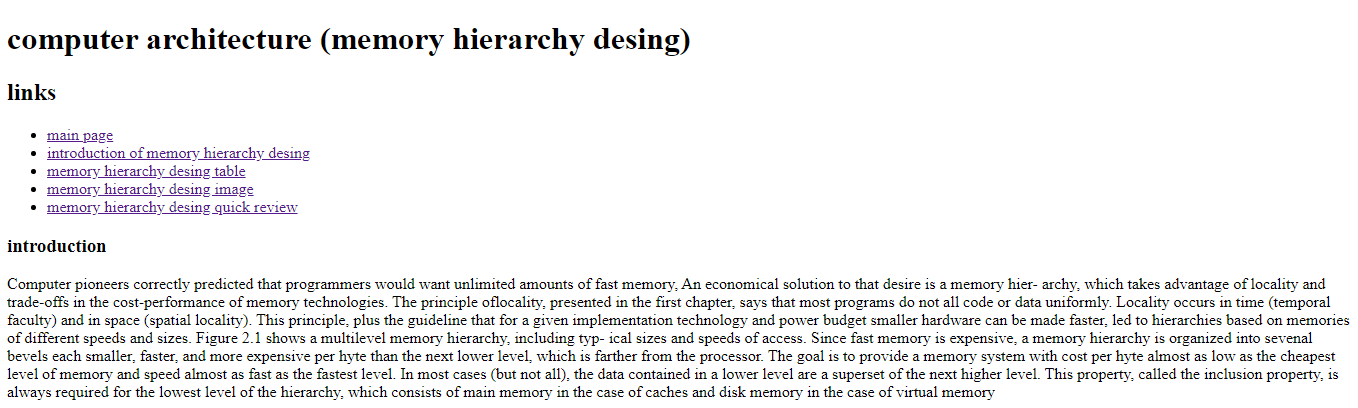
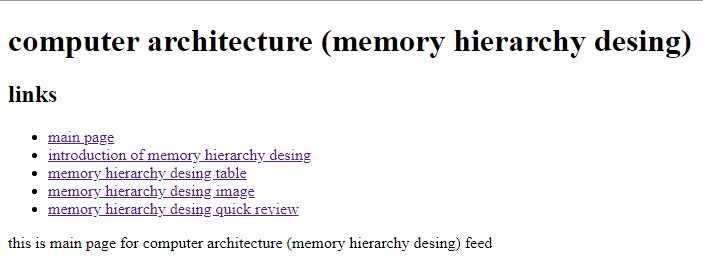
**Date :** 30/5/2020

**Topic:** computer architecture (memory hierarchy desing)

**Github link :** <https://github.com/mohamedmohamedramdan/html>

**Github page :** <https://mohamedmohamedramdan.github.io/html/>

**Application brief** : We investigate the implementation of IP look-up for core routers using multiple microengines and a tailored memory hierarchy. The main architectural concerns are limiting thenumber of and contention for memory accesses.Using a level compressed trie as an index, we show the impact of the main parameter, the root branching factor, on the memory capacity and number of memory accesses. Despite the lack of locality, we show how a cache can reduce the required memory capacity and limit the amount of expensive multibanking. Results of simulation experiments using contemporary routing tables show that the architecture scales well, at least up to 16 processors, and that thepresence of a small on-chip cache increases throughput significantly, up to 65% over an architecture with the same number of processors but without a cache, all while reducing the amount of required off-chip memory.

**Screeshots :**