

“Digital IC Design Diploma”

## **Project 2**

Under supervision of:

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Submitted by:

| <b>Members</b>                 | <b>Group</b> |
|--------------------------------|--------------|
| Mohamed Ossama Mohamed Mostafa | 2            |

## ➤ RTL Code:

### ○ Synchronous Ram Code:

```
F: > Family > Hamada > Digital design diploma kareem wasem > Project > testproj2 > RAM.v > RAM
 1  module RAM #(parameter MEM_DEPTH = 256 , parameter ADDR_SIZE = 8)
 2  (
 3      input  wire [9:0]   din,
 4      input  wire          rx_valid,
 5      input  wire          clk,
 6      input  wire          rst_n,
 7      output reg [7:0]    dout,
 8      output reg          tx_valid
 9  );
10  reg [7:0] mem [MEM_DEPTH-1:0];
11  reg [ADDR_SIZE-1:0] addr;
12  always @(posedge clk)
13  begin
14      if(~rst_n)
15      begin
16          dout <= 8'b0;
17          tx_valid <= 1'b0;
18          addr <= 'b0;
19      end
20      else
21      begin
22          if (rx_valid)
23          begin
24              case(din[9:8])
25                  2'b00: // Write Address
26                  begin
27                      addr <= din[7:0];
28                      tx_valid <= 1'b0;
29                  end
30                  2'b01: // Write Data
31                  begin
32                      mem[addr] <= din[7:0];
33                      tx_valid <= 1'b0;
34                  end
35                  2'b10: // Read Address
36                  begin
37                      addr <= din[7:0];
38                      tx_valid <= 1'b0;
39                  end
40                  2'b11: // Read Data
41                  begin
42                      dout <= mem[addr];
43                      tx_valid <= 1'b1;
44                  end
45              endcase
46          end
47      end
48  end
49 endmodule
```

## o SPI Code

```

F: > Family > Hamada > Digital design diploma kareem wasem > Project > proj2 > SPI.v > SPI
 1  module SPI
 2  (
 3      input  wire      MOSI,
 4      input  wire      ss_n,
 5      input  wire      clk,
 6      input  wire      rst_n,
 7      input  wire [7:0]  tx_data,
 8      input  wire      tx_valid,
 9      output reg       MISO,
10      output reg [9:0] rx_data,
11      output reg       rx_valid
12  );
13  reg      flag_add;
14  reg [3:0] counter1;
15  reg [3:0] counter2;
16  (* fsm_encoding = "one_hot" *)
17  reg [2:0] current_state,next_state;
18  parameter IDLE = 3'b000;
19  parameter CHK_CMD = 3'b001;
20  parameter WRITE = 3'b011;
21  parameter READ_ADD = 3'b101;
22  parameter READ_DATA = 3'b111;
23 // State Memory Logic
24  always @(posedge clk)
25 begin
26     if(~rst_n)
27     |   current_state <= IDLE;
28     else
29     |   current_state <= next_state;
30 end
31 // Next State Logic
32 always@(*)
33 begin
34     case (current_state)
35     IDLE:
36     begin
37         if(~ss_n)
38             current_state <= next_state;
39     end
40     // Next State Logic
41     always@(*)
42     begin
43         case (current_state)
44         IDLE:
45         begin
46             if(~ss_n)
47                 next_state = CHK_CMD;
48             else
49                 next_state = IDLE;
50         end
51         CHK_CMD:
52         begin
53             if(~MOSI && !ss_n)
54                 next_state = WRITE ;
55             else if( MOSI && !ss_n && flag_add) // flag addres to distinguish between Read addr and Read Data state
56                 next_state = READ_ADD;
57             else if( MOSI && !ss_n && !flag_add)
58                 next_state = READ_DATA;
59             else
60                 next_state = IDLE;
61         end
62         WRITE:
63         begin
64             if(~ss_n)
65                 next_state = WRITE;
66             else
67                 next_state = IDLE;
68         end
69     end
70 
```

```

1 module S7_1
2
3   begin
4     next_state = IDLE;
5   end
6   READ_ADD:
7   begin
8     if(~ss_n)
9       next_state = READ_ADD;
10    else
11      next_state = IDLE;
12   end
13   READ_DATA:
14   begin
15     if(~ss_n)
16       next_state = READ_DATA;
17     else
18       next_state = IDLE;
19   end
20   default: next_state = IDLE;
21   endcase
22 end
23 // output logic
24 always@(posedge clk)
25 begin
26   if(~rst_n)
27   begin
28     rx_data <= 10'b0;
29     rx_valid <= 1'b0;
30     MISO <= 1'b0;
31     counter1<=4'b0;
32     counter2<=4'b1000;
33     flag_add <= 1'b1;
34   end
35   else
36   begin
37     case(current_state)
38       IDLE:
39         begin
40           rx_data <= 10'b0;
41           rx_valid <= 1'b0;
42           MISO <= 1'b0;
43         end
44       CHK_CMD:
45         begin
46           rx_data <= 10'b0;
47           rx_valid <= 1'b0;
48           MISO <= 1'b0;
49         end
50       WRITE:
51         begin
52           if(counter1 < 4'b1010)
53             begin
54               rx_valid <= 1'b0;
55               rx_data <= {rx_data[8:0],MOSI};
56               counter1 <= counter1 + 1;
57             end
58           if(counter1 == 4'b1010)
59             begin
60               rx_valid <= 1'b1;
61               MISO <= 1'b0;
62               counter1 <= 4'b0;
63             end
64           end
65         end
66       end
67     end
68   end
69   end
70   end
71   end
72   end
73   end
74   end
75   end
76   end
77   end
78   end
79   end
80   end
81   end
82   end
83   end
84   end
85   end
86   end
87   end
88   end
89   end
90   end
91   end
92   end
93   end
94   end
95   end
96   end
97   end
98   end
99   end
100  end
101  end
102  end
103  end
104  end
105  end
106  end
107  end
108  end
109  end
110  end
111  end
112  end
113  end
114  end
115  end
116  end
117  end
118  end
119  end
120  end
121  end

```

```

120      end
121  end
122  READ_ADD: // Mem Read Address to send Data to SPI
123  begin
124      if(counter1 < 4'b1010)
125      begin
126          rx_valid <= 1'b0;
127          rx_data <= {rx_data[8:0],MOSI};
128          counter1 <= counter1 + 1;
129      end
130      if(counter1 == 4'b1010)
131      begin
132          rx_valid <= 1'b1;
133          MISO <= 1'b0;
134          counter1 <= 4'b0;
135          flag_add <= 1'b0;
136      end
137  end
138
139  end
140  READ_DATA:
141  begin
142      if (counter1 < 4'b1010)
143      begin
144          rx_valid <= 1'b0;
145          rx_data <= {rx_data[8:0],MOSI};
146          counter1 <= counter1 + 1;
147      end
148      if(counter1 == 4'b1001)
149      begin
150          rx_valid <= 1'b1;
151          MISO <= 1'b0;
152          counter1 <= 4'b0;
153      end
154      if (tx_valid && counter2 > 4'b0)
155      begin
156          MISO <= tx_data[counter2-1];
157          counter2 <= counter2 - 1 ;
158      end
159      if(counter2 == 4'b0)
160      begin
161          counter2 <= 4'b1000;
162          flag_add <= 1'b1;
163      end
164  end
165 end
166 endmodule

```

- o SPI Wrapper Code:

```
F: > Family > Hamada > Digital design diploma kareem wasem > Project > testproj2 > SPIWrapper.v > SPIWrapper
 1 module SPIWrapper
 2 (
 3     input wire MOSI,
 4     input wire SS_n,
 5     input wire clk,
 6     input wire rst_n,
 7     output wire MISO
 8
 9 );
10 parameter MEM_DEPTH = 256;
11 parameter ADDR_SIZE = 8;
12 wire [9:0] rx_dataaa;
13 wire rx_validd;
14 wire [7:0] tx_dataaa;
15 wire tx_validd;
16 SPI SPIbLock
17 (
18     .MOSI(MOSI),
19     .SS_n(SS_n),
20     .clk(clk),
21     .rst_n(rst_n),
22     .tx_data(tx_dataaa),
23     .tx_valid(tx_validd),
24     .MISO(MISO),
25     .rx_data(rx_dataaa),
26     .rx_valid(rx_validd)
27 );
28 RAM #(.MEM_DEPTH(MEM_DEPTH),.ADDR_SIZE(ADDR_SIZE)) RAMblock
29 (
30     .din(rx_dataaa),
31     .rx_valid(rx_validd),
32     .clk(clk),
33     .rst_n(rst_n),
34     .dout(tx_dataaa),
35     .tx_valid(tx_validd)
36 );
37 endmodule
```

- o Do File

```
F: > Family > Hamada > Digital design diploma kareem wasem > Project > testproj2 > run.do
 1 vlib work
 2 vlog RAM.v SPI.v SPIWrapper.v SPI_tb.v
 3 vsim -voptargs=+acc work.SPI_tb
 4 add wave *
 5 add wave -position insertpoint \
 6 sim:/SPI_tb/DUT/SPIbLock/tx_data \
 7 sim:/SPI_tb/DUT/SPIbLock/tx_valid \
 8 sim:/SPI_tb/DUT/SPIbLock/rx_data \
 9 sim:/SPI_tb/DUT/SPIbLock/rx_valid \
10 sim:/SPI_tb/DUT/SPIbLock/current_state \
11 sim:/SPI_tb/DUT/SPIbLock/next_state
12 add wave -position insertpoint \
13 sim:/SPI_tb/DUT/RAMblock/mem \
14 sim:/SPI_tb/DUT/RAMblock/addr
15 add wave -position insertpoint \
16 sim:/SPI_tb/DUT/SPIbLock/counter1
17 add wave -position insertpoint \
18 sim:/SPI_tb/DUT/SPIbLock/counter2
19 add wave -position insertpoint \
20 sim:/SPI_tb/DUT/RAMblock/din
21 add wave -position insertpoint \
22 sim:/SPI_tb/DUT/RAMblock/dout
23 run -all
24 #quit -sim
```

- Testbench

```
F: > Family > Hamada > Digital design diploma kareem wasem > Project > testproj2 > SPI_tb.v > SPI_tb
 1  module SPI_tb();
 2  ////////////////////////////////////////////////////////////////// Testbench Signals //////////////////////////////////////////////////////////////////
 3  reg    MOSI_tb;
 4  reg    SS_n_tb;
 5  reg    clk_tb;
 6  reg    rst_n_tb;
 7  wire   MISO_tb;
 8  integer i;
 9  ////////////////////////////////////////////////////////////////// Module Instantiation //////////////////////////////////////////////////////////////////
10 SPIWrapper DUT
11 (
12     .MOSI(MOSI_tb),
13     .SS_n(SS_n_tb),
14     .clk(clk_tb),
15     .rst_n(rst_n_tb),
16     .MISO(MISO_tb)
17 );
18 ////////////////////////////////////////////////////////////////// Clock Generator //////////////////////////////////////////////////////////////////
19 initial
20 begin
21     clk_tb = 0;
22     forever
23         #5 clk_tb = ~clk_tb;
24 end
25 ////////////////////////////////////////////////////////////////// Stimulus and Response Initial Block //////////////////////////////////////////////////////////////////
26 initial
27 begin
28     $readmemb("mem.dat",DUT.RAMblock.mem);
29
30     RstCheck();
31     ////////////////////////////////////////////////////////////////// 1. Write Address //////////////////////////////////////////////////////////////////
32     Startcomm();
33     state(0);
34     sendData(10'b00_0001_1100); //Address = 'h1c
35     Endcomm();
36     ////////////////////////////////////////////////////////////////// 1. Send Data //////////////////////////////////////////////////////////////////
37     Startcomm();
```

```
36     ////////////////////////////////////////////////////////////////// 1. Send Data //////////////////////////////////////////////////////////////////
37     Startcomm();
38     state(0);
39     sendData(10'b01_1010_1111); //Data = 'haf
40     Endcomm();
41
42     ////////////////////////////////////////////////////////////////// 1. Read Address //////////////////////////////////////////////////////////////////
43     Startcomm();
44     state(1);
45     sendData(10'b10_0001_1100); //Data af address = 'h1c
46     Endcomm();
47     ////////////////////////////////////////////////////////////////// 1. Read Data //////////////////////////////////////////////////////////////////
48     Startcomm();
49     state(1);
50     sendData(10'b11_1010_0011); //read Data af address 1c
51     repeat(9)@ (negedge clk_tb);
52     Endcomm();
53     ////////////////////////////////////////////////////////////////// 2. Write Address //////////////////////////////////////////////////////////////////
54     Startcomm();
55     state(0);
56     sendData(10'b00_0111_1100); //Address = 'h7c
57     Endcomm();
58
59     ////////////////////////////////////////////////////////////////// 2. Send Data //////////////////////////////////////////////////////////////////
60     Startcomm();
61     state(0);
62     sendData(10'b01_1110_1001); //Data = 'he9
63     Endcomm();
64     ////////////////////////////////////////////////////////////////// 2. Read Address //////////////////////////////////////////////////////////////////
65     Startcomm();
66     state(1);
67     sendData(10'b10_0111_1100); //Data of address = 'h7c
68     Endcomm();
69
70     ////////////////////////////////////////////////////////////////// 2. Read Data //////////////////////////////////////////////////////////////////
71     Startcomm();
72     state(1);
```

```

69   /////////////////////////////// 2. Read Data ///////////////////////
70   Startcomm();
71   state(1);
72   sendData(10'b11_1010_1111); //read Data af address = 'h7c
73   repeat(9)@(negedge clk_tb);
74   Endcomm();
75   /////////////////////////////// 3. write Adress /////////////////////
76   Startcomm();
77   state(0);
78   sendData(10'b00_0110_0010); //Address = 'h62
79   Endcomm();
80
81   /////////////////////////////// 3.Send Data ///////////////////////
82   Startcomm();
83   state(0);
84   sendData(10'b01_1100_1010); //Data = 'hca
85   Endcomm();
86   /////////////////////////////// 3.Read Address /////////////////////
87   Startcomm();
88   state(1);
89   sendData(10'b10_0110_0010); //Data af address = 'h62
90   Endcomm();
91   /////////////////////////////// 3.Read Data /////////////////////
92   Startcomm();
93   state(1);
94   sendData(10'b11_1000_1011); //read Data af address ='h62
95   repeat(9)@(negedge clk_tb);
96   Endcomm();
97
98 $stop;
99 end
100

```

```

55   end
100 ////////////////// Start Of Communication Task ///////////////////
101 task Startcomm();
102 begin
103   ss_n_tb = 0;
104   @(negedge clk_tb);
105 end
106 endtask
107 ////////////////// End Of communication Task ///////////////////
108 task Endcomm();
109 begin
110   ss_n_tb = 1;
111   @(negedge clk_tb);
112 end
113 endtask
114 ////////////////// Determine Read or Write Task //////////////////
115 task state(input z);
116 begin
117   MOSI_tb = z;
118   @(negedge clk_tb);
119 end
120 endtask
121 ////////////////// Reset Check Task /////////////////////
122 task RstCheck();
123 begin
124   ss_n_tb = 1'b1;
125   MOSI_tb = 1'b0;
126   rst_n_tb = 1'b0;
127   @(negedge clk_tb);
128   rst_n_tb = 1'b1;
129 end
130 endtask
131

```

```

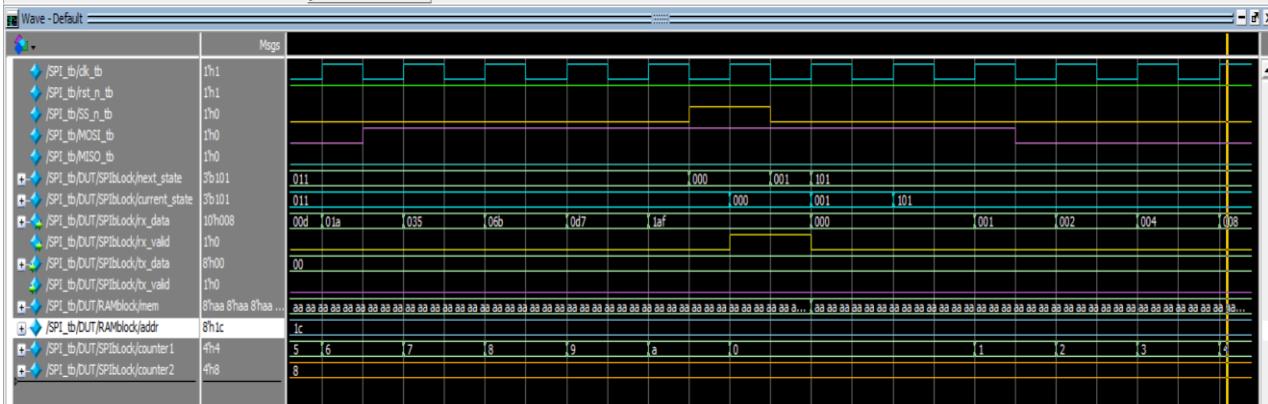
130    end
131  endtask
132 //////////////// Send Data Task ///////////////////
133 task sendData(input [9:0] temp);
134 begin
135   for(i=10;i>0;i=i-1) begin
136     MOSI_tb = temp[i-1];
137     @(negedge clk_tb);
138   end
139 end
140 endtask
141 endmodule

```

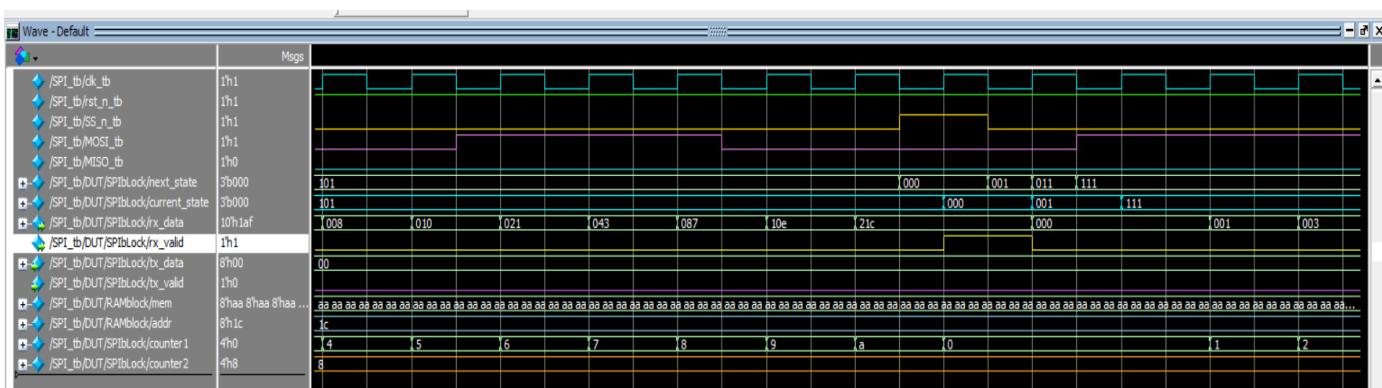
- Waveforms Snippets
  - Write at Address = 'h1c



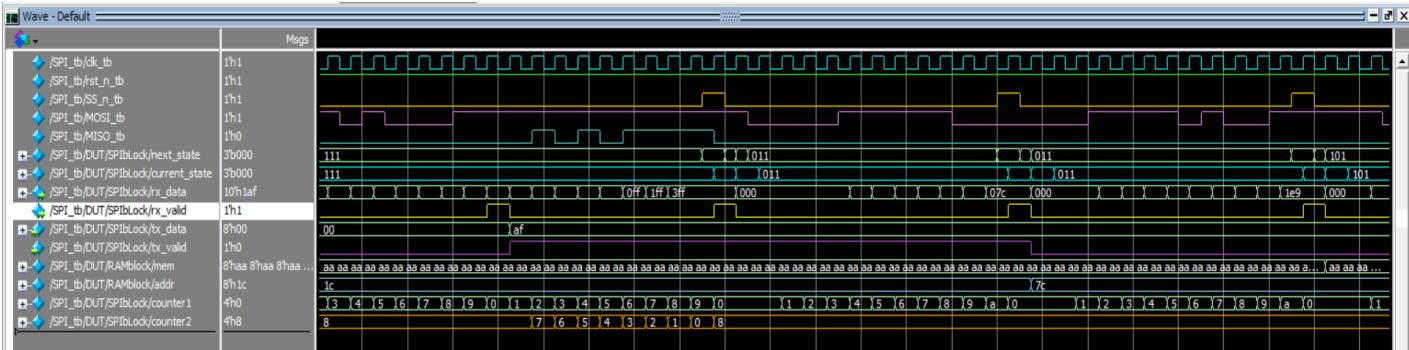
- Write Data = 8'h af



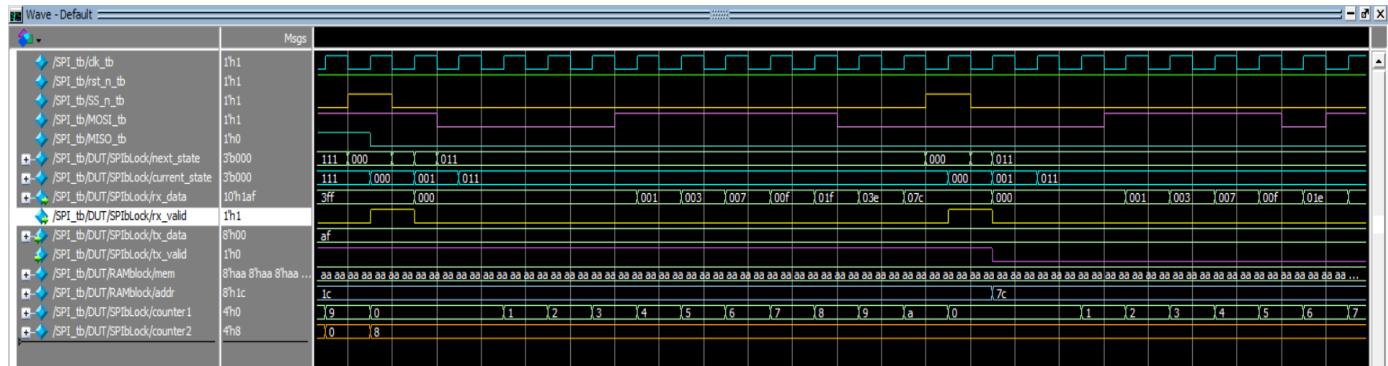
- Read Address = 'h1c



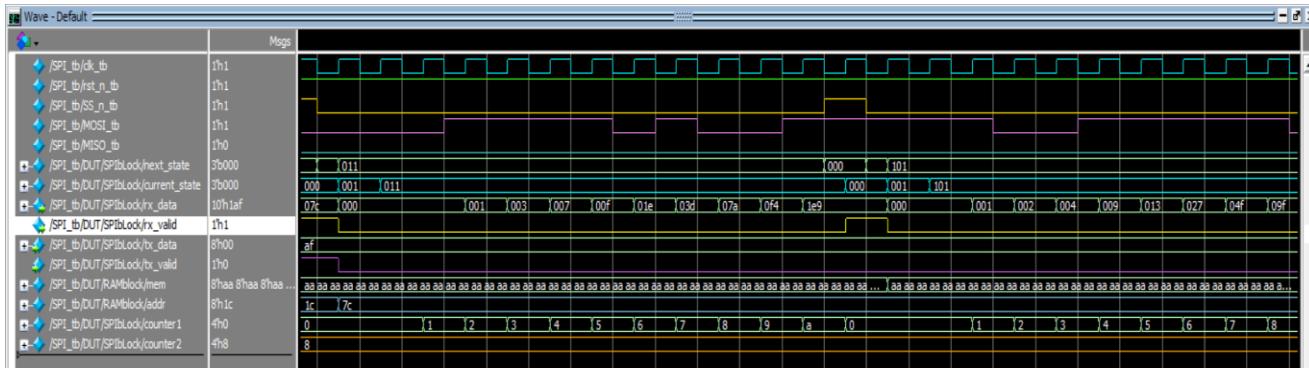
- Read Data = 8'haf from Address = 'h1c



- Write At Address = 'h7c



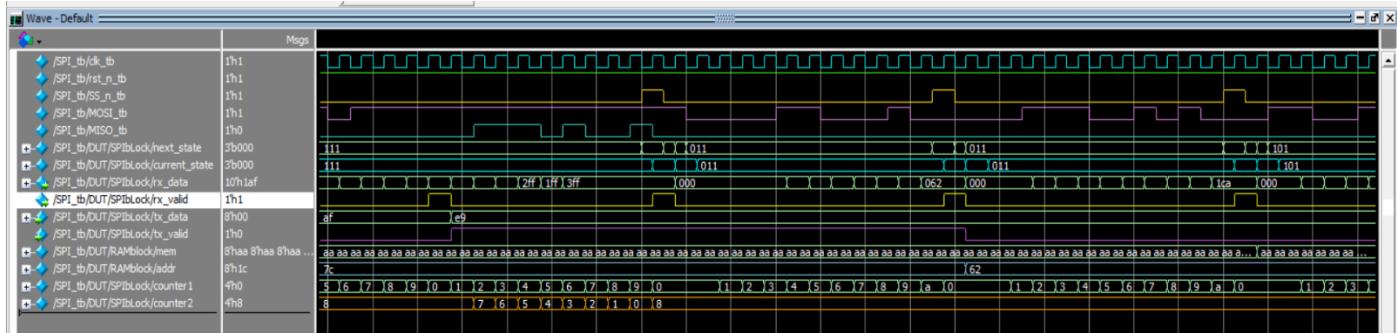
- Write Data = 'he9 at address = 'h7c



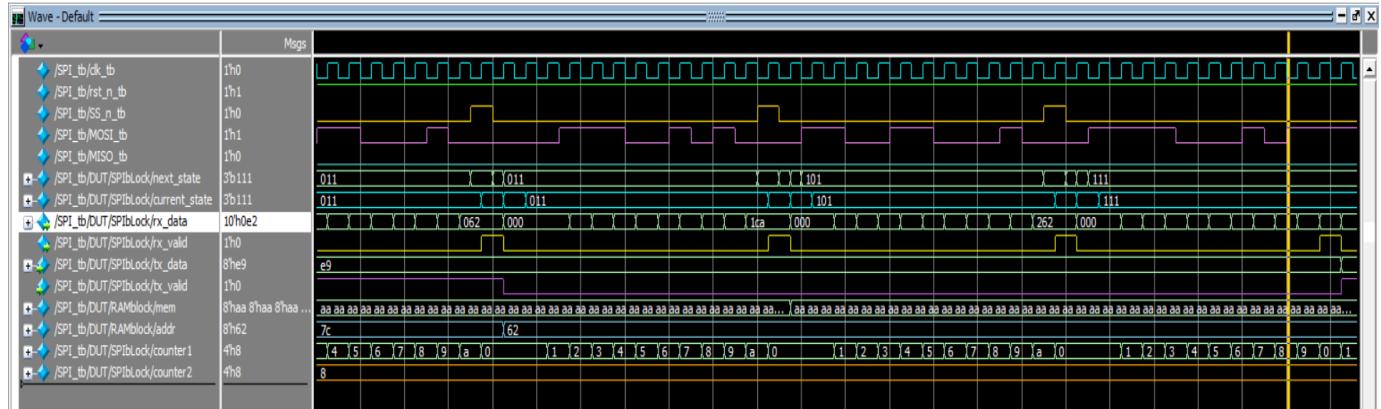
- Read Address = 'h7c



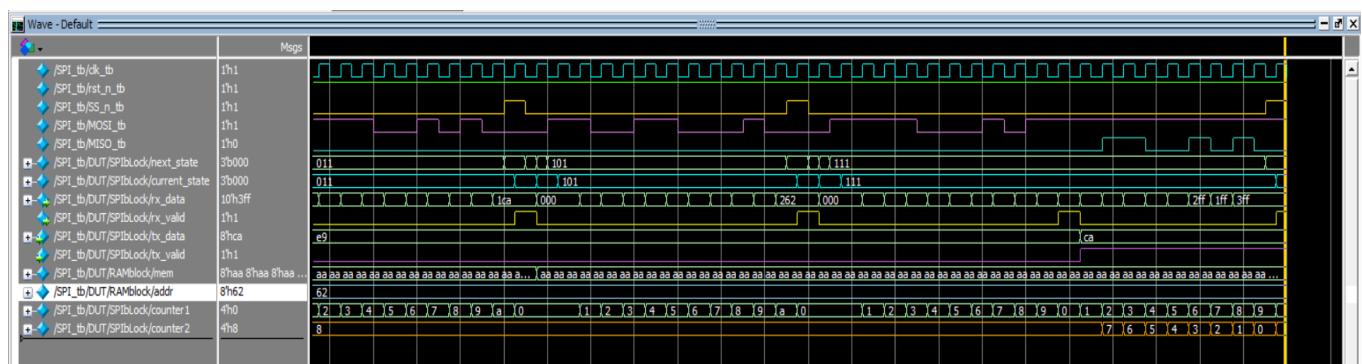
- Read Data = 'he9 from Address = 'h7c



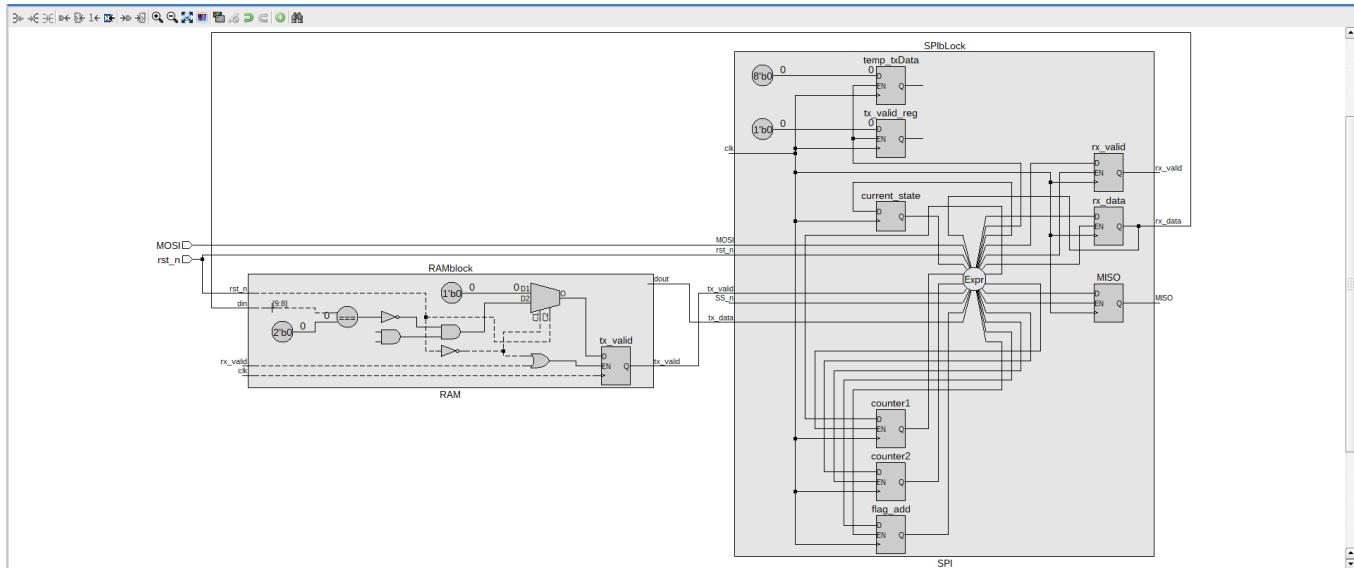
- Write at address = 'h62 and data = 'hca



- Read Address = 'h62 and Read data = 'hca



- Lint Tool:



```
=====
2 Lint Check Report
3 Questa Lint Version 2021.1 4558100 win64 28-Jan-2021
4
5 Timestamp : Tue Aug 5 01:05:56 2025
6 Description : Report for referring checks count, check violations details, and design information
7 Design : SPIWrapper
8 Database : F:/Family/Hamada/LintTool/Proj2Final/lint.db
9 Design Quality Score : 99.1%
10
11 Sections:
12   Section 1 : Check Summary
13   Section 2 : Check Details
14   Section 3 : Design Information
15 =====
16
17
18 =====
19 Section 1 : Check Summary
20 =====
21 | Error (0) |
22 -----
23
24 -----
25 | Warning (4) |
26 -----
27 seq_block_has_duplicate_assign : 4
28
29 | Info (3) |
30 -----
31 parameter_name_duplicate : 2
32 always_signal_assign_large : 1
33
34 -----
35 | Resolved (0) |
36
37 -----
38
39
40 =====
41 Section 2 : Check Details
42 =====
43
44 | Error (0) |
45 -----
46
47
48 -----
49 | Warning (4) |
50 -----
51
52 Check: seq_block_has_duplicate_assign [Category: Rtl Design Style] (4)
53   [Message: Signal is assigned more than once in a sequential block. Signal '<signal>', Module '<module>', File '<file>', Total Assigns Count '<count>', First Assign at Line '<line>', Second Assign at Line '<line>'.]
54
55 seq_block_has_duplicate_assign: [uninspected] Signal is assigned more than once in a sequential block. Signal 'rx_valid', Module 'SPI', File 'F:/Family/Hamada/LintTool/Proj2Final/SPI.V', Total Assigns Count '2', First Assign at Line '10', Second Assign at Line '11'
56
```

- Synthesis
  - One Hot Encoding

```

6 # Process ID: 4976
7 # Current directory: F:/Family/SynthesisKareemWasseemTasks/Projj2Finaaaal/project_2/project_2.runs/synth_1
8 # Command line: vivado.exe -log SPIWrapper.vds -product Vivado -mode batch -messageDb vivado.pb -notrace -source SPIWrapper.tcl
9 # Log file: F:/Family/SynthesisKareemWasseemTasks/Projj2Finaaaal/project_2/project_2.runs/synth_1/SPIWrapper.vds
10 # Journal file: F:/Family/SynthesisKareemWasseemTasks/Projj2Finaaaal/project_2/project_2.runs/synth_1/vivado.jou
11 -----
12 source SPIWrapper.tcl -notrace
13 Command: synth_design -top SPIWrapper -part xc7a35tictcg236-1L
14 Starting synth_design
15 Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35ti'
16 INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
17 INFO: Launching helper process for spawning children vivado processes
18 INFO: Helper process launched with PID 17712
19 -----
20 Starting RTL Elaboration : Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 354.664 ; gain = 98.613
21 -----
22 INFO: [Synth 8-6157] synthesizing module 'SPIWrapper' [F:/Family/SynthesisKareemWasseemTasks/Projj2Finaaaal/SPIWrapper.v:1]
23     Parameter MEM_DEPTH bound to: 256 - type: integer
24     Parameter ADDR_SIZE bound to: 8 - type: integer
25 INFO: [Synth 8-6157] synthesizing module 'SPI' [F:/Family/SynthesisKareemWasseemTasks/Projj2Finaaaal/SPI.v:1]
26     Parameter IDLE bound to: 3'b000
27     Parameter CHK_CMD bound to: 3'b001
28     Parameter WRITE bound to: 3'b011
29     Parameter READ_ADD bound to: 3'b101
30     Parameter READ_DATA bound to: 3'b111
31 INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [F:/Family/SynthesisKareemWasseemTasks/Projj2Finaaaal/SPI.v:17]
32 INFO: [Synth 8-155] case statement is not full and has no default [F:/Family/SynthesisKareemWasseemTasks/Projj2Finaaaal/SPI.v:91]
33 INFO: [Synth 8-6155] done synthesizing module 'SPI' (1#) [F:/Family/SynthesisKareemWasseemTasks/Projj2Finaaaal/SPI.v:1]
34 INFO: [Synth 8-6157] synthesizing module 'RAM' [F:/Family/SynthesisKareemWasseemTasks/Projj2Finaaaal/RAM.v:1]
35     Parameter MEM_DEPTH bound to: 256 - type: integer
36     Parameter ADDR_SIZE bound to: 8 - type: integer

```

Activate Windows

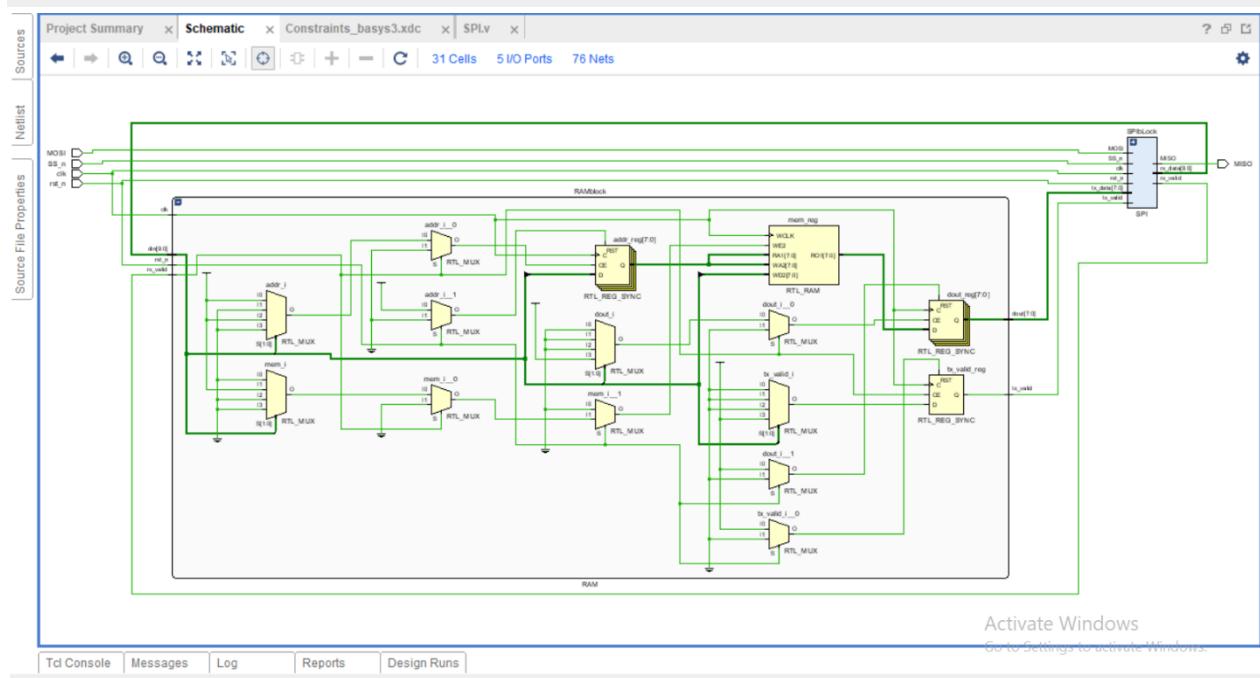
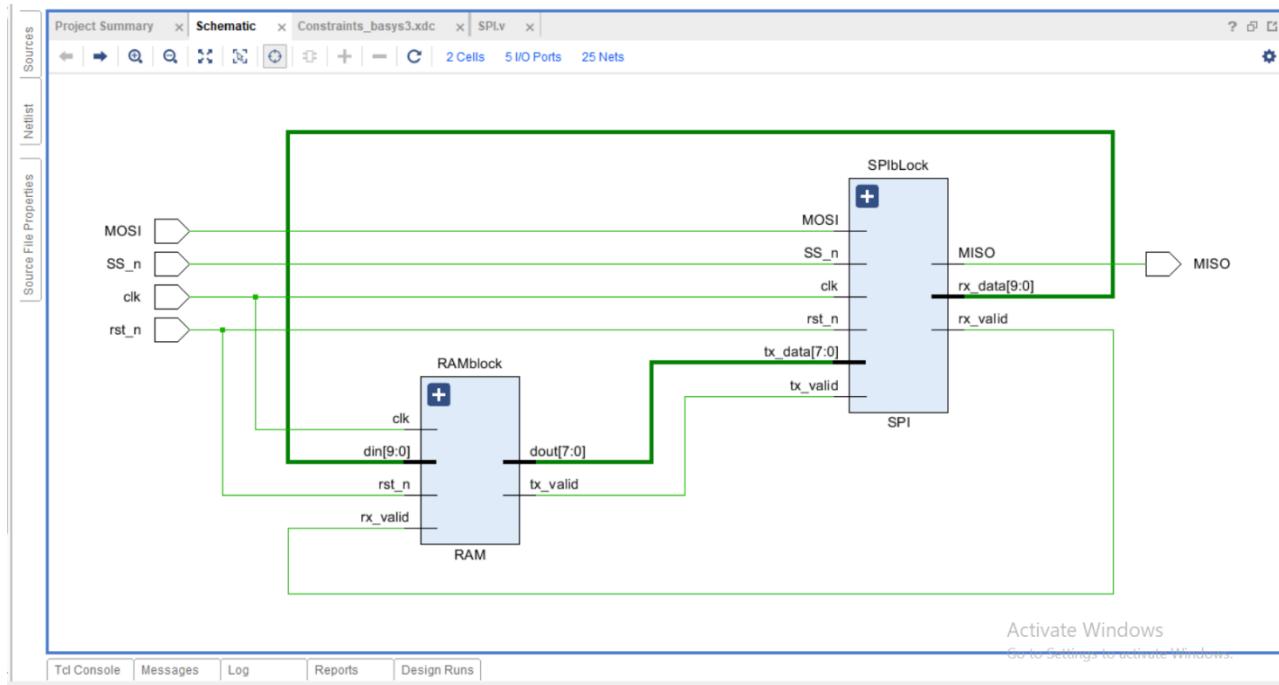
| State     | New Encoding | Previous Encoding |
|-----------|--------------|-------------------|
| IDLE      | 00001        | 000               |
| CHK_CMD   | 00010        | 001               |
| WRITE     | 00100        | 011               |
| READ_ADD  | 01000        | 101               |
| READ_DATA | 10000        | 111               |

INFO: [Synth 8-3354] encoded FSM with state register 'current\_state\_reg' using encoding 'one-hot' in module 'SPI'

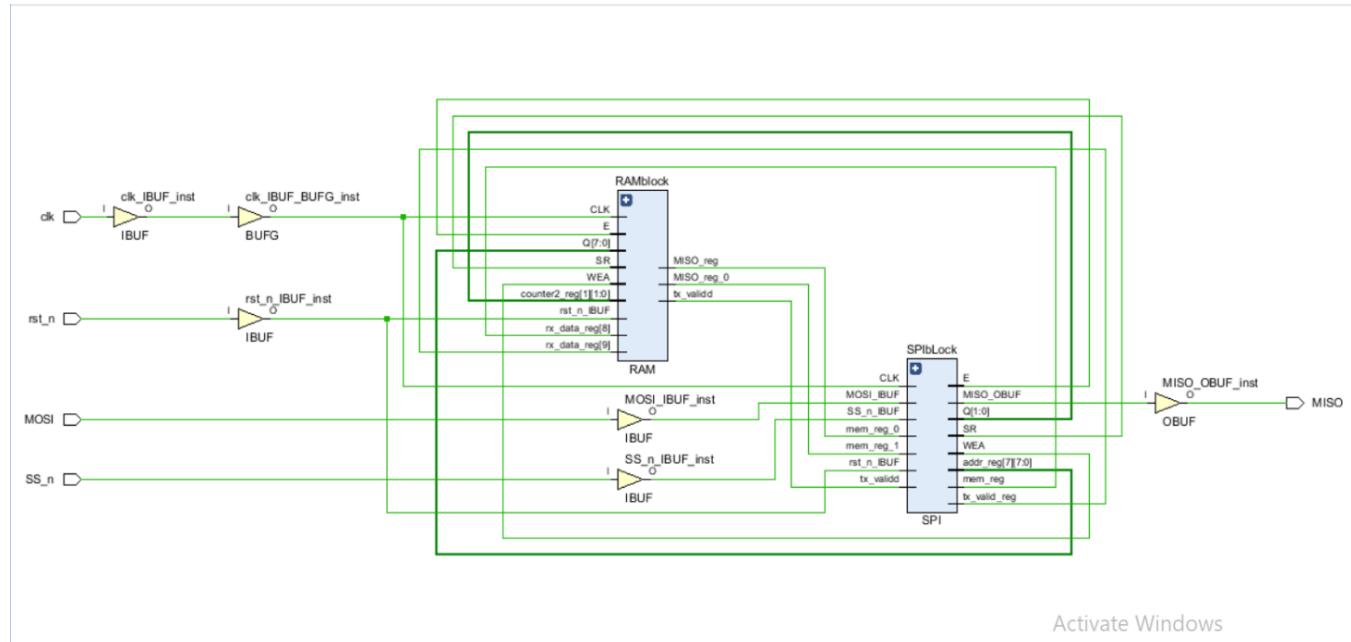
- Message After Elaboration

Activate Windows  
Go to Settings to activate Windows.

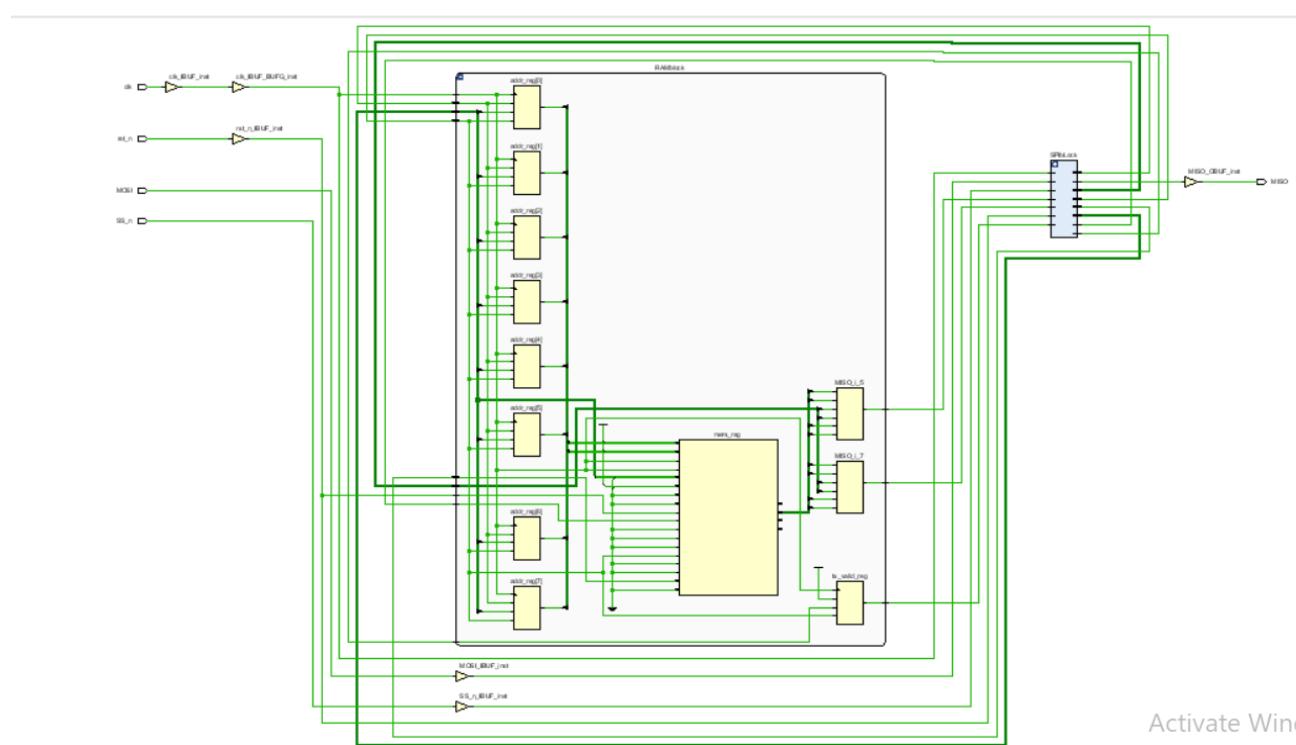
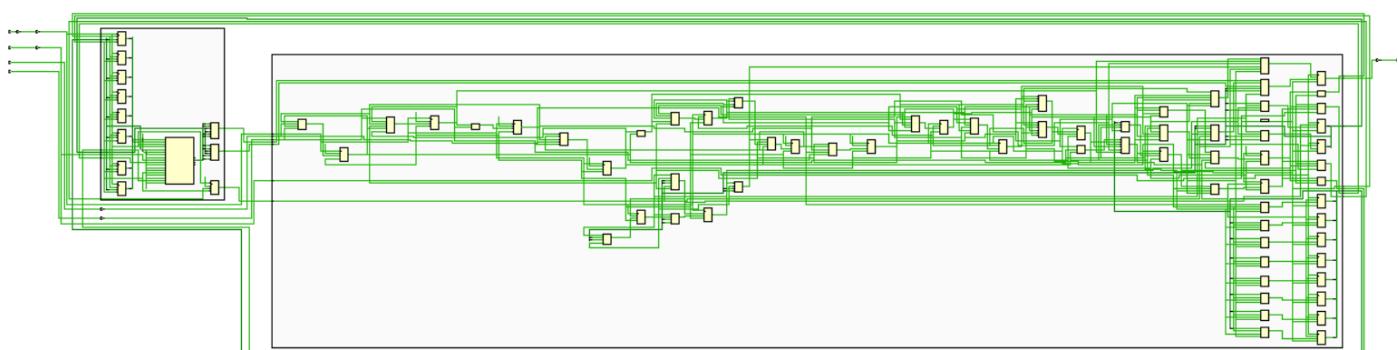
## ○ Elaborated Schematic



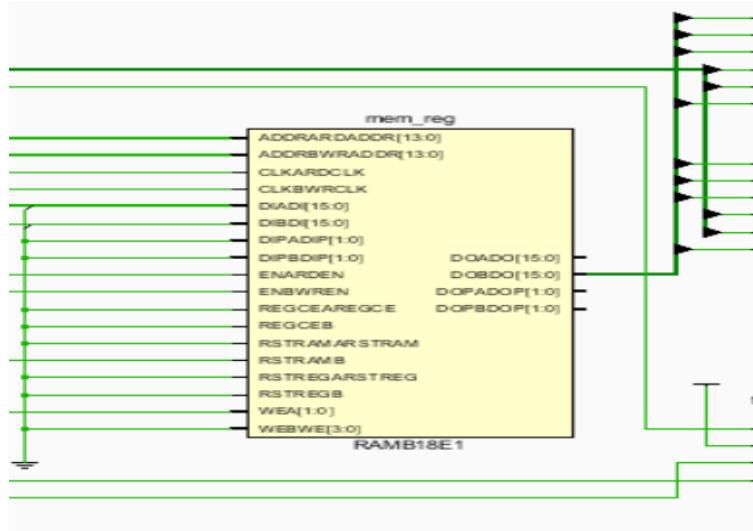
## ○ Synthesis Schematic



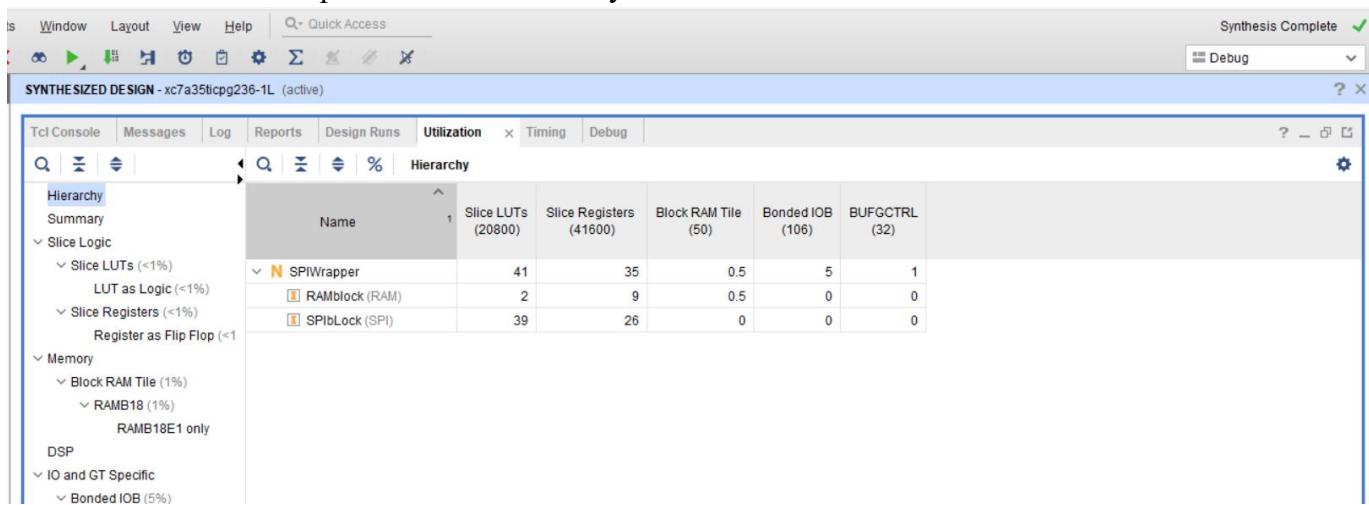
Activate Windows



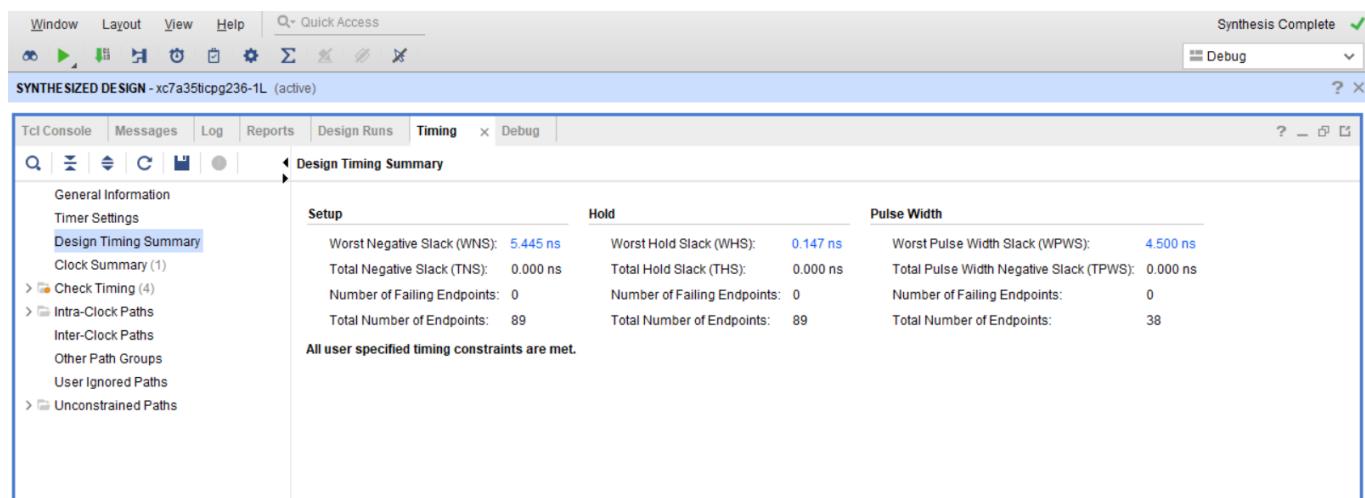
Activate Wind  
Page 15 | Page



- o Report Utilization after Synthesis



- o Timing Report after Synthesis



- Highest Delay Path

SYNTHESIZED DESIGN - xc7a35tcpg236-1L (active)

**Schematic** x Constraints\_basys3.xdc x SPI.v x SPIWrapper.v x

Path Properties

Path 1

| Name       | Path 1 |
|------------|--------|
| General    |        |
| Properties |        |
| Report     |        |
| Cells      |        |
| Nets       |        |

Tcl Console Messages Log Reports Design Runs Timing x Debug

Intra-Clock Paths - sys\_clk\_pin - Setup

| Name   | Slack | ^1 | Levels | Routes | High Fanout                     | From                       | To    | Total Delay | Logic Delay | Net Delay | Req |
|--------|-------|----|--------|--------|---------------------------------|----------------------------|-------|-------------|-------------|-----------|-----|
| Path 1 | 5.445 | 2  | 3      | 1      | RAMblock/me...g/CLKBWRCLK       | SPIbLock/MISO_reg/D        | 4.404 | 2.702       | 1.702       |           |     |
| Path 2 | 6.692 | 3  | 4      | 16     | SPIbLock/FSM_o...state_reg[3]/C | SPIbLock/MISO_reg/CE       | 2.926 | 0.999       | 1.927       |           |     |
| Path 3 | 6.970 | 2  | 3      | 24     | SPIbLock/FSM_o...state_reg[4]/C | SPIbLock/rx_data_reg[0]/CE | 2.648 | 0.875       | 1.773       |           |     |
| Path 4 | 6.970 | 2  | 3      | 24     | SPIbLock/FSM_o...state_reg[4]/C | SPIbLock/rx_data_reg[1]/CE | 2.648 | 0.875       | 1.773       |           |     |
| Path 5 | 6.970 | 2  | 3      | 24     | SPIbLock/FSM_o...state_reg[4]/C | SPIbLock/rx_data_reg[2]/CE | 2.648 | 0.875       | 1.773       |           |     |
| Path 6 | 6.970 | 2  | 3      | 24     | SPIbLock/FSM_o...state_reg[4]/C | SPIbLock/rx_data_reg[3]/CE | 2.648 | 0.875       | 1.773       |           |     |

Timing Summary - timing\_1

Activating Windows

Go to 'Settings' to activate Windows.

SYNTHESIZED DESIGN - xc7a35tcpg236-1L (active)

**Schematic** x Constraints\_basys3.xdc x SPI.v x SPIWrapper.v x Path 1 - timing\_1 x

Path Properties

Path 1

| Name       | Path 1 |
|------------|--------|
| General    |        |
| Properties |        |
| Report     |        |
| Cells      |        |
| Nets       |        |

Tcl Console Messages Log Reports Design Runs Timing x Debug

Intra-Clock Paths - sys\_clk\_pin - Setup

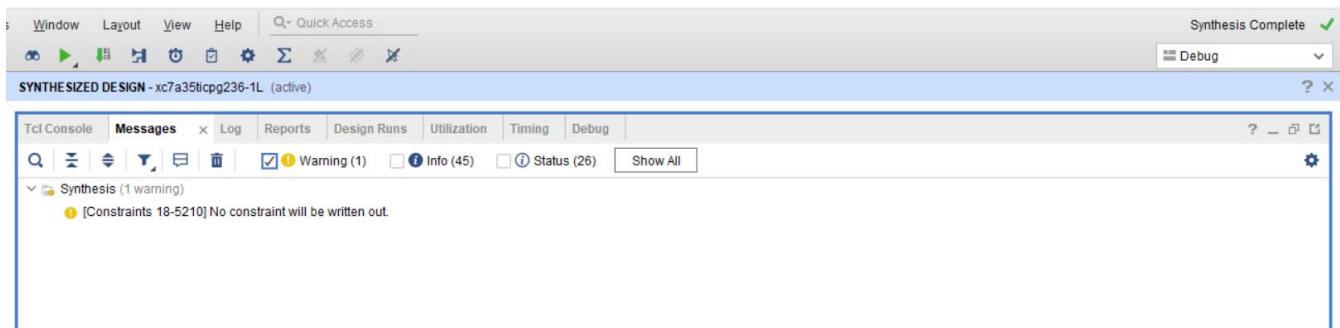
| Name   | Slack | ^1 | Levels | Routes | High Fanout                     | From                       | To    | Total Delay | Logic Delay | Net Delay | Req |
|--------|-------|----|--------|--------|---------------------------------|----------------------------|-------|-------------|-------------|-----------|-----|
| Path 1 | 5.445 | 2  | 3      | 1      | RAMblock/me...g/CLKBWRCLK       | SPIbLock/MISO_reg/D        | 4.404 | 2.702       | 1.702       |           |     |
| Path 2 | 6.692 | 3  | 4      | 16     | SPIbLock/FSM_o...state_reg[3]/C | SPIbLock/MISO_reg/CE       | 2.926 | 0.999       | 1.927       |           |     |
| Path 3 | 6.970 | 2  | 3      | 24     | SPIbLock/FSM_o...state_reg[4]/C | SPIbLock/rx_data_reg[0]/CE | 2.648 | 0.875       | 1.773       |           |     |
| Path 4 | 6.970 | 2  | 3      | 24     | SPIbLock/FSM_o...state_reg[4]/C | SPIbLock/rx_data_reg[1]/CE | 2.648 | 0.875       | 1.773       |           |     |
| Path 5 | 6.970 | 2  | 3      | 24     | SPIbLock/FSM_o...state_reg[4]/C | SPIbLock/rx_data_reg[2]/CE | 2.648 | 0.875       | 1.773       |           |     |
| Path 6 | 6.970 | 2  | 3      | 24     | SPIbLock/FSM_o...state_reg[4]/C | SPIbLock/rx_data_reg[3]/CE | 2.648 | 0.875       | 1.773       |           |     |

Timing Summary - timing\_1

Activating Windows

Go to 'Settings' to activate Windows.

- Message after Synthesis

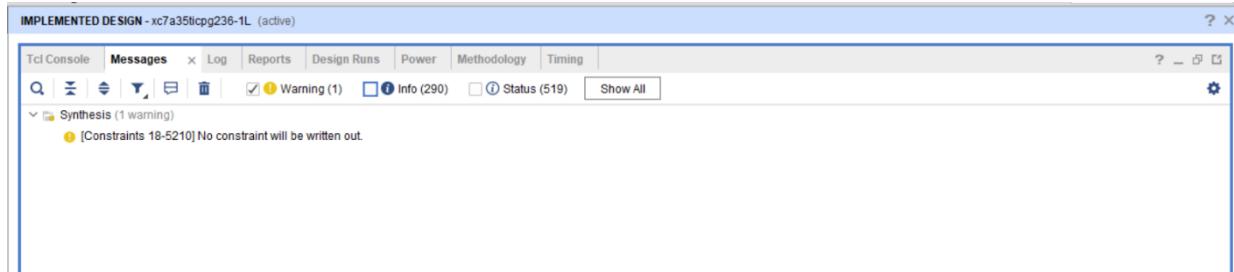


- Implement Utilization

IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

| Name                         | Slice LUTs (20800) | Slice Registers (41600) | F7 Muxes (16300) | Slice (8150) | LUT as Logic (20800) | LUT as Memory (9600) | LUT Flip Flop Pairs (20800) | Block RAM Tile (50) | Bonded IOB (106) | BUFGCT (32) |
|------------------------------|--------------------|-------------------------|------------------|--------------|----------------------|----------------------|-----------------------------|---------------------|------------------|-------------|
| <b>SPIWrapper</b>            | 1278               | 1951                    | 10               | 626          | 1170                 | 108                  | 756                         | 1                   | 5                |             |
| > <b>dbg_hub (dbg_hub)</b>   | 476                | 727                     | 0                | 235          | 452                  | 24                   | 309                         | 0                   | 0                |             |
| <b>RAMBlock (RAM)</b>        | 2                  | 9                       | 0                | 3            | 2                    | 0                    | 0                           | 0.5                 | 0                |             |
| <b>SPIBlock (SPI)</b>        | 36                 | 26                      | 0                | 11           | 36                   | 0                    | 25                          | 0                   | 0                |             |
| > <b>u_ilia_0 (u_ilia_0)</b> | 764                | 1189                    | 10               | 383          | 680                  | 84                   | 422                         | 0.5                 | 0                |             |

- Implement Message

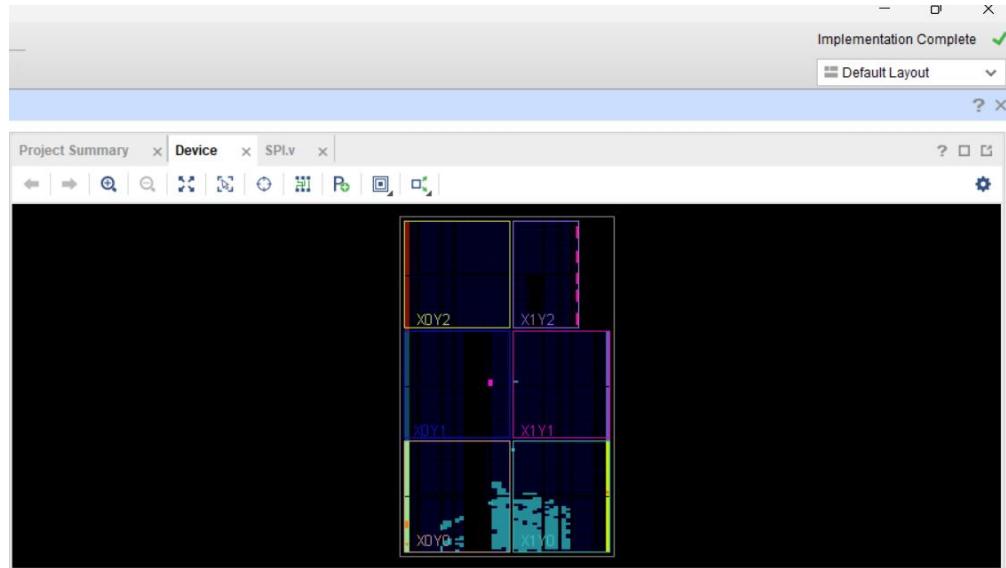


- Implement Timing Without Debug core

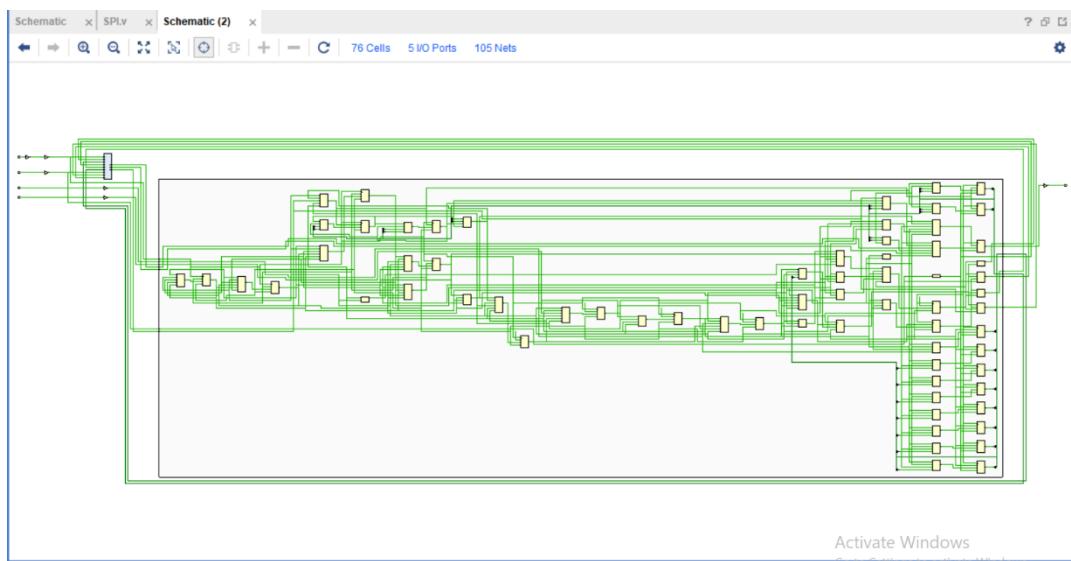
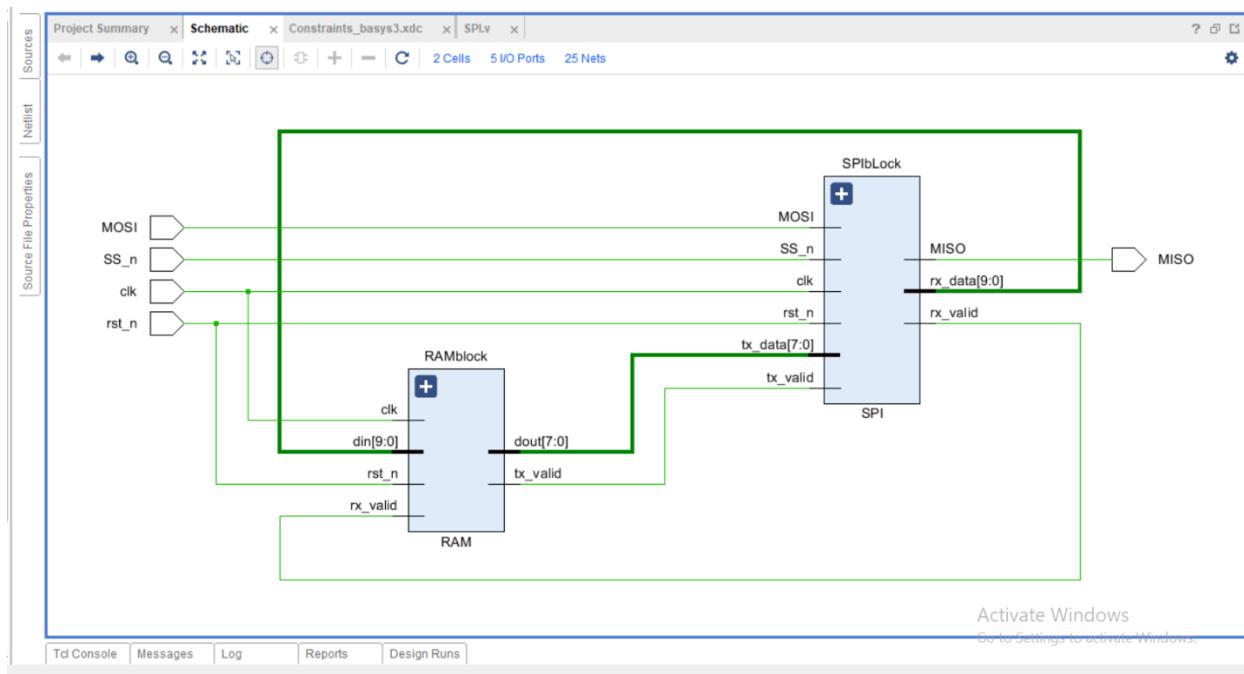
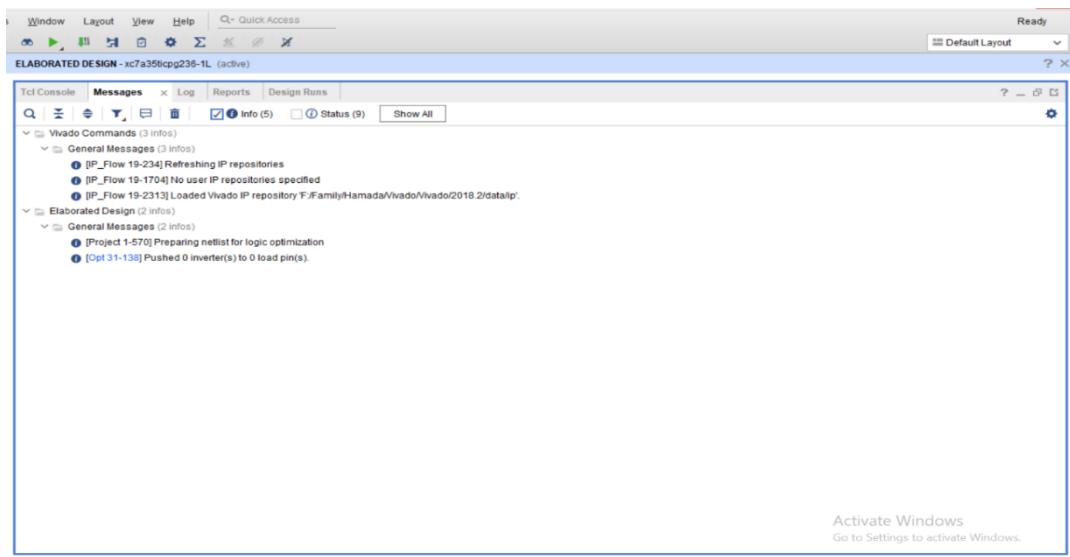
IMPLEMENTED DESIGN - xc7a35ticpg236-1L (active)

| Setup                                       | Hold                                    | Pulse Width   |
|---|---|---|
| Worst Negative Slack (WNS): <b>5.551 ns</b> | Worst Hold Slack (WHS): <b>0.109 ns</b> | Worst Pulse Width Slack (WPWS): <b>4.500 ns</b>           |
| Total Negative Slack (TNS): <b>0.000 ns</b> | Total Hold Slack (THS): <b>0.000 ns</b> | Total Pulse Width Negative Slack (TPWNS): <b>0.000 ns</b> |
| Number of Failing Endpoints: <b>0</b>       | Number of Failing Endpoints: <b>0</b>   | Number of Failing Endpoints: <b>0</b>                     |
| Total Number of Endpoints: <b>90</b>        | Total Number of Endpoints: <b>90</b>    | Total Number of Endpoints: <b>38</b>                      |

All user specified timing constraints are met.



- Gray Encoding



**Synthesized Design - xc7a35tciapg236-1L (active)**

**Timing**

**Design Timing Summary**

| Setup                        |          | Hold                         |          | Pulse Width                              |          |
|------------------------------|----------|------------------------------|----------|--|----------|
| Worst Negative Slack (WNS):  | 5.682 ns | Worst Hold Slack (WHS):      | 0.142 ns | Worst Pulse Width Slack (WPWS):          | 4.500 ns |
| Total Negative Slack (TNS):  | 0.000 ns | Total Hold Slack (THS):      | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0        | Number of Failing Endpoints: | 0        | Number of Failing Endpoints:             | 0        |
| Total Number of Endpoints:   | 87       | Total Number of Endpoints:   | 87       | Total Number of Endpoints:               | 36       |

All user specified timing constraints are met.

**Utilization**

**Hierarchy**

| Name           | Slice LUTs (20800) | Slice Registers (41600) | Block RAM Tile (50) | Bonded IOB (106) | BUFGCTRL (32) |
|----------------|--------------------|-------------------------|---------------------|------------------|---------------|
| N SPIWrapper   | 40                 | 33                      | 0.5                 | 5                | 1             |
| RAMblock (RAM) | 2                  | 9                       | 0.5                 | 0                | 0             |
| SPIbLock (SPI) | 38                 | 24                      | 0                   | 0                | 0             |

**Schematic (5)**

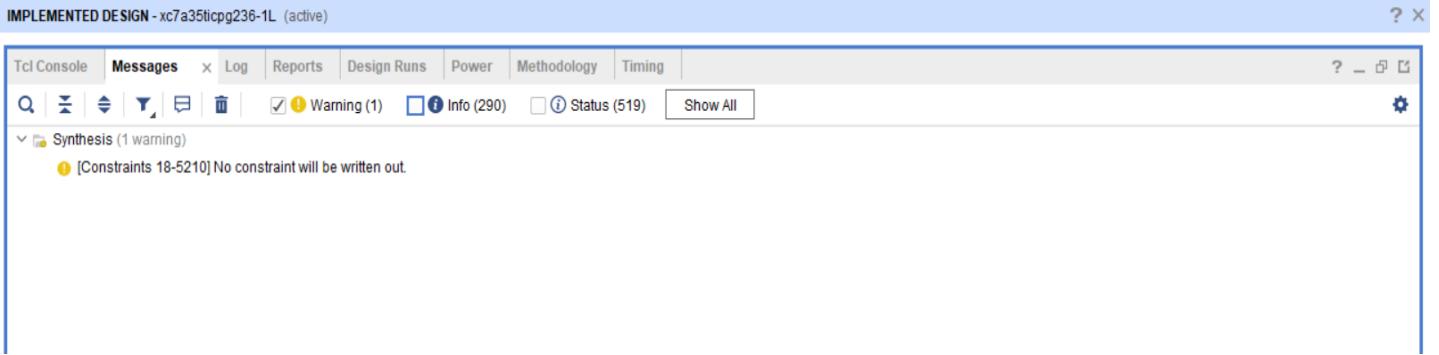
**Timing**

**Intra-Clock Paths - sys\_clk\_pin - Setup**

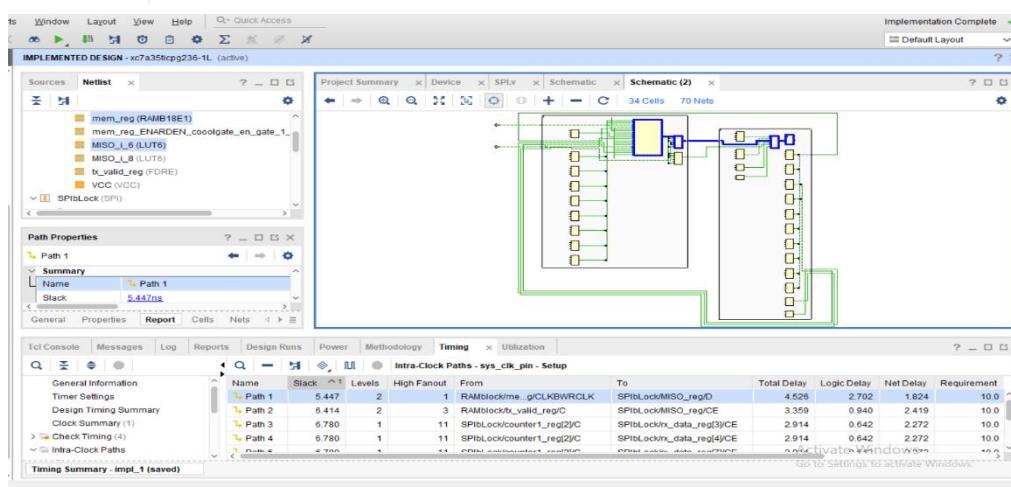
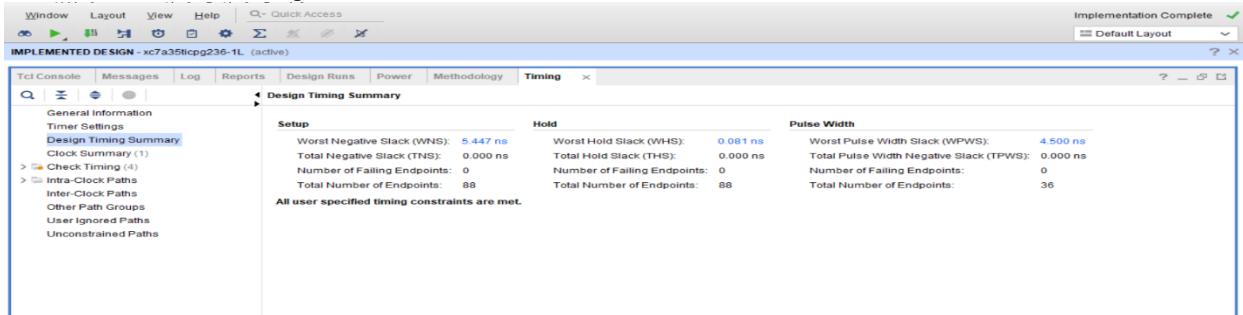
| Name   | Slack | Levels | Routes | High Fanout | From                            | To                          | Total Delay | Logic Delay | Net Delay | Req |
|--------|-------|--------|--------|-------------|---------------------------------|-----------------------------|-------------|-------------|-----------|-----|
| Path 1 | 5.682 | 2      | 3      | 1           | RAMblock/me...g/CLKBWRCLK       | SPIbLock/MISO_reg/D         | 4.167       | 2.702       | 1.465     |     |
| Path 2 | 6.533 | 2      | 3      | 3           | RAMblocktx_valid_reg/C          | SPIbLock/MISO_reg/CE        | 3.085       | 0.875       | 2.210     |     |
| Path 3 | 6.956 | 2      | 3      | 25          | SPIbLock/FSM_g...state_reg[2]/C | SPIbLock/counter1_reg[0]/CE | 2.662       | 0.875       | 1.787     |     |
| Path 4 | 6.956 | 2      | 3      | 25          | SPIbLock/FSM_g...state_reg[2]/C | SPIbLock/counter1_reg[1]/CE | 2.662       | 0.875       | 1.787     |     |
| Path 5 | 6.956 | 2      | 3      | 25          | SPIbLock/FSM_g...state_reg[2]/C | SPIbLock/counter1_reg[2]/CE | 2.662       | 0.875       | 1.787     |     |
| Path 6 | 6.956 | 2      | 3      | 25          | SPIbLock/FSM_g...state_reg[2]/C | SPIbLock/counter2_reg[0]/CE | 2.662       | 0.875       | 1.787     |     |
| Path 7 | 6.978 | 2      | 3      | 9           | SPIbLock/counter2_reg[0]/C      | SPIbLock/counter2_reg[1]/CE | 2.640       | 0.901       | 1.739     |     |
| Path 8 | 6.978 | 2      | 3      | 9           | SPIbLock/counter2_reg[1]/C      | SPIbLock/counter2_reg[1]/CE | 2.640       | 0.901       | 1.739     |     |

Timing Summary - timing\_1      Timing Summary - timing\_2

- Implemented Message



- Implementation Time:



Timing Summary - impl\_1 (saved)

| Name           | 1  | Slice LUTs (20800) | Slice Registers (41600) | Slice (8150) | LUT as Logic (20800) | LUT Flip Flop Pairs (20800) | Block RAM Tile (50) | Bonded IOB (106) | BUFGCTRL (32) |
|----------------|----|--------------------|-------------------------|--------------|----------------------|-----------------------------|---------------------|------------------|---------------|
| spiwrapper     | 41 | 33                 | 13                      | 41           | 22                   | 0.5                         | 5                   | 1                |               |
| RAMblock (RAM) | 3  | 9                  | 4                       | 3            | 0                    | 0.5                         | 0                   | 0                |               |
| SPIBlock (SPI) | 38 | 24                 | 12                      | 38           | 22                   | 0                           | 0                   | 0                |               |

- Sequential Encoding

Schematic x Constraints\_basys3.xdc x SPI.v x SPIWrapper.v x synth\_1\_synth\_synthesis\_report\_0 - synth\_1 x F:/Family/SynthesisKareemWassemTasks/Projj2Finaaaal/project\_2/runs/synth\_1/SPIWrapper.vds

Q | H | ← | → | X | // | E | O | Read-only | settings

```

6 # Process ID: 10156
7 # Current directory: F:/Family/SynthesisKareemWassemTasks/Projj2Finaaaal/project_2/runs/synth_1
8 # Command line: vivado.exe -log SPIWrapper.vds -product Vivado -mode batch -messageDb vivado.pb -notrace -source SPIWrapper.tcl
9 # Log file: F:/Family/SynthesisKareemWassemTasks/Projj2Finaaaal/project_2/runs/synth_1/SPIWrapper.vds
10 # Journal file: F:/Family/SynthesisKareemWassemTasks/Projj2Finaaaal/project_2/runs/synth_1\vivado.jou
11 -----
12 source SPIWrapper.tcl -notrace
13 Command: synth_design -top SPIWrapper -part xc7a35tictcpg236-1L
14 Starting synth_design
15 Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35ti'
16 INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
17 INFO: Launching helper process for spawning children vivado processes
18 INFO: Helper process launched with PID 1932
19 -----
20 Starting RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 355.492 ; gain = 98.867
21 -----
22 INFO: [Synth 8-6157] synthesizing module 'SPIWrapper' [F:/Family/SynthesisKareemWassemTasks/Projj2Finaaaal/SPIWrapper.v:1]
23     Parameter MEM_DEPTH bound to: 256 - type: integer
24     Parameter ADDR_SIZE bound to: 8 - type: integer
25 INFO: [Synth 8-6157] synthesizing module 'SPI' [F:/Family/SynthesisKareemWassemTasks/Projj2Finaaaal/SPI.v:1]
26     Parameter IDLE bound to: 3'b000
27     Parameter CHK_CMD bound to: 3'b001
28     Parameter WRITE bound to: 3'b011
29     Parameter READ_ADD bound to: 3'b101
30     Parameter READ_DATA bound to: 3'b111
31 INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential" *) [F:/Family/SynthesisKareemWassemTasks/Projj2Finaaaal/SPI.v:17]
32 INFO: [Synth 8-155] case statement is not full and has no default [F:/Family/SynthesisKareemWassemTasks/Projj2Finaaaal/SPI.v:91]
33 INFO: [Synth 8-6155] done synthesizing module 'SPI' (#1) [F:/Family/SynthesisKareemWassemTasks/Projj2Finaaaal/SPI.v:1]
34 INFO: [Synth 8-6157] synthesizing module 'RAM' [F:/Family/SynthesisKareemWassemTasks/Projj2Finaaaal/RAM.v:1]
35     Parameter MEM_DEPTH bound to: 256 - type: integer
36     Parameter ADDR_SIZE bound to: 8 - type: integer

```

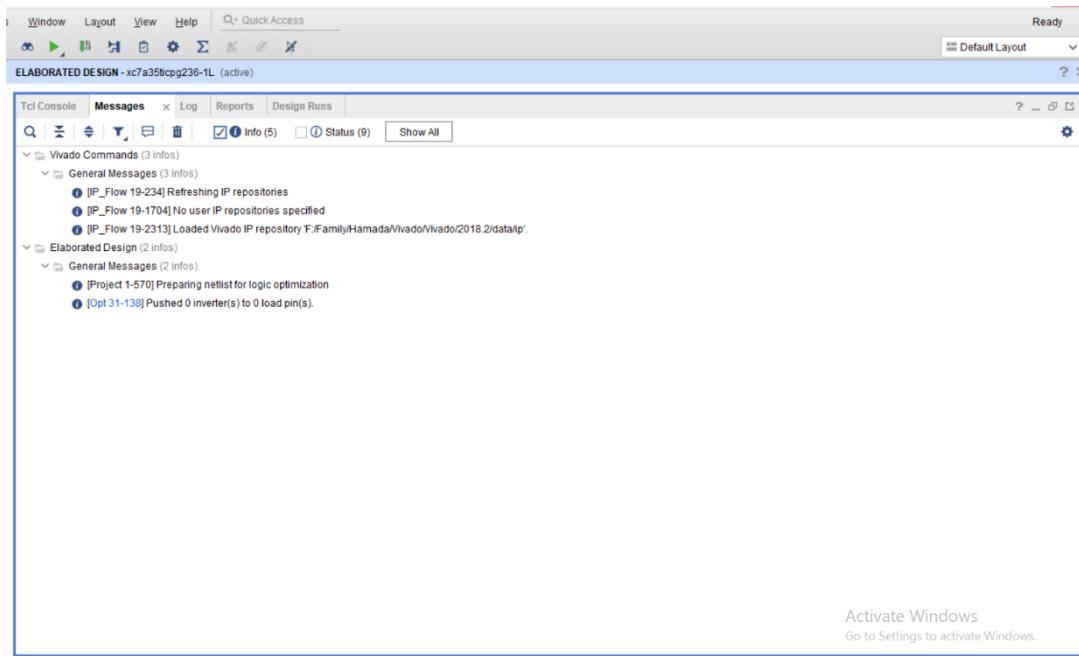
Activate Windows

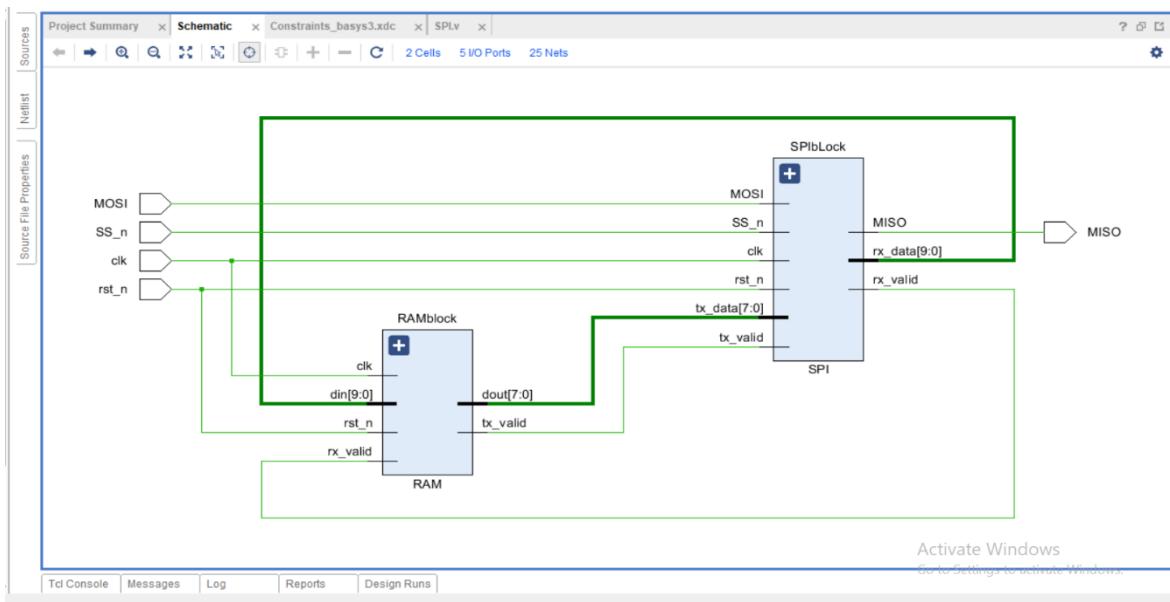
| 96  | 97 | State     | New Encoding | Previous Encoding |
|-----|----|-----------|--------------|-------------------|
| 98  |    | IDLE      | 000          | 000               |
| 100 |    | CHK_CMD   | 001          | 001               |
| 101 |    | WRITE     | 010          | 011               |
| 102 |    | READ_ADD  | 011          | 101               |
| 103 |    | READ_DATA | 100          | 111               |

104 -----

105 INFO: [Synth 8-3354] encoded FSM with state register 'current\_state\_reg' using encoding 'sequential' in module 'SPI'

106



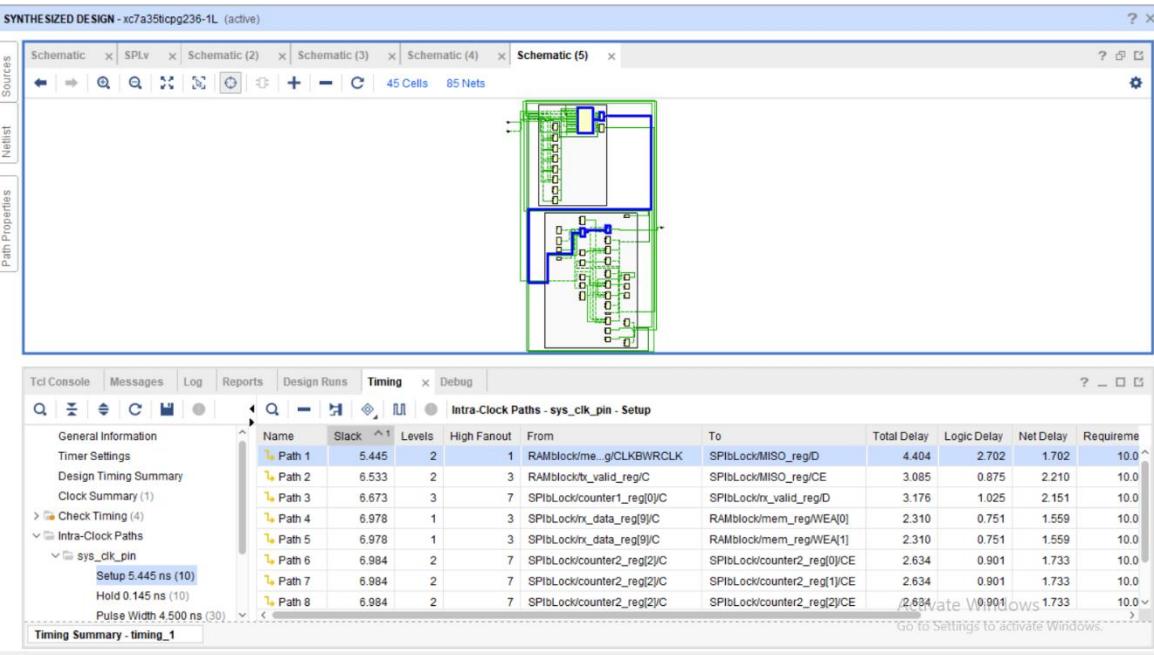


### SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)

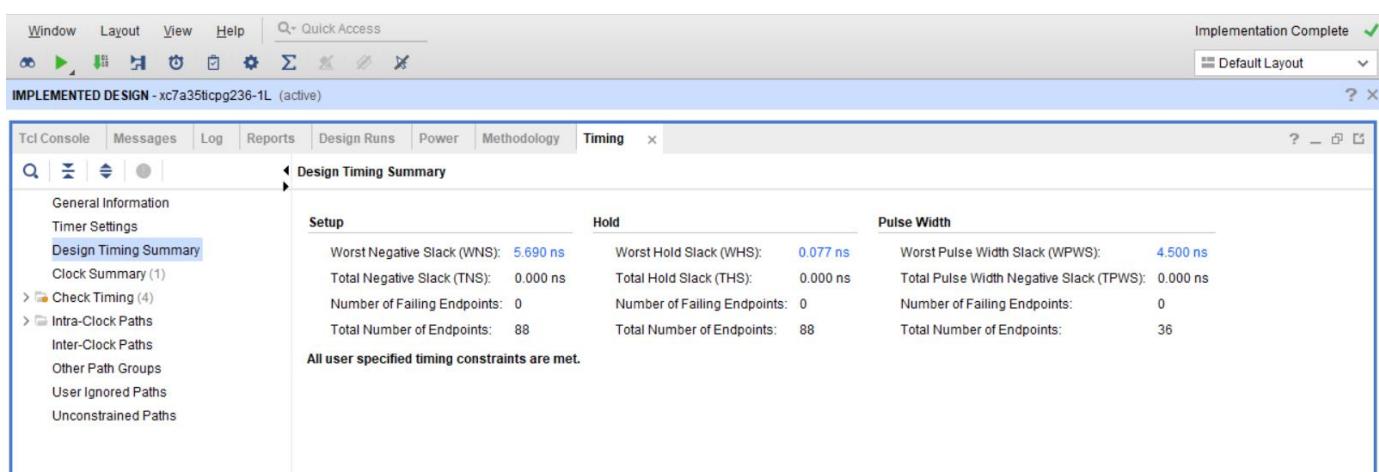
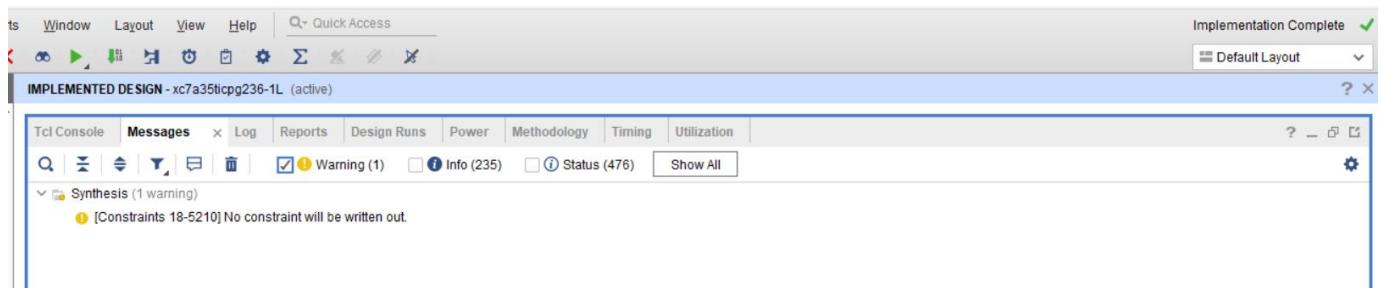
| Hierarchy |                |    |                    |                         |                     |
|-----------|----------------|----|--------------------|-------------------------|---------------------|
|           | Name           | 1  | Slice LUTs (20800) | Slice Registers (41600) | Block RAM Tile (50) |
| +         | N SPIWrapper   | 39 | 33                 | 0.5                     | 5                   |
|           | RAMblock (RAM) | 2  | 9                  | 0.5                     | 0                   |
|           | SPIbLock (SPI) | 37 | 24                 | 0                       | 0                   |

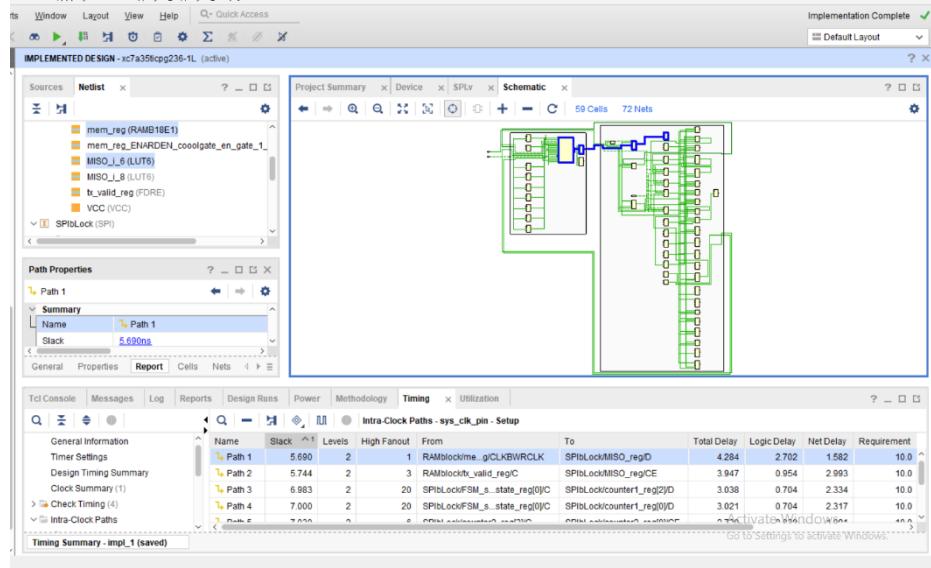
### SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)

| Design Timing Summary        |                 |                              |                 |
|------------------------------|-----------------|------------------------------|-----------------|
| General Information          |                 | Setup                        |                 |
| Worst Negative Slack (WNS):  | <b>5.445 ns</b> | Worst Hold Slack (WHS):      | <b>0.145 ns</b> |
| Total Negative Slack (TNS):  | <b>0.000 ns</b> | Total Hold Slack (THS):      | <b>0.000 ns</b> |
| Number of Failing Endpoints: | <b>0</b>        | Number of Failing Endpoints: | <b>0</b>        |
| Total Number of Endpoints:   | <b>87</b>       | Total Number of Endpoints:   | <b>87</b>       |

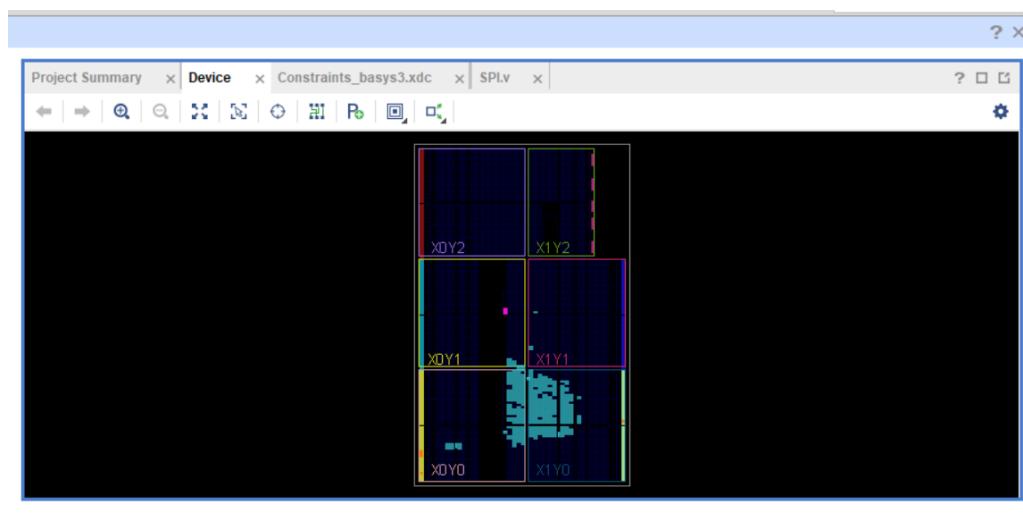


### o Implemented Message:

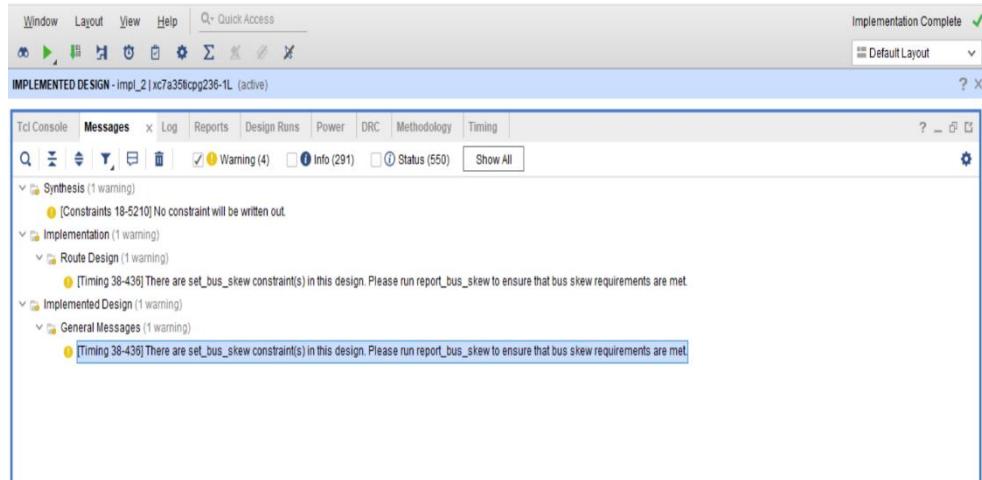




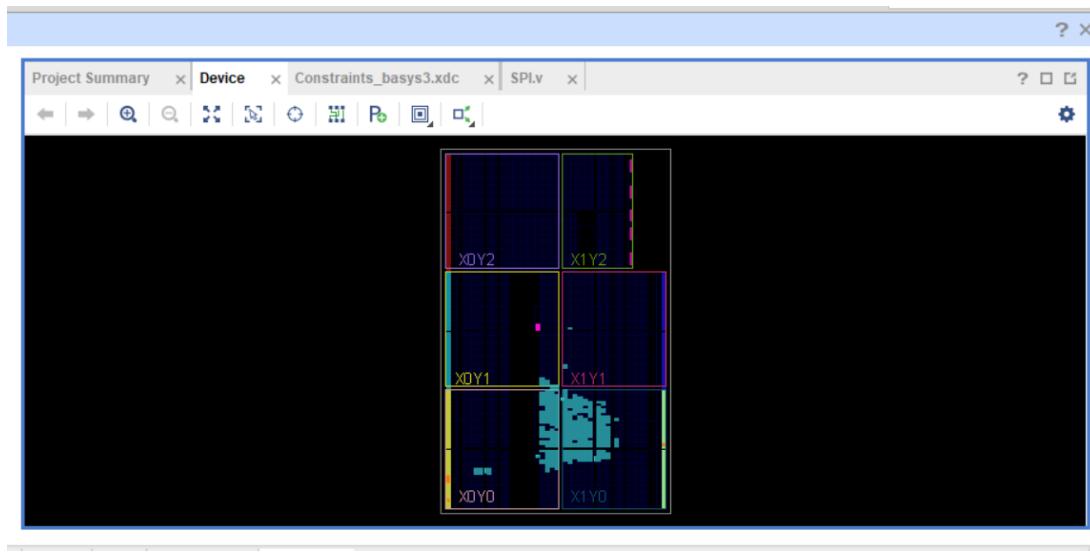
Conclusion: it is better here To use One Hot Encoding to obtain Highest Frequency to operate. And I used it to generate bitstream file.



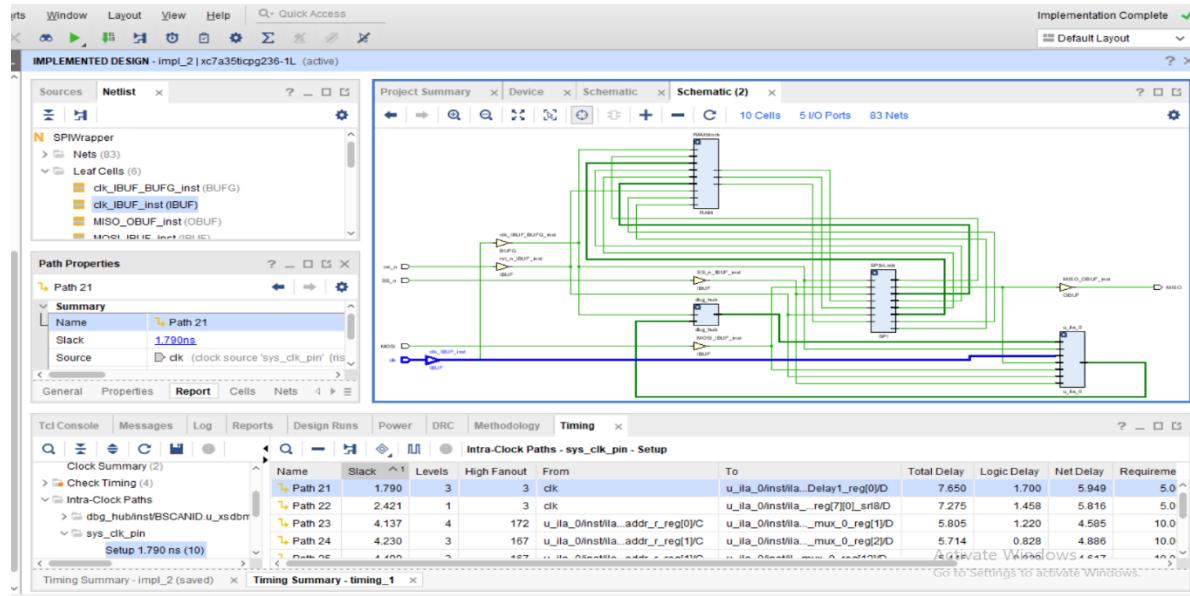
- Message After Implementation With Debug Core



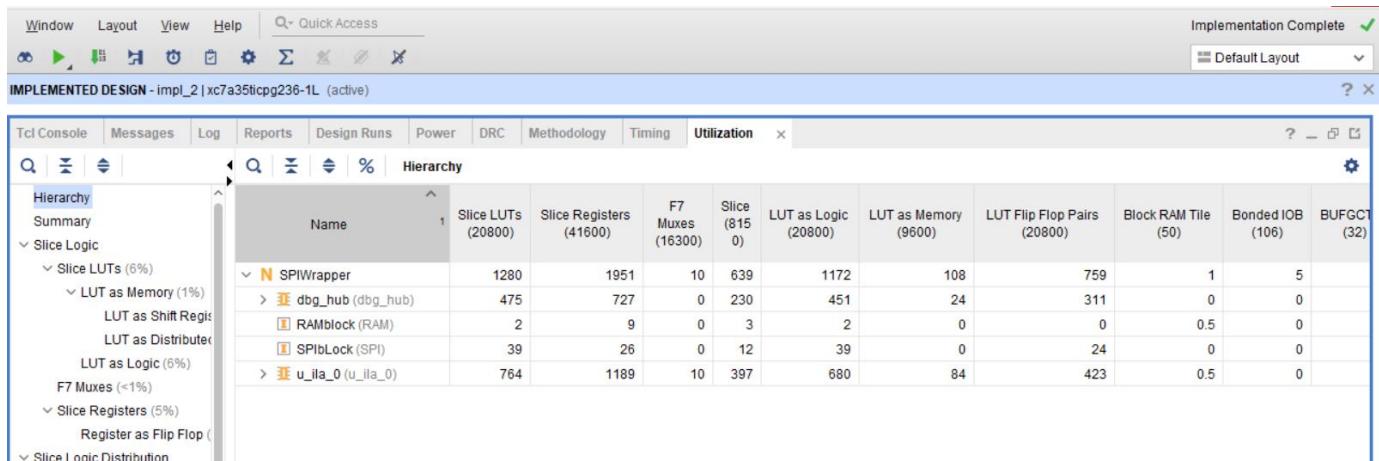
- FPGA Schematic After Implementation with debug core



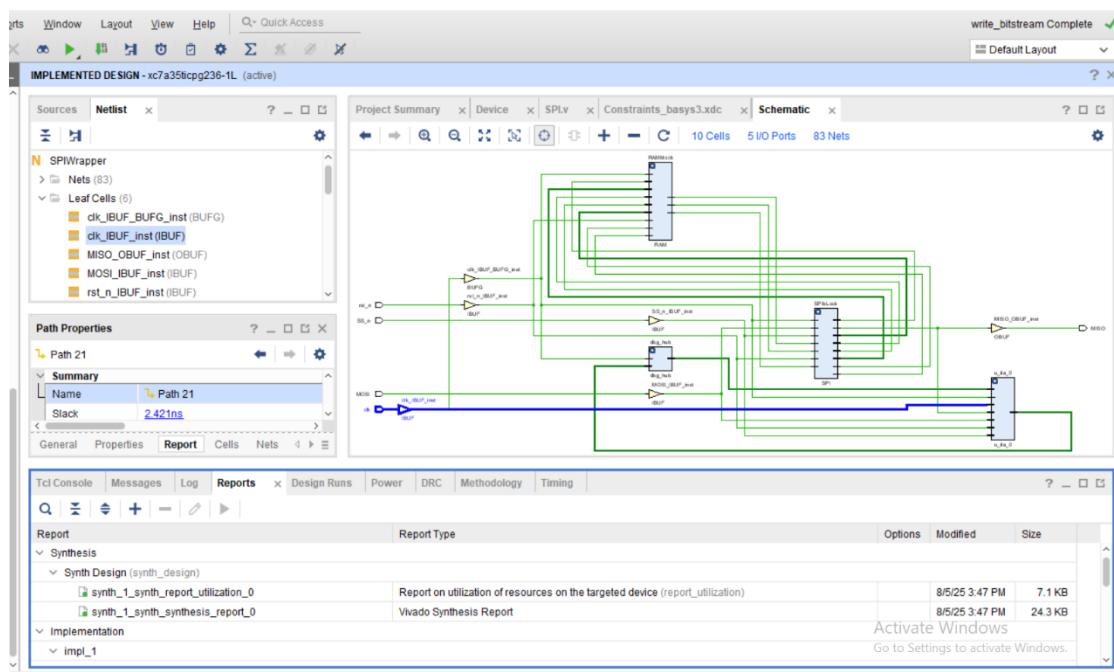
- Highest Path with Delay after Implementation After Debug Core



- Report Utilization After Implementation with debug core



- Bitstream Generation after Debug Core



- Constraint File

```

5
6 ## Clock signal
7 set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports clk]
8 create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports clk]
9
10
11 ## Switches
12 set_property -dict {PACKAGE_PIN V17 IOSTANDARD LVCMOS33} [get_ports MOSI]
13 set_property -dict {PACKAGE_PIN V16 IOSTANDARD LVCMOS33} [get_ports SS_N]
14 #set_property -dict { PACKAGE_PIN W16 IOSTANDARD LVCMOS33 } [get_ports {sw[2]}]
15 #set_property -dict { PACKAGE_PIN W17 IOSTANDARD LVCMOS33 } [get_ports {sw[3]}]
16 #set_property -dict { PACKAGE_PIN V15 IOSTANDARD LVCMOS33 } [get_ports {sw[4]}]
17 #set_property -dict { PACKAGE_PIN V13 IOSTANDARD LVCMOS33 } [get_ports {sw[5]}]
18 #set_property -dict { PACKAGE_PIN W14 IOSTANDARD LVCMOS33 } [get_ports {sw[6]}]
19 #set_property -dict { PACKAGE_PIN W13 IOSTANDARD LVCMOS33 } [get_ports {sw[7]}]
20 #set_property -dict { PACKAGE_PIN V2 IOSTANDARD LVCMOS33 } [get_ports {sw[8]}]
21 #set_property -dict { PACKAGE_PIN T3 IOSTANDARD LVCMOS33 } [get_ports {sw[9]}]
22 #set_property -dict { PACKAGE_PIN T2 IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
23 #set_property -dict { PACKAGE_PIN R3 IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
24 #set_property -dict { PACKAGE_PIN M2 IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
25 #set_property -dict { PACKAGE_PIN U1 IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
26 #set_property -dict { PACKAGE_PIN T1 IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
27 #set_property -dict { PACKAGE_PIN R2 IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]
28
29
30 ## LEDs
31 set_property -dict {PACKAGE_PIN U16 IOSTANDARD LVCMOS33} [get_ports MISO]
32 #set_property -dict { PACKAGE_PIN E19 IOSTANDARD LVCMOS33 } [get_ports {led[1]}]
33 #set_property -dict { PACKAGE_PIN H19 IOSTANDARD LVCMOS33 } [get_ports {led[2]}]

```

```

64
65
66 ##Buttons
67 set_property -dict {PACKAGE_PIN U18 IOSTANDARD LVCMOS33} [get_ports rst_n]
68 #set_property -dict { PACKAGE_PIN T18 IOSTANDARD LVCMOS33 } [get_ports btnU]
69 #set_property -dict { PACKAGE_PIN W19 IOSTANDARD LVCMOS33 } [get_ports btnL]
70 #set_property -dict { PACKAGE_PIN T17 IOSTANDARD LVCMOS33 } [get_ports btnR]
71 #set_property -dict { PACKAGE_PIN U17 IOSTANDARD LVCMOS33 } [get_ports btnD]
72
73

152 ## Configuration options, can be used for all designs
153 set_property CONFIG_VOLTAGE 3.3 [current_design]
154 set_property CFGBVS VCCO [current_design]
155
156 ## SPI configuration mode options for QSPI boot, can be used for all designs
157 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
158 set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
159 set_property CONFIG_MODE SPIX4 [current_design]
160
161 create_debug_core u_ila_0 ila
162 set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
163 set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
164 set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
165 set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
166 set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
167 set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
168 set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
169 set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
170 set_property port_width 1 [get_debug_ports u_ila_0/clk]
171 connect_debug_port u_ila_0/clk [get_nets [list clk_IBUF_BUFG]]
172 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
173 set_property port_width 1 [get_debug_ports u_ila_0/probe0]
174 connect_debug_port u_ila_0/probe0 [get_nets [list clk_IBUF]]
175 create_debug_port u_ila_0 probe
176 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
177 set_property port_width 1 [get_debug_ports u_ila_0/probe1]
178 connect_debug_port u_ila_0/probe1 [get_nets [list MISO_OBUF]]
179 create_debug_port u_ila_0 probe
180 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
181 set_property port_width 1 [get_debug_ports u_ila_0/probe2]
182 connect_debug_port u_ila_0/probe2 [get_nets [list MOSI_IBUF]]
183 create_debug_port u_ila_0 probe
184 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
185 set_property port_width 1 [get_debug_ports u_ila_0/probe3]
186 connect_debug_port u_ila_0/probe3 [get_nets [list rst_n_IBUF]]
187 create_debug_port u_ila_0 probe
188 set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
189 set_property port_width 1 [get_debug_ports u_ila_0/probe4]
190 connect_debug_port u_ila_0/probe4 [get_nets [list SS_n_IBUF]]
191 set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
192 set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
193 set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
194 connect_debug_port dbg_hub/clk [get_nets clk_IBUF_BUFG]
195

```

- Link For Verilog Code Files & Constraints file:

[https://drive.google.com/drive/folders/1qXkQ5w1o80IBtnOUyWGcMueKFCOsKCLm?usp=drive\\_link](https://drive.google.com/drive/folders/1qXkQ5w1o80IBtnOUyWGcMueKFCOsKCLm?usp=drive_link)