Mixed-Signal Excellence

Digital Design Assignment

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Rev 1.0

1   Assignment Details

Please consider the following design example for a controller unit for a washing machine
- The operation of the machine consists of the following states:
  - o   Idle
  - o   Filling Water
  - o   Washing
  - o   Rinsing
  - o   Spinning

- The inputs/ outputs of the design are given by the below table

Port	Direction	Description
rst_n	Input	Active low asynchronous clock
clk	Input	System clock
clk_freq[1:0]	Input	Input Clock Frequency Configuration Code
coin_in	input	Input flag which is asserted when a coin is deposited
double_wash	input	Input flag which is asserted if the user requires double wash option
timer_pause	input	Input flag when it is set to '1' spinning phase is paused until this flag is de-asserted
wash_done	output	Active high output asserted when spinning phase is done and deasserted when coin_in is set to '1'

- The input clock can have 1 of 4 frequencies, encoded by the clk_freq[1:0] input port, the encoding is given by the following table

clk_freq	Clock Frequency (MHz)
2'b00	1
2'b01	2
2'b10	4
2'b11	8

- The machine starts when a coin is deposited. (Assume that the user will only deposit the exact amount of coins)
- There is a double wash input, when it is turned on, a second wash and rinse to occur after completing the first rinse. Assume that the double wash button is pressed before depositing the coins (if needed) and stays pressed till the job completes.

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- If the timer_pause flag is asserted during the spin cycle, the machine stops spinning until the flag is de-asserted. Note that the machine is designed to stop when this flag is raised only during the spin cycle.
- Each state of this machine takes a time period as stated in the following table

State	Time Duration (Minutes)
Filling Water	2
Washing	5
Rinsing	2
Spinning	1

2 Deliverables

1. A well *commented and synthesizable* Verilog code for this design.
2. A Verilog Test Bench to verify the design and try to cover all the possible scenarios
3. A *presentation* containing the following:
   a. Clear explanation of the problem/requirements.
   b. Overview of the Solution and Design flow.
   c. Detailed explanation of your code.
   d. The testing covered scenarios.

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3   Revision History

Revision Number	Revision Date	Changes
1.0	06/15/2022	Version 1.0 release

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