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\* Final Report \*

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Final Results

RTL Top Level Output File Name : FP\_Multiplier\_Single.ngr

Top Level Output File Name : FP\_Multiplier\_Single

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 96

Cell Usage :

# BELS : 794

# GND : 1

# INV : 2

# LUT1 : 4

# LUT2 : 163

# LUT3 : 113

# LUT4 : 329

# MULT\_AND : 17

# MUXCY : 90

# MUXF5 : 2

# VCC : 1

# XORCY : 72

# IO Buffers : 96

# IBUF : 64

# OBUF : 32

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Device utilization summary:

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Selected Device : 3s5000fg1156-4

Number of Slices: 344 out of 33280 1%

Number of 4 input LUTs: 611 out of 66560 0%

Number of IOs: 96

Number of bonded IOBs: 96 out of 784 12%

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Partition Resource Summary:

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No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 65.460ns

Timing Detail:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis

Total number of paths / destination ports: 34051591346 / 32

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Delay: 65.460ns (Levels of Logic = 40)

Source: A<18> (PAD)

Destination: Out<26> (PAD)

Data Path: A<18> to Out<26>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 17 0.821 1.684 A\_18\_IBUF (A\_18\_IBUF)

LUT2:I0->O 3 0.551 0.000 MM0/MM0/Madd\_temporary\_1\_0\_addsub0000\_lut<0> (MM0/MM0/temporary\_1<0><0>)

MUXCY:S->O 1 0.500 0.000 MM0/MM0/Madd\_temporary\_1\_0\_addsub0000\_cy<0> (MM0/MM0/Madd\_temporary\_1\_0\_addsub0000\_cy<0>)

XORCY:CI->O 14 0.904 1.526 MM0/MM0/Madd\_temporary\_1\_0\_addsub0000\_xor<1> (MM0/MM0/temporary\_1<0><1>)

LUT2:I0->O 3 0.551 1.246 MM0/MM0/MM2/temp\_7\_and00001 (MM0/MM0/MM2/temp<7>)

LUT4:I0->O 2 0.551 1.216 MM0/MM0/MM2/Madd\_AUX\_17\_addsub00051 (MM0/MM0/MM2/Madd\_AUX\_17\_addsub0005)

LUT4:I0->O 4 0.551 0.985 MM0/MM0/MM2/Madd\_AUX\_17\_addsub0003\_cy<0>11 (MM0/MM0/MM2/Madd\_AUX\_17\_addsub0003\_cy<0>)

LUT4:I2->O 3 0.551 1.246 MM0/MM0/MM2/Madd\_AUX\_17\_addsub0003\_xor<2>11 (MM0/MM0/MM2/cy2<1>)

LUT3:I0->O 2 0.551 1.072 MM0/MM0/MM2/Madd\_AUX\_18\_addsub0004\_cy<1>11 (MM0/MM0/MM2/Madd\_AUX\_18\_addsub0004\_cy<1>)

LUT3:I1->O 3 0.551 1.246 MM0/MM0/MM2/Madd\_AUX\_18\_addsub0004\_xor<2>11 (MM0/MM0/MM2/cy3<1>)

LUT3:I0->O 2 0.551 0.945 MM0/MM0/MM2/Madd\_AUX\_19\_addsub0005\_cy<1>11 (MM0/MM0/MM2/Madd\_AUX\_19\_addsub0005\_cy<1>)

LUT3:I2->O 3 0.551 1.246 MM0/MM0/MM2/Madd\_AUX\_19\_addsub0005\_xor<2>11 (MM0/MM0/MM2/cy4<1>)

LUT3:I0->O 2 0.551 0.945 MM0/MM0/MM2/Madd\_AUX\_20\_addsub0006\_cy<1>11 (MM0/MM0/MM2/Madd\_AUX\_20\_addsub0006\_cy<1>)

LUT3:I2->O 2 0.551 1.216 MM0/MM0/MM2/Madd\_AUX\_20\_addsub0006\_xor<2>11 (MM0/MM0/MM2/cy5<1>)

LUT3:I0->O 2 0.551 1.072 MM0/MM0/MM2/Madd\_\_AUX\_21\_cy<1>11 (MM0/MM0/MM2/Madd\_\_AUX\_21\_cy<1>)

LUT4:I1->O 3 0.551 1.246 MM0/MM0/MM2/Madd\_\_AUX\_21\_xor<2>11 (MM0/MM0/MM2/cy6<1>)

LUT3:I0->O 2 0.551 1.072 MM0/MM0/MM2/Madd\_\_AUX\_22\_Madd\_cy<1>11 (MM0/MM0/MM2/Madd\_\_AUX\_22\_Madd\_cy<1>)

LUT4:I1->O 3 0.551 1.246 MM0/MM0/MM2/Madd\_\_AUX\_22\_Madd\_xor<2>11 (MM0/MM0/MM2/cy7<1>)

LUT3:I0->O 2 0.551 1.072 MM0/MM0/MM2/Madd\_\_AUX\_23\_cy<1>11 (MM0/MM0/MM2/Madd\_\_AUX\_23\_cy<1>)

LUT4:I1->O 3 0.551 1.246 MM0/MM0/MM2/Madd\_\_AUX\_23\_xor<2>11 (MM0/MM0/MM2/cy8<1>)

LUT3:I0->O 2 0.551 0.945 MM0/MM0/MM2/Madd\_AUX\_24\_addsub0006\_cy<1>11 (MM0/MM0/MM2/Madd\_AUX\_24\_addsub0006\_cy<1>)

LUT3:I2->O 3 0.551 1.246 MM0/MM0/MM2/Madd\_AUX\_24\_addsub0006\_xor<2>11 (MM0/MM0/MM2/cy9<1>)

LUT3:I0->O 2 0.551 0.945 MM0/MM0/MM2/Madd\_AUX\_25\_addsub0005\_cy<1>11 (MM0/MM0/MM2/Madd\_AUX\_25\_addsub0005\_cy<1>)

LUT3:I2->O 3 0.551 1.246 MM0/MM0/MM2/Madd\_AUX\_25\_addsub0005\_xor<2>11 (MM0/MM0/MM2/cy10<1>)

LUT3:I0->O 2 0.551 1.072 MM0/MM0/MM2/Madd\_AUX\_26\_addsub0004\_cy<1>11 (MM0/MM0/MM2/Madd\_AUX\_26\_addsub0004\_cy<1>)

LUT3:I1->O 3 0.551 1.246 MM0/MM0/MM2/Madd\_AUX\_26\_addsub0004\_xor<2>11 (MM0/MM0/MM2/cy11<1>)

LUT3:I0->O 2 0.551 1.072 MM0/MM0/MM2/Madd\_AUX\_27\_addsub0003\_cy<1>11 (MM0/MM0/MM2/Madd\_AUX\_27\_addsub0003\_cy<1>)

LUT3:I1->O 3 0.551 0.975 MM0/MM0/MM2/Madd\_AUX\_27\_addsub0003\_xor<2>11 (MM0/MM0/MM2/cy12<1>)

LUT3:I2->O 2 0.551 1.072 MM0/MM0/MM2/Madd\_AUX\_28\_addsub0002\_cy<1>11 (MM0/MM0/MM2/Madd\_AUX\_28\_addsub0002\_cy<1>)

LUT4:I1->O 3 0.551 1.246 MM0/MM0/MM2/Madd\_AUX\_29\_addsub0001\_xor<1>11 (MM0/MM0/MM2/cy14<0>)

LUT3:I0->O 0 0.551 0.000 MM0/MM0/MM2/Madd\_\_AUX\_301 (MM0/MM0/temporary\_2<16>)

MUXCY:DI->O 0 0.889 0.000 MM0/MM0/Msub\_temporary\_3\_cy<16> (MM0/MM0/Msub\_temporary\_3\_cy<16>)

XORCY:CI->O 2 0.904 1.072 MM0/MM0/Msub\_temporary\_3\_xor<17> (MM0/MM0/temporary\_3<17>)

LUT4:I1->O 1 0.551 0.000 MM0/MM0/Madd\_Mul\_Out\_Madd\_lut<25> (N63)

MUXCY:S->O 1 0.500 0.000 MM0/MM0/Madd\_Mul\_Out\_Madd\_cy<25> (MM0/MM0/Madd\_Mul\_Out\_Madd\_cy<25>)

MUXCY:CI->O 0 0.064 0.000 MM0/MM0/Madd\_Mul\_Out\_Madd\_cy<26> (MM0/MM0/Madd\_Mul\_Out\_Madd\_cy<26>)

XORCY:CI->O 31 0.904 1.915 MM0/MM0/Madd\_Mul\_Out\_Madd\_xor<27> (man\_r<27>)

LUT4:I2->O 1 0.551 0.869 Out<26>\_SW0 (N610)

LUT3:I2->O 1 0.551 0.801 Out<26> (Out\_26\_OBUF)

OBUF:I->O 5.644 Out\_26\_OBUF (Out<26>)

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Total 65.460ns (28.211ns logic, 37.249ns route)

(43.1% logic, 56.9% route)

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CPU : 116.10 / 122.65 s | Elapsed : 116.00 / 123.00 s

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Total memory usage is 256088 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 26 ( 0 filtered)

Number of infos : 0 ( 0 filtered)