CND 211

Midterm Project

FIFO Verification

Submitted to:

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Submitted by:

Section: 13

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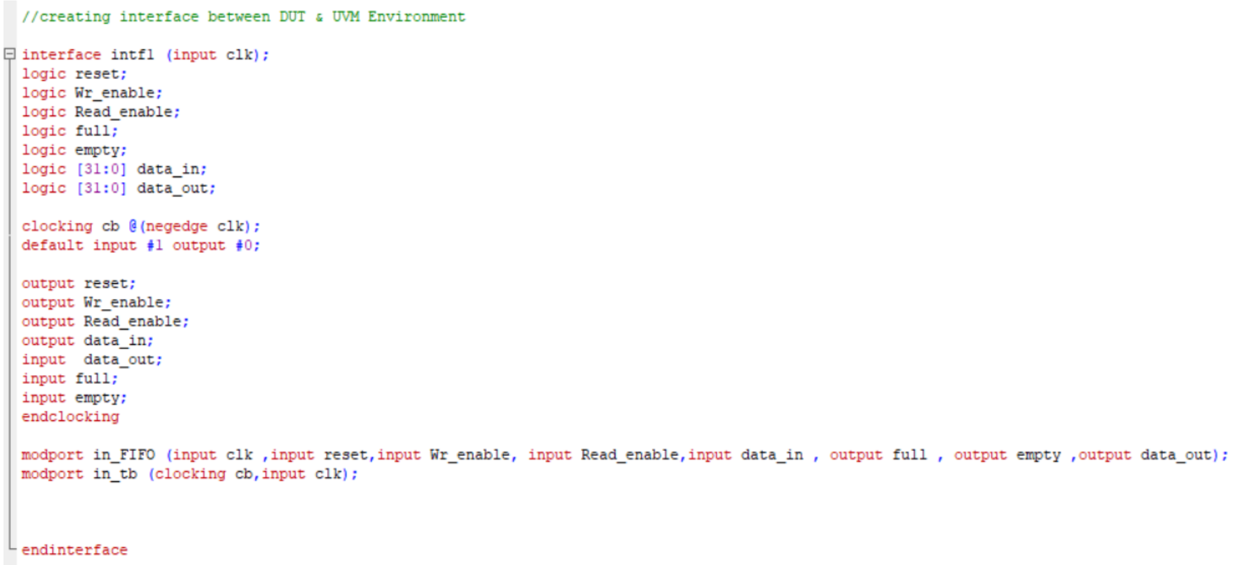
Introduction

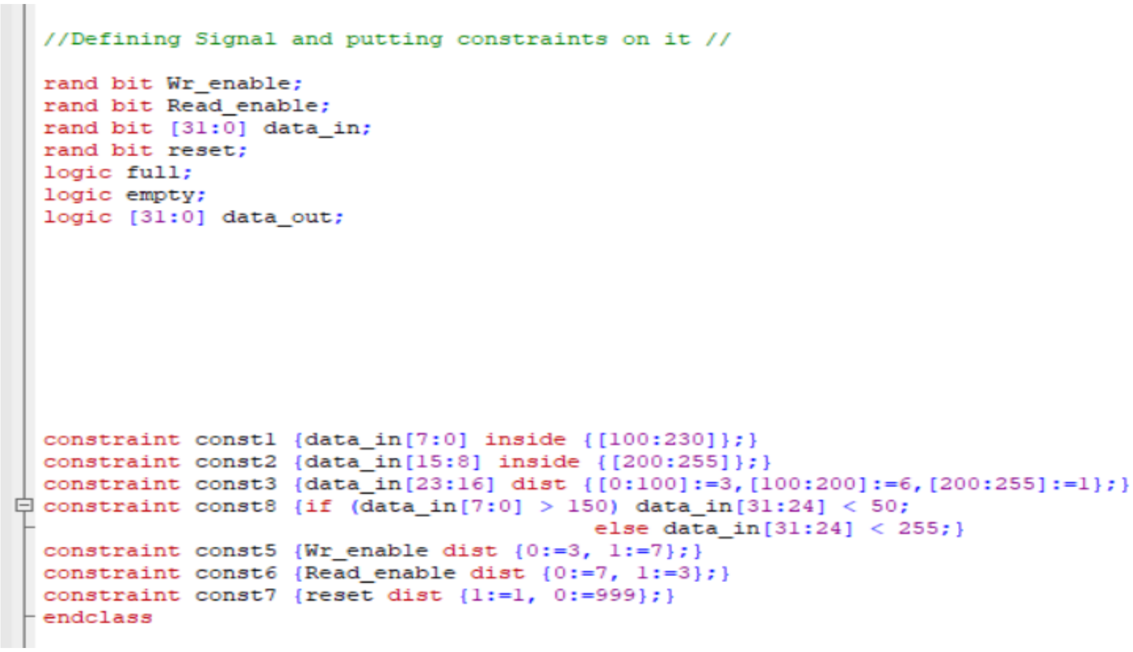
In this project we will verify FIFO using full UVM environment using QuestaSim applying to it given constraints and doing randomization for 80 consecutive sequences then applying coverage on both signals full & empty also doing assertion on write pointer to check that it is incremented right , also we made an interface using two modports and clocking block active on negedge of the original clock to avoid racing conditions

Interface:



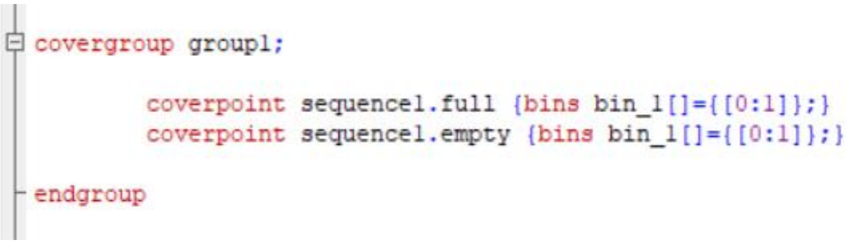
```
//creating interface between DUT & UVM Environment

interface intf1 (input clk);
logic reset;
logic Wr_enable;
logic Read_enable;
logic full;
logic empty;
logic [31:0] data_in;
logic [31:0] data_out;

clocking cb @(negedge clk);
default input #1 output #0;

output reset;
output Wr_enable;
output Read_enable;
output data_in;
input  data_out;
input full;
input empty;
endclocking

modport in_FIFO (input clk ,input reset,input Wr_enable, input Read_enable,input data_in , output full , output empty ,output data_out);
modport in_tb (clocking cb,input clk);



endinterface
```

Constraints:



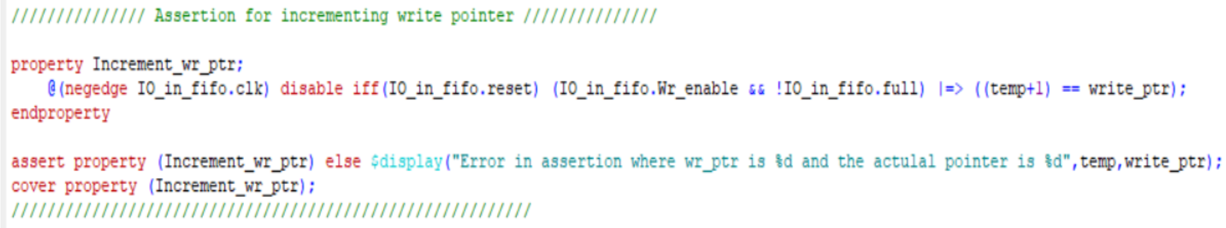
```

//Defining Signal and putting constraints on it //

rand bit Wr_enable;
rand bit Read_enable;
rand bit [31:0] data_in;
rand bit reset;
logic full;
logic empty;
logic [31:0] data_out;









constraint const1 {data_in[7:0] inside {[100:230]};}
constraint const2 {data_in[15:8] inside {[200:255]};}
constraint const3 {data_in[23:16] dist {[0:100]:=3,[100:200]:=6,[200:255]:=1};}
constraint const8 {if (data_in[7:0] > 150) data_in[31:24] < 50;
                                        else data_in[31:24] < 255;}
constraint const5 {Wr_enable dist {0:=3, 1:=7};}
constraint const6 {Read_enable dist {0:=7, 1:=3};}
constraint const7 {reset dist {1:=1, 0:=999};}
endclass
```

Covergroup:



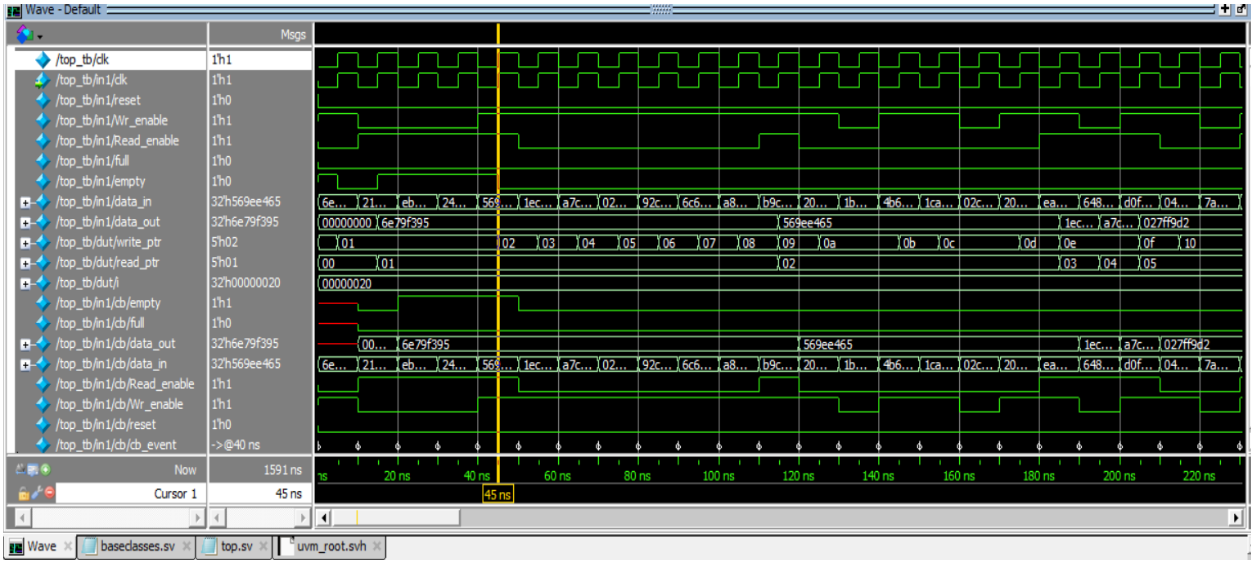
```
covergroup group1;

        coverpoint sequence1.full {bins bin_1[]={[0:1]};}
        coverpoint sequence1.empty {bins bin_1[]={[0:1]};}

endgroup
```

Assertion:



```
/////////////// Assertion for incrementing write pointer ///////////////

property Increment_wr_ptr;
    @(negedge IO_in_fifo.clk) disable iff(IO_in_fifo.reset) (IO_in_fifo.Wr_enable && !IO_in_fifo.full) |=> ((temp+1) == write_ptr);
endproperty

assert property (Increment_wr_ptr) else $display("Error in assertion where wr_ptr is %d and the actulal pointer is %d",temp,write_ptr);
cover property (Increment_wr_ptr);
/////////////////////////////////////////////////////////
```

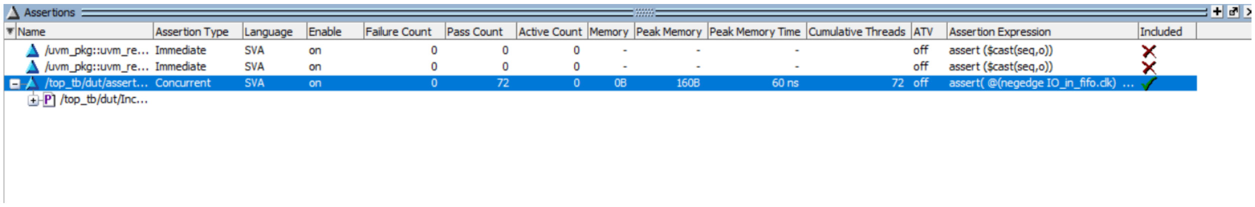
Waveform:



```
Wave - Default
                                Msgs
/top_tb/clk                     1'h1
/top_tb/in1/clk                 1'h1
/top_tb/in1/reset               1'h0
/top_tb/in1/Wr_enable           1'h1
/top_tb/in1/Read_enable         1'h1
/top_tb/in1/full                1'h0
/top_tb/in1/empty               1'h0
/top_tb/in1/data_in             32'h569ee465
/top_tb/in1/data_out            32'h6e79f395
/top_tb/dut/write_ptr           5'h02
/top_tb/dut/read_ptr            5'h01
/top_tb/dut/i                   32'h00000020
/top_tb/in1/cb/empty            1'h1
/top_tb/in1/cb/full             1'h0
/top_tb/in1/cb/data_out         32'h6e79f395
/top_tb/in1/cb/data_in          32'h569ee465
/top_tb/in1/cb/Read_enable      1'h1
/top_tb/in1/cb/Wr_enable        1'h1
/top_tb/in1/cb/reset            1'h0
/top_tb/in1/cb/cb_event         ->@40 ns
Now                             1591 ns
Cursor 1                        45 ns
```

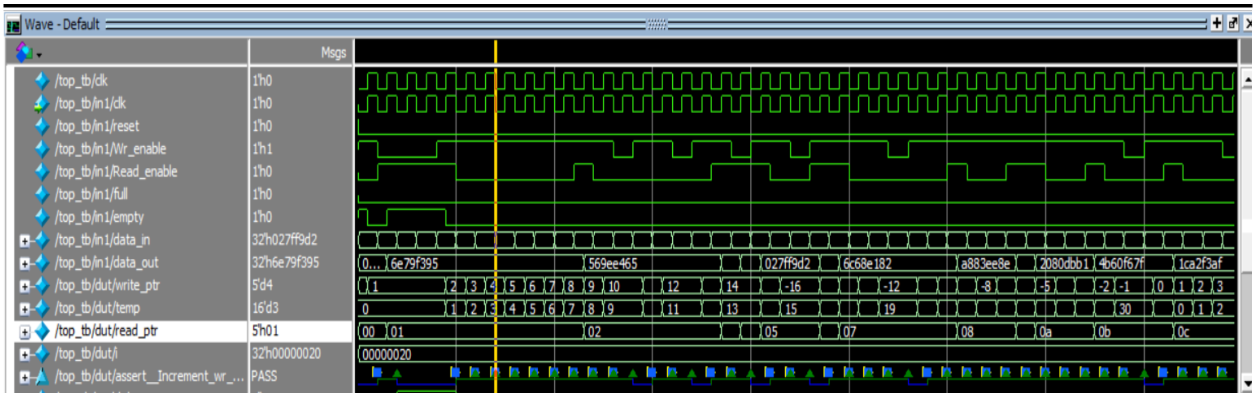
6e... 21... eb... 24... 569... 1ec... a7c... 02... 92c... 6c6... a8... b9c... 20... 1b... 4b6... 1ca... 02c... 20... ea... 648... d0f... 04... 7a...
00000000 6e79f395 569ee465 1ec... a7c... 027ff9d2
01 02 03 04 05 06 07 08 09 0a 0b 0c 0d 0e 0f 10
00 01 02 03 04 05
00000020
00... 6e79f395 569ee465 1ec... a7c... 027ff9d2
ns 20 ns 40 ns 60 ns 80 ns 100 ns 120 ns 140 ns 160 ns 180 ns 200 ns 220 ns
45 ns
Wave
baseclasses.sv
top.sv
uvm_root.svh

Assertion wave and its coverage:



Assertions

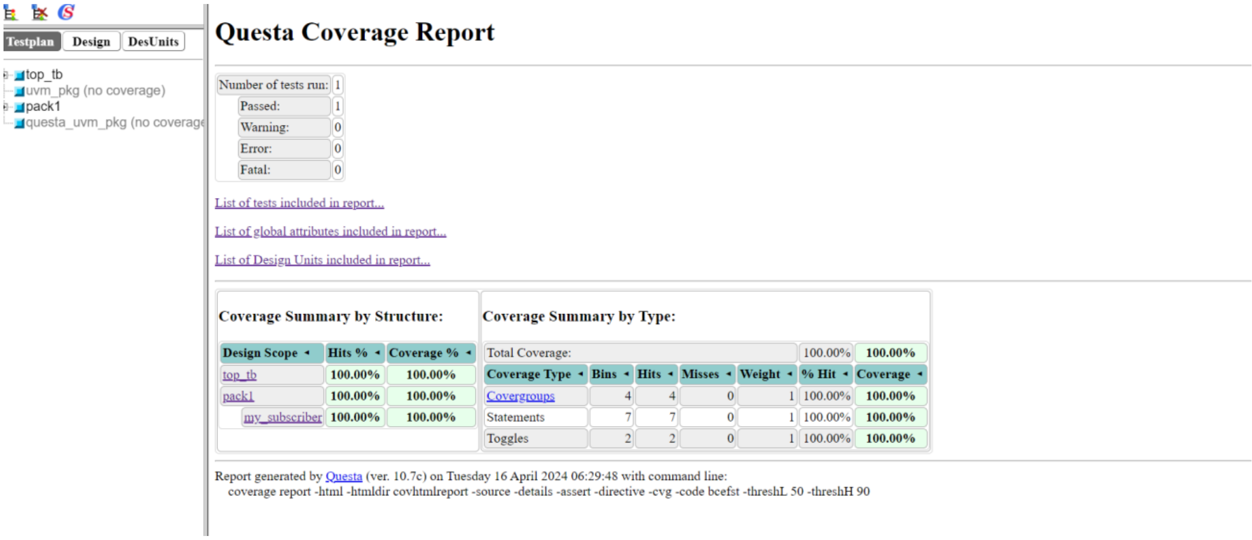
Name	Assertion Type	Language	Enable	Failure Count	Pass Count	Active Count	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	ATV	Assertion Expression	Included
/uvm_pkg::uvm_re…	Immediate	SVA	on	0	0	0	-	-	-		off	assert ($cast(seq,o))	✗
/uvm_pkg::uvm_re…	Immediate	SVA	on	0	0	0	-	-	-		off	assert ($cast(seq,o))	✗
/top_tb/dut/assert…	Concurrent	SVA	on	0	72	0	0B	160B	60 ns	72	off	assert(@(negedge IO_in_fifo.clk) …	✓
P /top_tb/dut/Inc…													



Wave - Default

	Msgs
/top_tb/clk	1'h0
/top_tb/in1/clk	1'h0
/top_tb/in1/reset	1'h0
/top_tb/in1/Wr_enable	1'h1
/top_tb/in1/Read_enable	1'h0
/top_tb/in1/full	1'h0
/top_tb/in1/empty	1'h0
/top_tb/in1/data_in	32'h027ff9d2
/top_tb/in1/data_out	32'h6e79f395
/top_tb/dut/write_ptr	5'd4
/top_tb/dut/temp	16'd3
/top_tb/dut/read_ptr	5'h01
/top_tb/dut/i	32'h00000020
/top_tb/dut/assert__Increment_wr_…	PASS

Coverage reports:



Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
top_tb	100.00%	100.00%
pack1	100.00%	100.00%
my_subscriber	100.00%	100.00%

Coverage Summary by Type:

Total Coverage:					100.00%	100.00%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	4	4	0	1	100.00%	100.00%
Statements	7	7	0	1	100.00%	100.00%
Toggles	2	2	0	1	100.00%	100.00%

Report generated by Questa (ver. 10.7c) on Tuesday 16 April 2024 06:29:48 with command line:

```
    coverage report -html -htmldir covhtmlreport -source -details -assert -directive -cvg -code bcefst -threshL 50 -threshH 90
```