

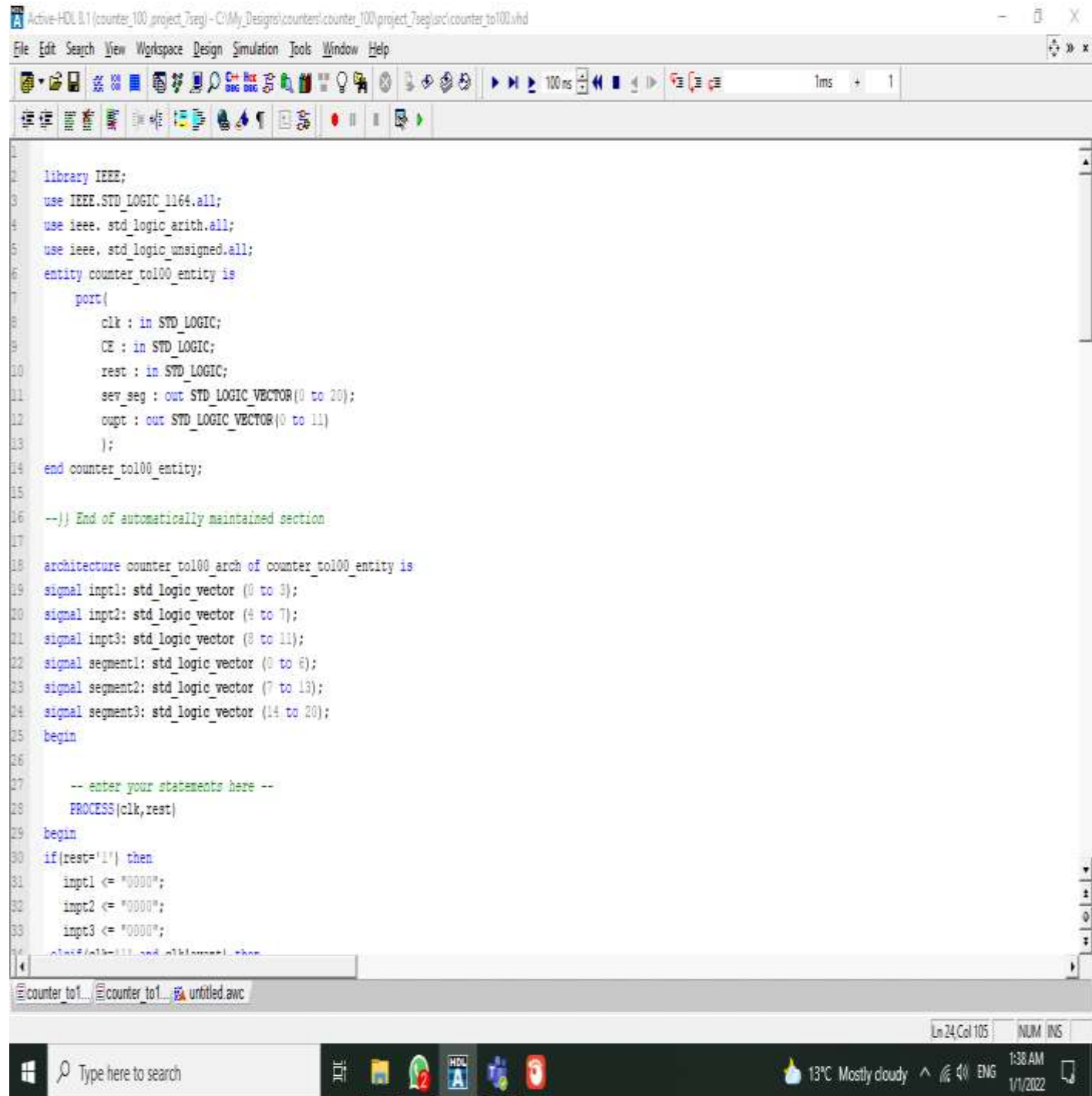
Course : Digital Systems

Project: counting from 0 to 100

Using 7_segment

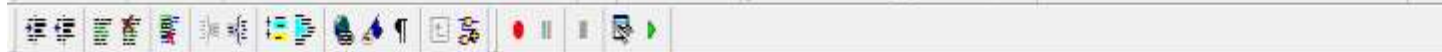
Name :Mohamed Ahmed Zaki Ahmed

Section : (5)



Active-HDL 8.1 (counter_100_project_7seg) - C:\My_Designs\counters\counter_100\project_7seg\src\counter_to100.vhd

File Edit Search View Workspace Design Simulation Tools Window Help

 100 ns 1ms 1

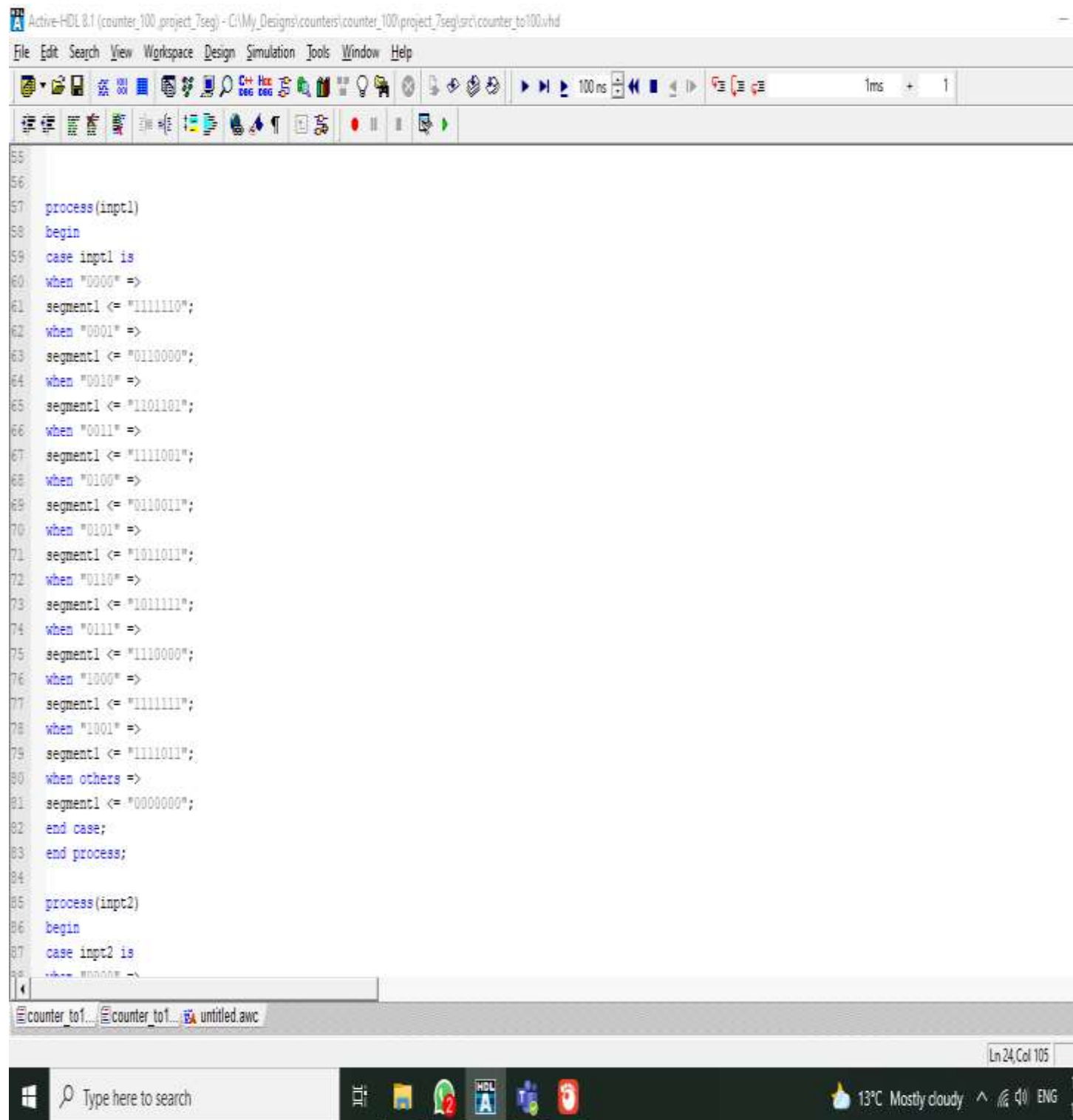
```
25 begin
26
27     -- enter your statements here --
28     PROCESS(clk,rest)
29     begin
30     if(rest='1') then
31         inpt1 <= "0000";
32         inpt2 <= "0000";
33         inpt3 <= "0000";
34     elsif(clk='1' and clk'event) then
35         if(CE='1')then
36             if(inpt1="1001" and inpt2="1001") then
37                 inpt1 <= "0000";
38                 inpt2 <= "0000";
39                 inpt3 <= inpt3 + 1;
40                 elsif(inpt3 = "0001") then
41                     inpt1 <= "0000";
42                     inpt2 <= "0000";
43                     inpt3 <= "0000";
44                 elsif(inpt1="1001")then
45                     inpt1 <= "0000";
46                     inpt2 <= inpt2 + 1;
47                 else
48                     inpt1 <= inpt1 + 1;
49
50             end if;
51         end if;
52     end if;
53     end PROCESS;
54
55
56
57 process(inpt1)
58 begin
```

counter_to1... counter_to1... untitled.awc

Type here to search



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Active-HDL 8.1 (counter_100_project_7seg) - C:\My_Designs\counters\counter_100\project_7seg\src\counter_to100.vhd

File Edit Search View Workspace Design Simulation Tools Window Help

1ms + 1

```
85 process(inpt2)
86 begin
87 case inpt2 is
88 when "0000" =>
89 segment2 <= "1111110";
90 when "0001" =>
91 segment2 <= "0110000";
92 when "0010" =>
93 segment2 <= "1101101";
94 when "0011" =>
95 segment2 <= "1111001";
96 when "0100" =>
97 segment2 <= "0110011";
98 when "0101" =>
99 segment2 <= "1011011";
100 when "0110" =>
101 segment2 <= "1011111";
102 when "0111" =>
103 segment2 <= "1110000";
104 when "1000" =>
105 segment2 <= "1111111";
106 when "1001" =>
107 segment2 <= "1111011";
108 when others =>
109 segment2 <= "0000000";
110 end case;
111
112 end process;
113
114
115 process(inpt3)
116 begin
117 case inpt3 is
118 when "0000" =>
```

counter_to1... counter_to1... untitled.awc

Ln 24 Col 105 NUM INS

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Active-HDL 8.1 (counter_100_project_7seg) - C:\My_Designs\counters\counter_100\project_7seg\src\counter_to100.vhd

File Edit Search View Workspace Design Simulation Tools Window Help

1ms + 1

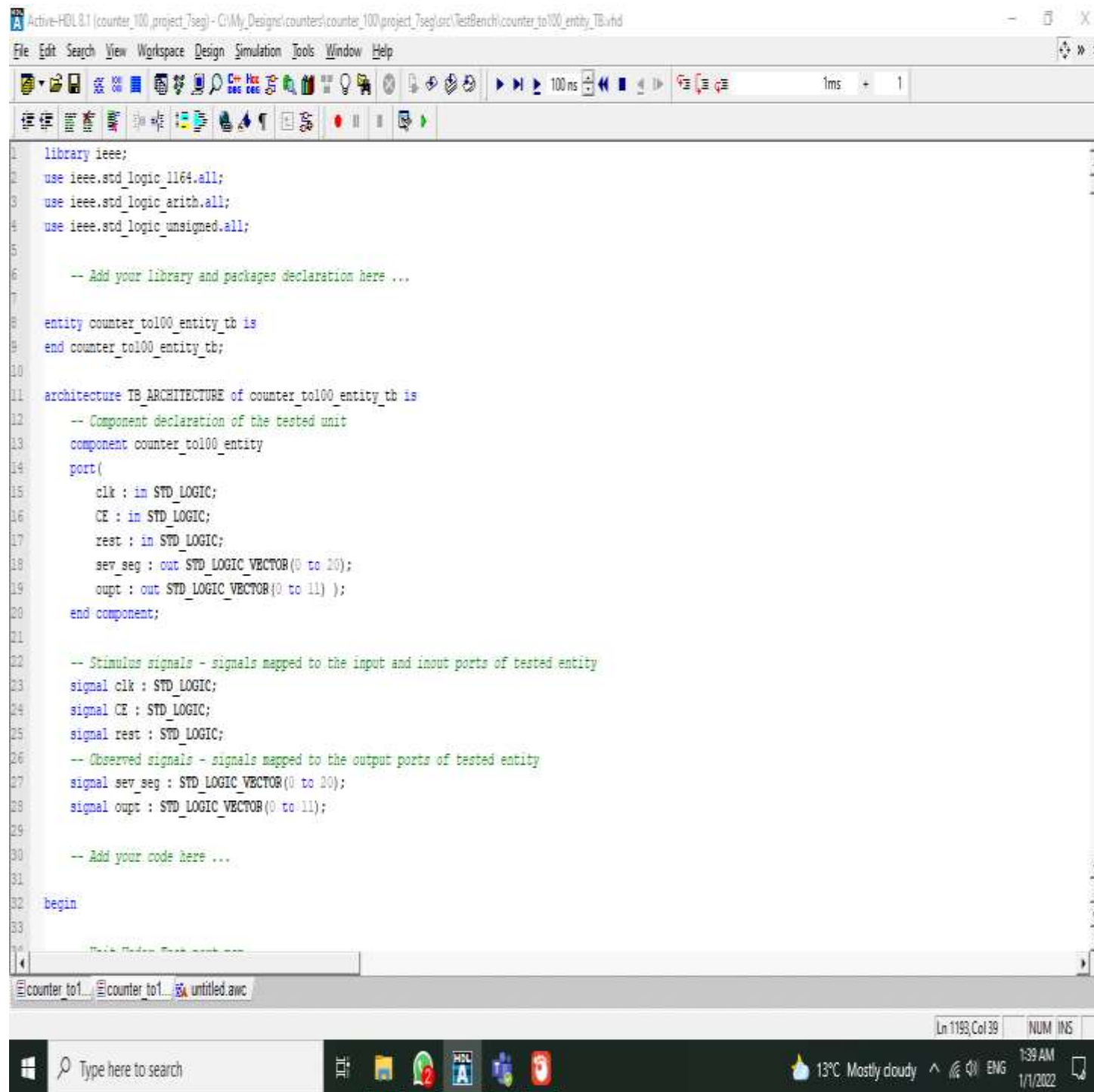
```
102 when "0111" =>
103     segment2 <= "11110000";
104 when "1000" =>
105     segment2 <= "11111111";
106 when "1001" =>
107     segment2 <= "11110111";
108 when others =>
109     segment2 <= "00000000";
110 end case;
111
112 end process;
113
114
115 process(inp3)
116 begin
117     case inp3 is
118     when "0000" =>
119         segment3 <= "11111110";
120     when "0001" =>
121         segment3 <= "01110000";
122     when others =>
123         segment3 <= "00000000";
124     end case;
125
126 end process;
127
128 oupt <= inp3 & (inp2 & inp1);
129 sev_seg <= segment3 & | segment2 & segment1;
130
131
132 end counter_to100_arch;
133
134
```

@counter_to1... @counter_to1... untitled.awc

Ln 24, Col 105 NUM INS

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The screenshot shows the Active-HDL 8.1 IDE with a VHDL testbench file named `counter_to100_entity_TB.vhd`. The code is as follows:

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_arith.all;
4  use ieee.std_logic_unsigned.all;
5
6  -- Add your library and packages declaration here ...
7
8  entity counter_to100_entity_tb is
9  end counter_to100_entity_tb;
10
11 architecture TB_ARCHITECTURE of counter_to100_entity_tb is
12     -- Component declaration of the tested unit
13     component counter_to100_entity
14     port(
15         clk : in STD_LOGIC;
16         CE : in STD_LOGIC;
17         rest : in STD_LOGIC;
18         sev_seg : out STD_LOGIC_VECTOR(0 to 20);
19         oupt : out STD_LOGIC_VECTOR(0 to 11) );
20     end component;
21
22     -- Stimulus signals - signals mapped to the input and input ports of tested entity
23     signal clk : STD_LOGIC;
24     signal CE : STD_LOGIC;
25     signal rest : STD_LOGIC;
26
27     -- Observed signals - signals mapped to the output ports of tested entity
28     signal sev_seg : STD_LOGIC_VECTOR(0 to 20);
29     signal oupt : STD_LOGIC_VECTOR(0 to 11);
30
31     -- Add your code here ...
32
33 begin
```

The IDE interface includes a menu bar (File, Edit, Search, View, Workspace, Design, Simulation, Tools, Window, Help), a toolbar with various icons, and a status bar at the bottom showing the current line and column (Ln 1193, Col 39) and the number of instances (NUM INS).

Active-HDL 8.1 (counter_100/project_7seg) - C:\My_Designs\counters\counter_100\project_7seg\src\TestBench\counter_to100_entity_TB.vhd

File Edit Search View Workspace Design Simulation Tools Window Help

1ms + 1

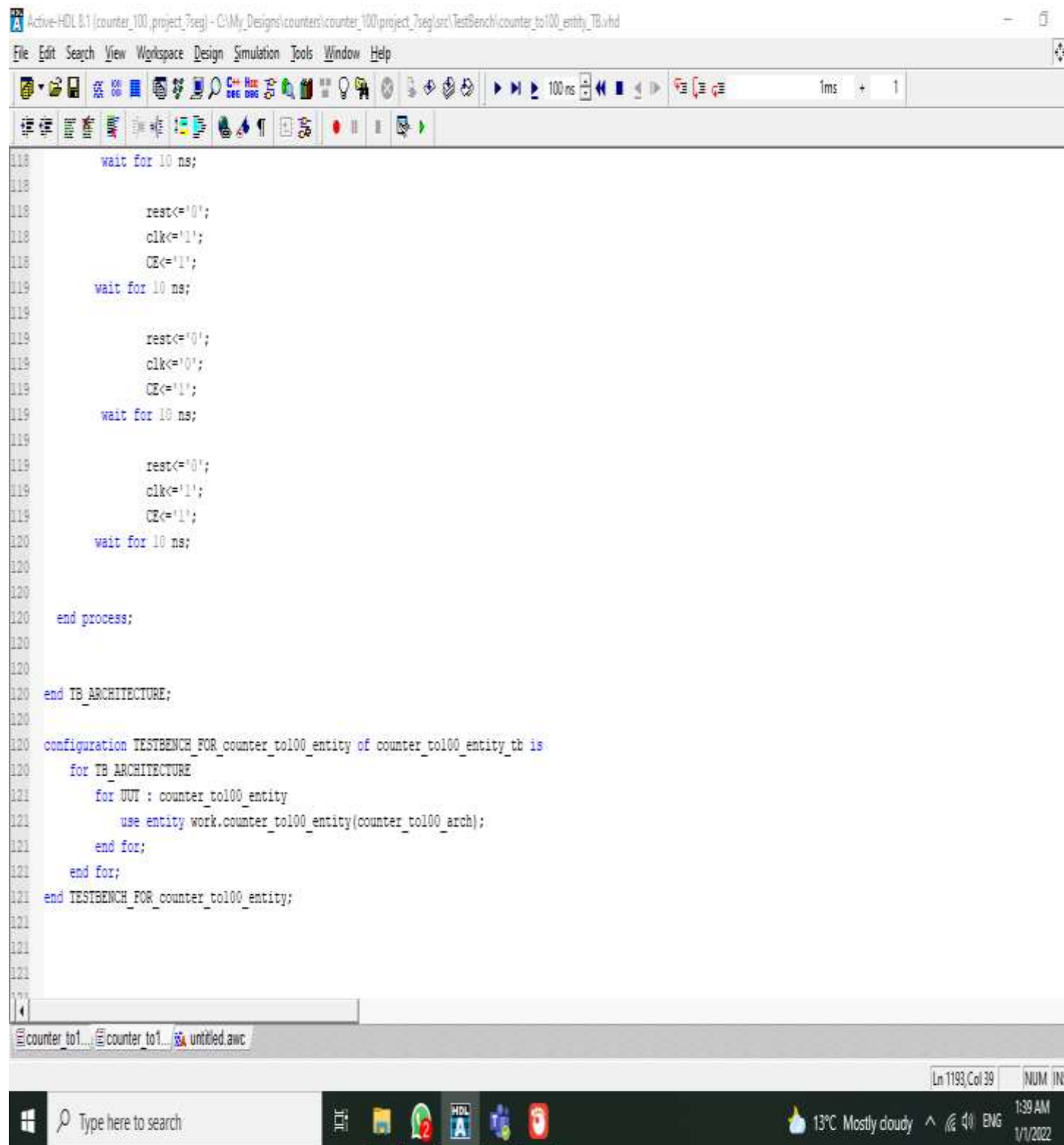
```
31
32 begin
33
34     -- Unit Under Test port map
35     UUT : counter_to100_entity
36         port map (
37             clk => clk,
38             CE => CE,
39             rest => rest,
40             sev_seg => sev_seg,
41             oupt => oupt
42         );
43
44     -- Add your stimulus here ...
45
46
47     process
48     begin
49         rest<='1';
50         clk<='-' ;
51         CE<='-' ;
52         wait for 10 ns;
53
54         rest<='0';
55         clk<='0';
56         CE<='1';
57         wait for 10 ns;
58
59         rest<='0';
60         clk<='1';
61         CE<='1';
62         wait for 10 ns;
63
64         rest<='1';
```

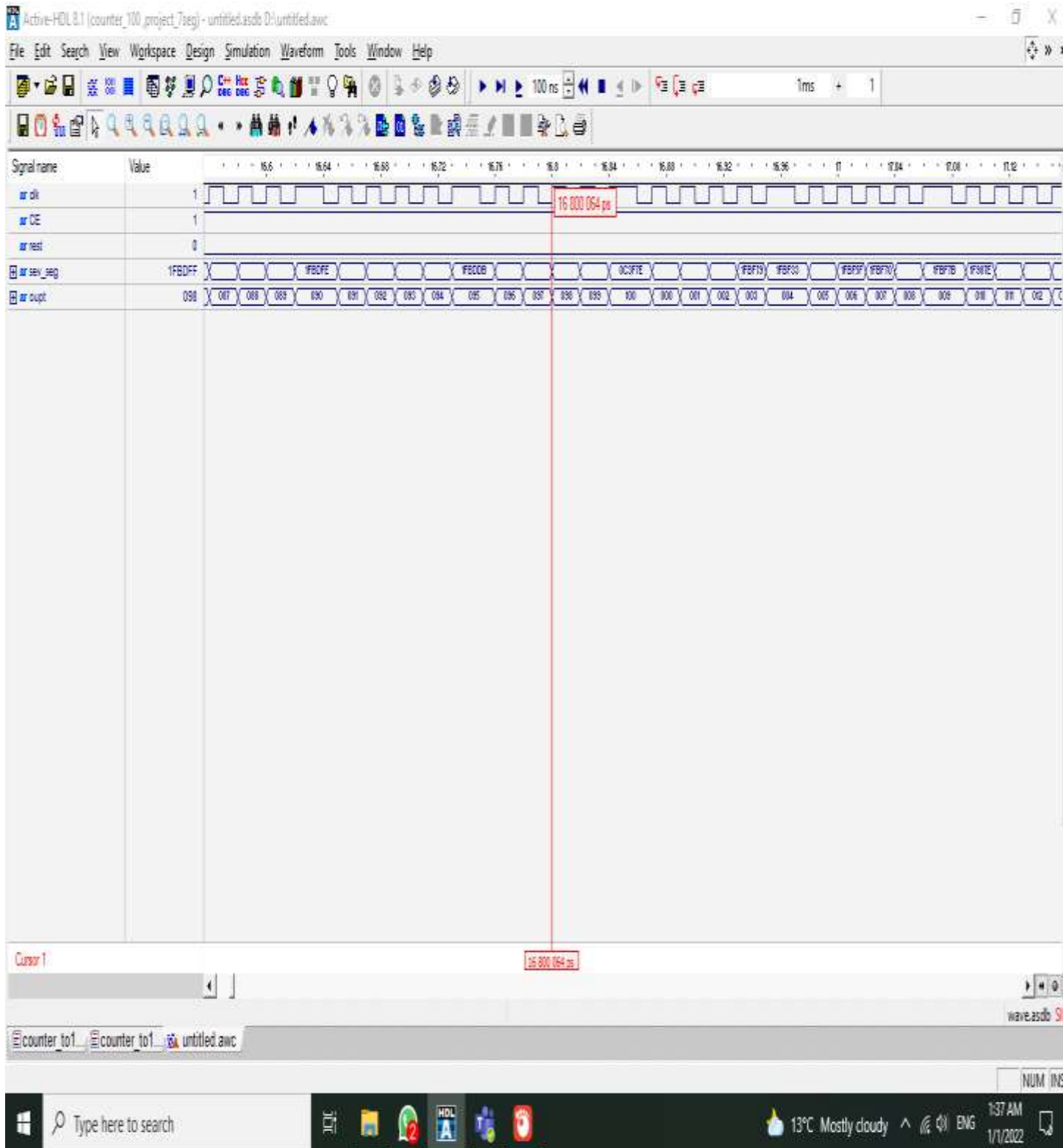
counter_to1... counter_to1... untitled.awc

Ln 1193, Col 39 NUM INS

Type here to search

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Active-HDL 8.1 (counter_100.project_7seg) - untitled.asdb D:\untitled.awc

File Edit Search View Workspace Design Simulation Waveform Tools Window Help

100 ns 1ms 1

Design Browser

counter_to100_entity_tb

Unsorted

Workspace 'counter_1'

counter_100

project_7seg

myproject

project_7seg

Add New File

counter_to100.vhd

counter_to100_e

untitled.asdb

untitled.awc

TestBench

counter_to100_e

counter_to1

testbench_for

counter_to100_e

Add New Library

project_7seg library

Files Stru... Res...

Signal name Value

16.72 16.76 16.8 16.84 16.88 16.92 16.96 17 17.04 17.08 17.12 17.16 17.2

ar ck 1

ar CE 1

ar rest 0

ar sev_seg 1FBF33 1FB00B 0C3F1E 1FBF33 1FBF7D 1FBF1B 1FB01E 1FB07D 1FB033

ar oust 004 004 005 006 007 008 009 00A 00B 00C 00D 00E 00F 010 011 012 013 014

Cursor 1 16.954646 ns

wave.asdb SM

counter_to1 counter_to100 untitled.awc

Console

```

> # Selected Top-Level: counter_to100_entity_tb (tb_architecture)
> # 5 signal(s) traced.
> run @1ms
> # KERNEL: stopped at time: 1 ms
> # Adding file C:\My_Designs\counters\counter_100\project_7seg\src\untitled.asdb ... Done
> # Adding file D:\untitled.awc ... Done
> # Error: ELAB1_0028: countb0d_TB.vhd : (35, 0): Entity port length is 21. Output length is 8.

```