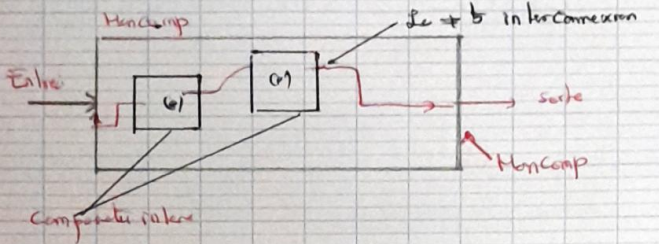
# 6] Description Structurelle en VHDL :

* Il s'agit d'écrire en VHDL la description de la strate du schéma Cirait.

*

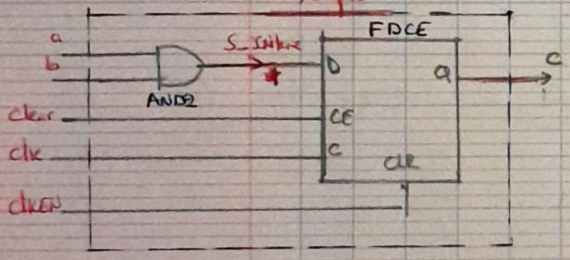



* La description structurelle en VHDL permet : d'écrire un fichier de tests.

* → entity : Pour la description externe de : MonComp
  → component : Pour la description des + bs composants internes
  → Port map : Pour la description des + bs interconnexions

} architecture (la description interne)

Exemple :




VHDL : monCompe.vhd :

```
Library IEEE;
use ieee.std_logic_1164.ALL;
use ieee.numeric_std.ALL;

entity monComp is
    Port ( a : in std_logic;
           b : in std_logic;
           clear : in std_logic;
           clk : in std_logic;
           clkEn in std_logic;
           c : out std_logic));

end monComp ;

architecture structurelle of monComp is
    Signal INterne : std_logic;
Component AND2
    port ( I0 : in std_logic;
           I1 in std_logic;
           O : out std_logic));
end component;

Component FDCE
    generic ( INIT : bit := '0' );
    port ( C : in std_logic;
           CE : in std_logic;
           CLR : in std_logic;
           D : in std_logic;
           Q : out std_logic );
end component;
begin
    XLXI_1 : AND2
    port map ( I0 => b,
               I1 => a,
               O => INterne);
    XLXI_2 : FDCE
    port map ( C => clk,
               CE => clkEn,
               CLR => clear,
               D => Interne
               Q => c );
end monComp;
```