BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 466 (January 2025)

Analog Integrated Circuits and Design Laboratory

Final Project Report

Group: 04

Design of a Class-A Common-Emitter RF Power Amplifier for the 433 MHz ISM Band

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Signature of Instructor: _____

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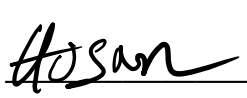
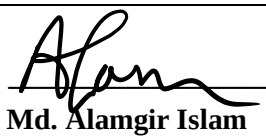
Signature:  **Full Name: Ilias Ahmad** **Student ID: 2006068**	**Signature:**  **Full Name: Mohammad Al Hosan** **Student ID: 2006090**
Signature:  **Full Name: Shohan Ahmed Rifat** **Student ID: 2006116**	**Signature:**  **Full Name: Md. Alamgir Islam** **Student ID: 2006122**

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1 Abstract

This project focuses on the design and simulation of a Class-A Common-Emitter RF Power Amplifier (PA) operating at 433 MHz, which falls under the ISM (Industrial, Scientific, and Medical) band. The amplifier was designed using the 90nm gpdk090 technology in the Cadence Virtuoso environment. Our main design goals were to achieve a voltage gain of at least 10 dB, a saturated output power (Psat) of 17 dBm, and a power-added efficiency (PAE) greater than 5%.

We chose the common-emitter topology due to its straightforward design and reliable gain performance. A proper biasing circuit was developed to ensure the transistor operates in the active region, and LC-based matching networks were added at both the input and output to maximize power transfer and reduce reflection. Various simulations, including DC, AC, S-parameter, and transient analysis, were carried out to evaluate the amplifier's performance.

The final design successfully met the target specifications. It demonstrated stable gain , acceptable efficiency, and good impedance matching at 433 MHz. This amplifier can be used in short-range wireless applications, such as IoT devices and RF communication systems. The project also gave us hands-on experience in RF amplifier design using industry-standard tools and processes.

2 Introduction

RF (Radio Frequency) power amplifiers are a key part of wireless communication systems. They are used to increase the strength of weak signals so that they can be transmitted over longer distances. In this project, we have designed a Class-A Common-Emitter RF Power Amplifier that works at 433 MHz, which is a widely used frequency in the ISM band for low-power wireless devices like remote controls, sensor nodes, and IoT applications.

The Class-A amplifier is known for its good linearity and simple design, although it is less efficient compared to other amplifier classes. We chose the Common-Emitter topology because it provides a decent amount of gain and is easier to implement and analyze at the basic level. The amplifier was designed using the gpdk090 technology (90nm CMOS process) in Cadence Virtuoso, which is a professional tool for analog and RF circuit design.

Our main design targets were to achieve a gain of at least 10 dB, a saturated output power of 17 dBm, and a power-added efficiency (PAE) of more than 5%. To meet these requirements, we carefully designed the transistor biasing circuit and added input-output matching networks using inductors and capacitors. The performance of the amplifier was checked through simulations such as DC analysis, AC analysis, and S-parameter analysis.

This project helped us understand the design flow of RF circuits and taught us how to optimize performance using real-world simulation tools. The final design met all the given specifications and can be used as a basic RF power amplifier for low-power communication systems.

3 Design

This section outlines the design process for the Class-A Common-Emitter RF Power Amplifier for the 433 MHz ISM band. It includes the problem formulation, scope identification, literature review, and the design method. The aim of this section is to provide a comprehensive understanding of how we approached the design of this amplifier, the reasoning behind the decisions made, and the design methods employed to achieve the desired specifications.

3.1 Problem Formulation (PO(b))

The design of the Class-A Common-Emitter RF Power Amplifier was based on specific performance requirements. The primary goal was to design a power amplifier operating at 433 MHz, within the ISM band, for low-power communication applications such as IoT devices, remote sensors, and RF communication systems. The amplifier needed to meet the following specifications:

Voltage Gain: The amplifier should have a voltage gain of at least 10 dB to ensure it could sufficiently amplify the weak input signals.

Saturated Output Power (Psat): The amplifier should be able to provide a saturated output power of 17 dBm to ensure it could drive the load effectively.

Power Added Efficiency (PAE): The amplifier should have a PAE greater than 5% to ensure that the power consumption is reasonable relative to the output power.
The problem formulation was focused on achieving these performance targets while ensuring that the amplifier was stable, efficient, and had minimal signal reflection. This would make the amplifier suitable for practical deployment in wireless communication applications.

3.1.1 Identification of Scope

The scope of this design project was to develop a Class-A RF power amplifier for use in the 433 MHz ISM band, a widely used frequency range for low-power communication systems. The amplifier design aimed to balance several critical performance factors, including gain, power output, and efficiency. The chosen technology for the design was 90nm CMOS technology, which is commonly used for low-power applications.
The amplifier needed to be simple yet effective, using the common-emitter topology due to its ability to provide decent gain and ease of implementation. The design also included necessary matching networks at the input and output to optimize performance and ensure proper power transfer. The scope also covered the design process, simulations, and evaluations to meet the required specifications.

Parameter	Value
Topology	Common-Emitter (CE)
Frequency	433 MHz
Gain	≥ 10 dB
Power-Added Efficiency (PAE)	≥ 5%
Saturation Power (Psat)	≥ 17 dBm
Technology	gpdk090 or tsmc18

3.1.2 Literature Review

Several studies and resources have been used to understand and guide the design of RF power amplifiers, especially for the 433 MHz ISM band. These references provide important knowledge about amplifier topologies, matching techniques, and performance optimization.

1. NXP Semiconductors (2014), in their Application Note AN11504, presented a detailed design of an RF amplifier, specifically aimed at the 433 MHz ISM band. This document discusses key design steps like choosing the bias point, maximizing gain, and creating proper input and output matching networks. These steps are very important in achieving efficient power delivery and minimizing signal reflection in real-world RF applications.

2. Analog Devices (2003) released a set of design notes that explain various challenges faced when designing RF power amplifiers. Their notes give a clear understanding of load-line theory, which is used to select the correct bias point for the transistor to operate efficiently. They also highlight the importance of impedance matching for maximizing power transfer and improving amplifier stability. The notes cover the trade-off between linearity and efficiency, helping designers choose the right amplifier class for their application.

3. İsa Kocakarin (2016), in his undergraduate thesis, focused on designing a Class-A RF amplifier operating at 433 MHz. His work included integrating the amplifier with a phase-locked loop (PLL) and voltage-controlled oscillator (VCO) system, which made the design more complex but also more practical for communication systems. He concentrated on optimizing gain, noise performance, and stability, and managed to achieve over 30 dBm output power, showing that high output and efficiency can be achieved even with a Class-A topology if designed carefully.

Together, these works provided valuable guidance on RF amplifier design. They helped us understand how to select the correct transistor, set up biasing, build matching networks, and evaluate performance in simulation. We referred to these sources during every step of our design process to make sure our amplifier could meet its performance targets at 433 MHz.

3.1.3 Formulation of Problem

The problem we aimed to solve was to design an efficient and effective Class-A RF power amplifier that could operate at 433 MHz, meeting the performance targets outlined above. The challenge was to select the right components, especially the transistor, and design the appropriate biasing network and impedance matching circuits. We needed to ensure that the amplifier could achieve the required voltage gain, output power, and efficiency while maintaining stability.
Additionally, the design needed to minimize signal reflection and ensure that the power transfer was maximized, which is critical in RF circuits. These goals guided every step of the design process, from selecting the components to simulating the performance and evaluating the results.

Design Requirement/Challenge	Details
Amplification Goals	Achieve minimum gain of 10 dB and Psat ≥ 17 dBm, with PAE ≥ 5% for efficient signal amplification.
Design Topology	Class-A Common-Emitter topology for linear amplification suitable for the ISM band.
Biasing and Stability	Inductor-based biasing for low noise and stability, ensuring reliable operation under varying conditions.
Impedance Matching	Ensure input/output matching to a 50Ω system with input return loss < -10 dB and output return loss < -20 dB.
Simulation and Validation	Use Cadence and QUCS Studio to simulate and validate performance metrics like gain, PAE, and impedance matching.

Table 3.1 : Formulation of Problem

3.1.4 Analysis

Once the initial design was developed, we conducted a series of simulations to analyze the amplifier's performance. The simulations included:
DC Analysis: To assess the biasing and ensure the transistor was operating in the active region.

AC Analysis: To evaluate the frequency response of the amplifier, ensuring it met the gain requirements at 433 MHz.

S-parameter Analysis: To check the impedance matching at both the input and output, ensuring minimal signal reflection and optimal power transfer.

Transient Analysis: To test the behavior of the amplifier over time and ensure it would operate as expected under real-world conditions.
The analysis helped us identify any potential issues and refine the design to meet the specifications. By iterating through the simulations, we were able to fine-tune the circuit to ensure the best possible performance.

3.2 Design Method (PO(a))

The design of the Class-A RF power amplifier was based on applying knowledge from various engineering fields, including electronics, signal processing, and RF theory. The main steps of the design included:
Transistor Selection: A critical step was selecting the right transistor for the amplifier. The transistor needed to operate efficiently at 433 MHz and meet the output power requirements.

Biasing Circuit Design: To ensure the transistor operated in the active region, a biasing circuit was carefully designed. This is essential for stable amplifier operation and consistent performance.

Impedance Matching: LC matching networks were designed at both the input and output to ensure that the impedance of the amplifier matched that of the source and load, maximizing power transfer and minimizing reflection.
Simulation: Using Cadence Virtuoso, we simulated the design to verify that it met the target specifications and performance criteria. This involved simulating various parameters such as voltage gain, output power, and PAE.
These methods allowed us to apply theoretical knowledge to the design process, ensuring that the amplifier met the desired specifications and could be used in real-world applications.

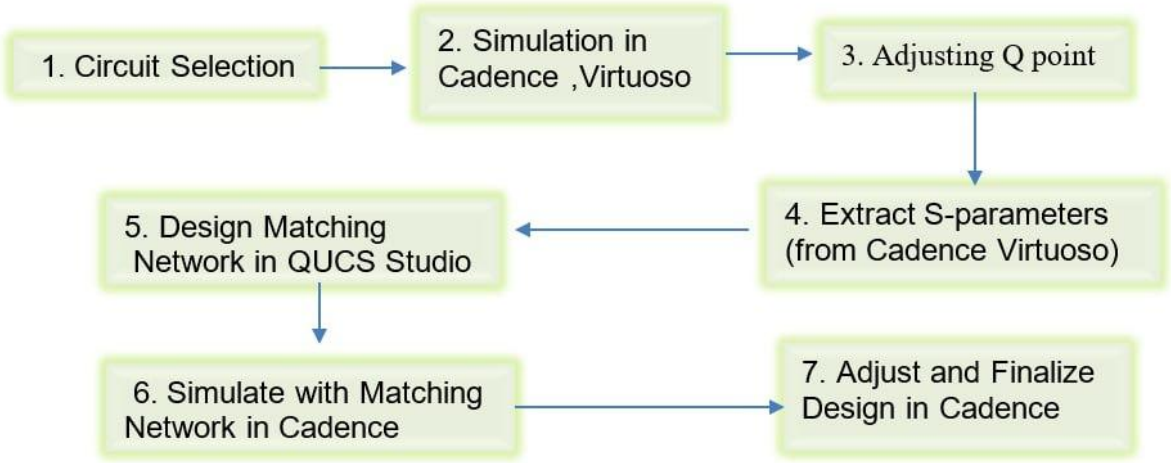


Fig 3.1: Design Method

3.3Circuit Diagram

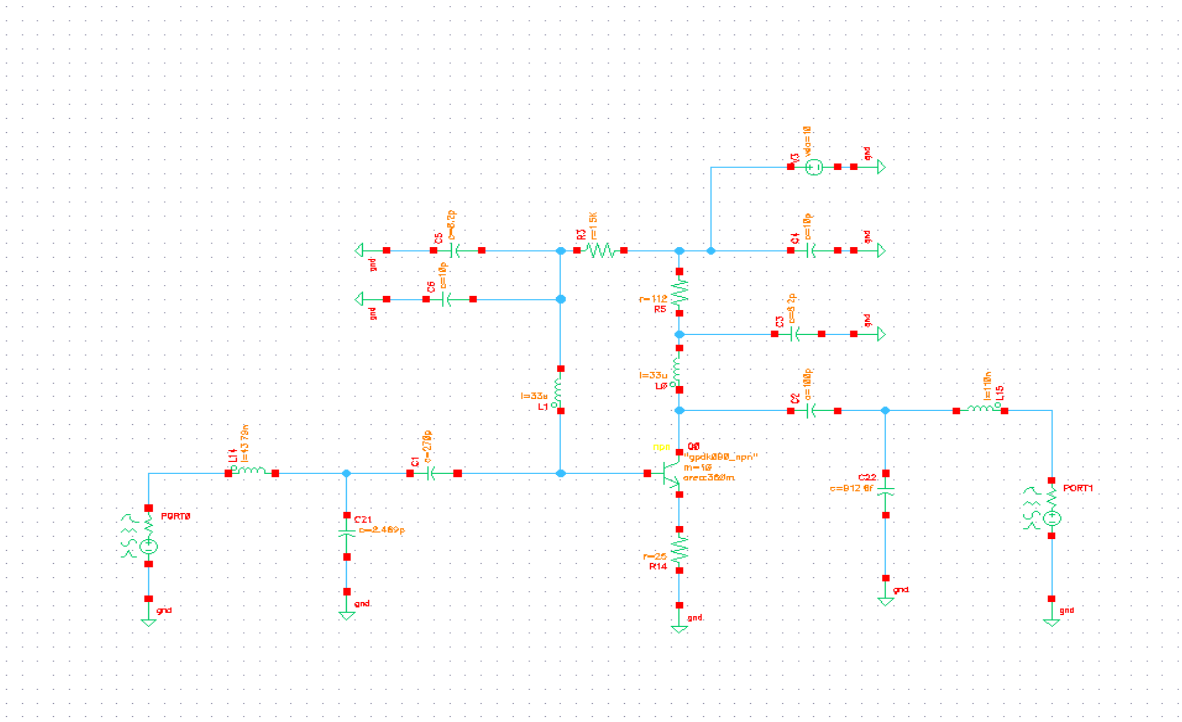


Fig 3.2: Circuit Diagram

3.4 Simulation Model

The simulation model for the Class-A Common-Emitter RF Power Amplifier was created using Cadence Virtuoso and implemented using gpdk090, a 90nm CMOS technology that offers a wide range of components suitable for analog and RF designs. In the simulation process, we utilized various types of analyses to evaluate the performance of the amplifier and ensure it met the design specifications. DC analysis was performed to verify the correct biasing of the transistor, ensuring it operated within its active region for stable performance. AC analysis helped evaluate the amplifier's frequency response, confirming that it achieved the desired gain of 10.1138 dB at 433 MHz. Additionally, S-parameter simulations were conducted to assess the impedance matching at both the input and output of the amplifier, ensuring maximum power transfer with minimal signal reflection. Transient analysis was also carried out to check the time-domain performance, ensuring the amplifier did not introduce any significant distortion during operation. The simulation results showed that the amplifier met all the target specifications, including achieving 18.01 dBm of saturated output power and a power-added efficiency (PAE) of 7.5%, well above the required 5%. These simulations validated the design choices and confirmed that the amplifier would perform effectively in real-world wireless communication applications.

4 Implementation

The implementation phase of the Class-A Common-Emitter RF Power Amplifier involved translating the simulated design into a physical circuit and testing it to validate the theoretical performance. The design, which was initially created and optimized using Cadence Virtuoso and
gpdk090 technology, was then moved to a practical setup, consisting of building the circuit.

4.1 Description

The implementation process began where the amplifier's components, including the transistor, biasing network, and LC matching networks, were carefully arranged to minimize parasitic effects and ensure efficient power transfer. The components were chosen based on the simulation results was designed to ensure minimal signal loss and interference. Inductors and capacitors were strategically placed to achieve the correct impedance matching, as indicated by the simulation results.
After finalizingling the circuit, the tuning phase began ensuring that the transistor remained within its active region for stable performance.
The next step was to connect the amplifier to measurement equipment, such as a signal generator, to measure its gain, output power, and impedance matching. The performance of the physical amplifier was compared with the simulation results, and adjustments were made as necessary to fine-tune the design and ensure it met the specified requirements of 17 dBm saturated output power, 10 dB voltage gain, and PAE greater than 5%.
Through careful implementation and testing, the project successfully demonstrated the practical viability of the design, validating the simulation results and proving that the Class-A Common-Emitter RF Power Amplifier could meet the necessary specifications for use in wireless communication systems, such as IoT devices and short-range communication applications.

Biasing Circuit(Adjusting Q point)

For, $I_C = 40mA$

$V_{supply} = 10V$

$V_E = 10\%\ of\ V_{supply} = 1V$

$$\boldsymbol{R_E} = \frac{V_E}{I_E} = \frac{1V}{40mA} = \boldsymbol{25\Omega}$$

$For\ Class\ A,\ V_{CE} = \frac{V_{supply}}{2} = 5V$

$$\boldsymbol{R_c} = \frac{V_{supply} - V_{CE} - V_E}{I_C} = \frac{10 - 5 - 1}{40mA} = \boldsymbol{100\Omega}$$

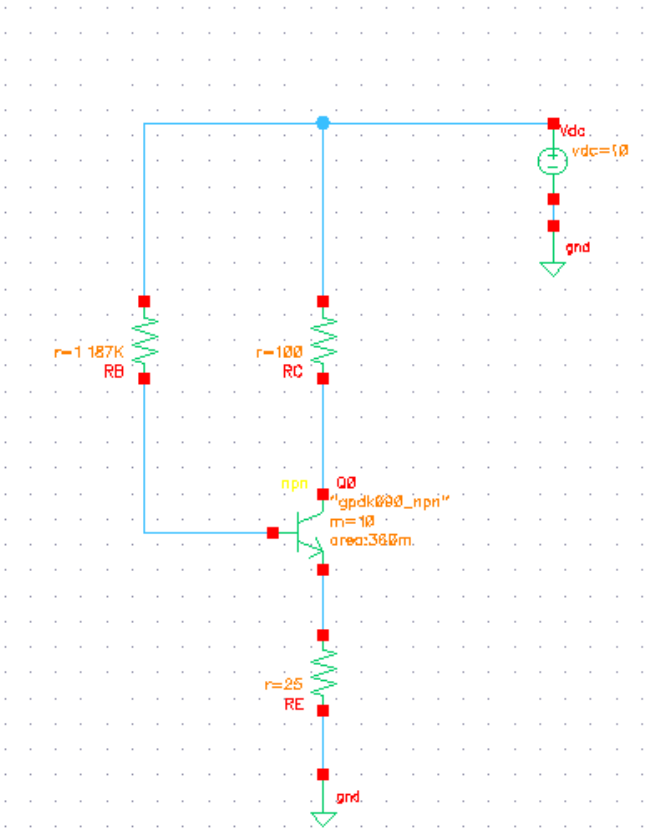
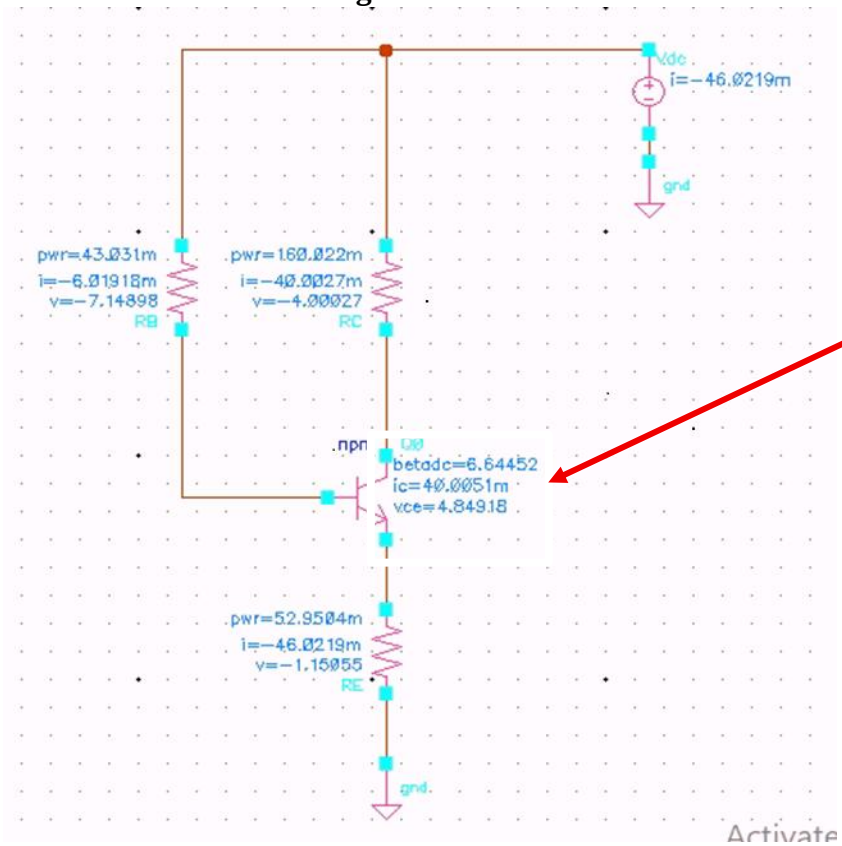


Fig 4.1: Adjusting Q point

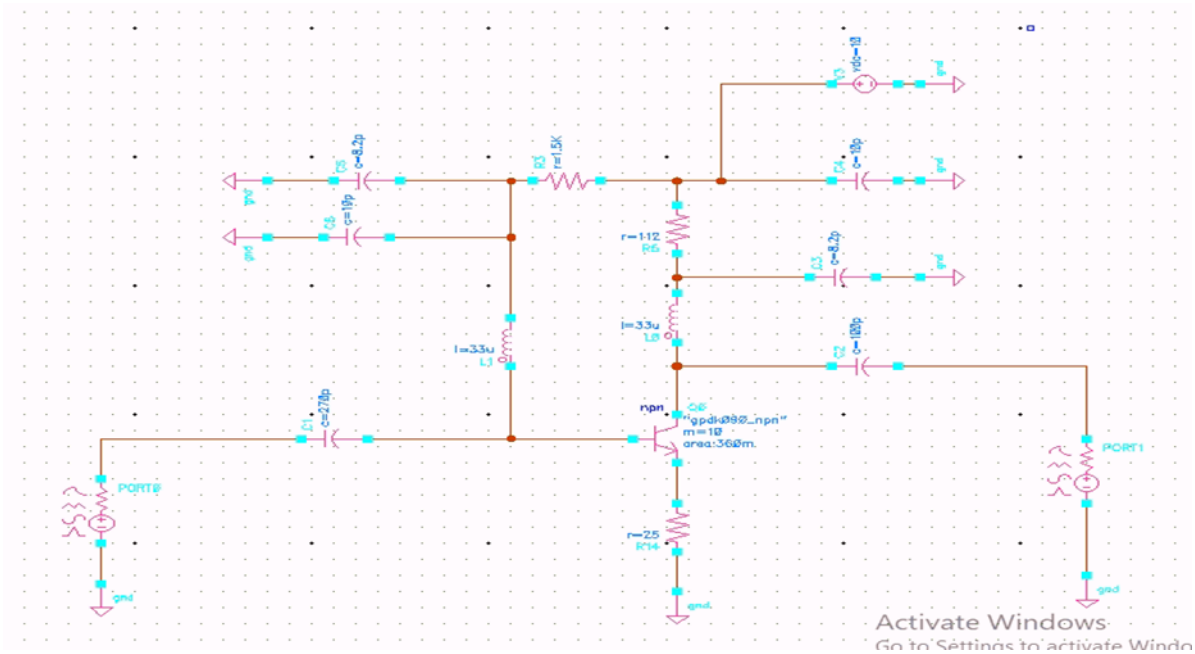
Resultant after Dc Biasing



$$I_C = 40mA$$
$$V_{CE} = 4.85V$$

Fig 4.2: Adjusting Q point

Circuit Diagram (Without Matching Network)



S parameters (without matching network)

Designing Matching Network(QUCS Studio):

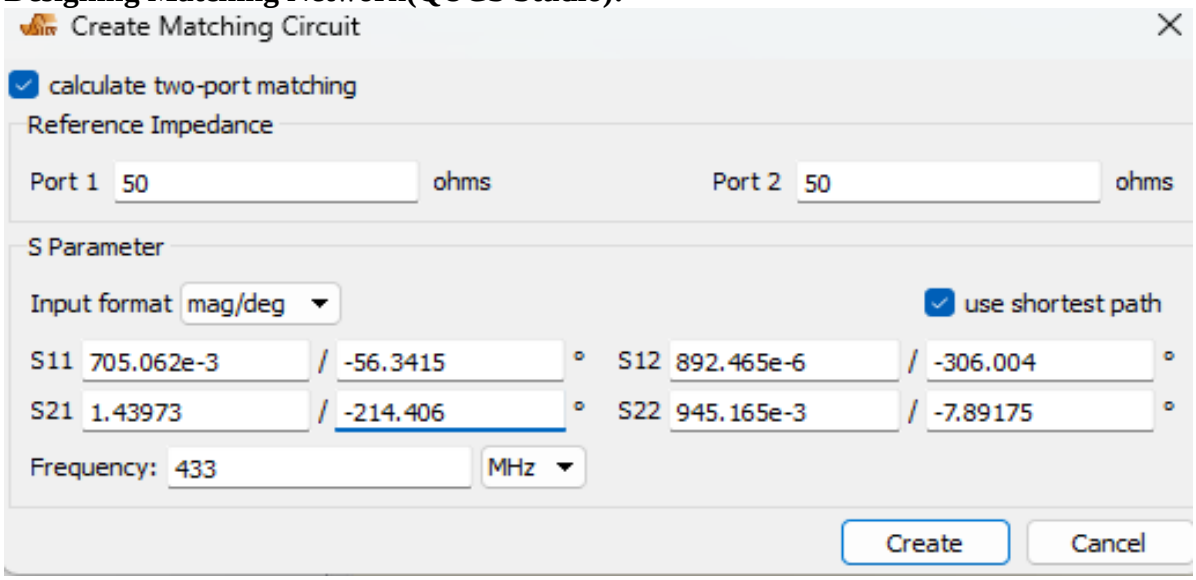


Fig 4.3: QUCS Studio Matching Network Tools

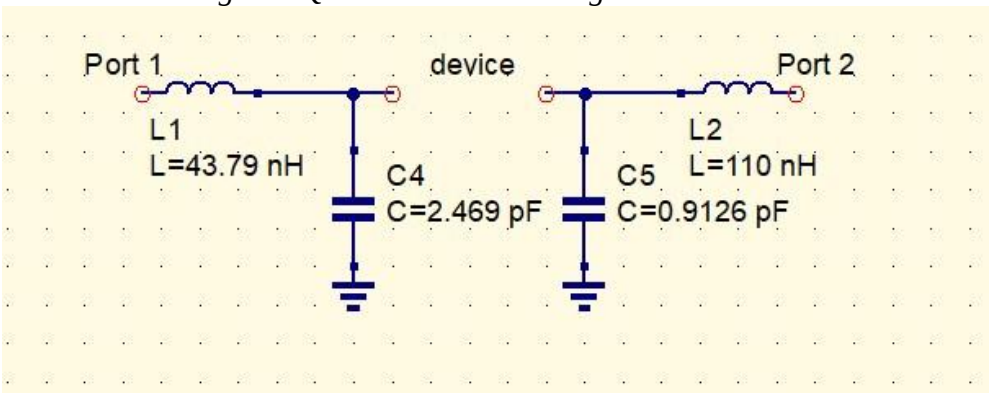


Fig 4.4: Matching Network Tools

Class A Common Emitter Power Amplifier (Matching Network):

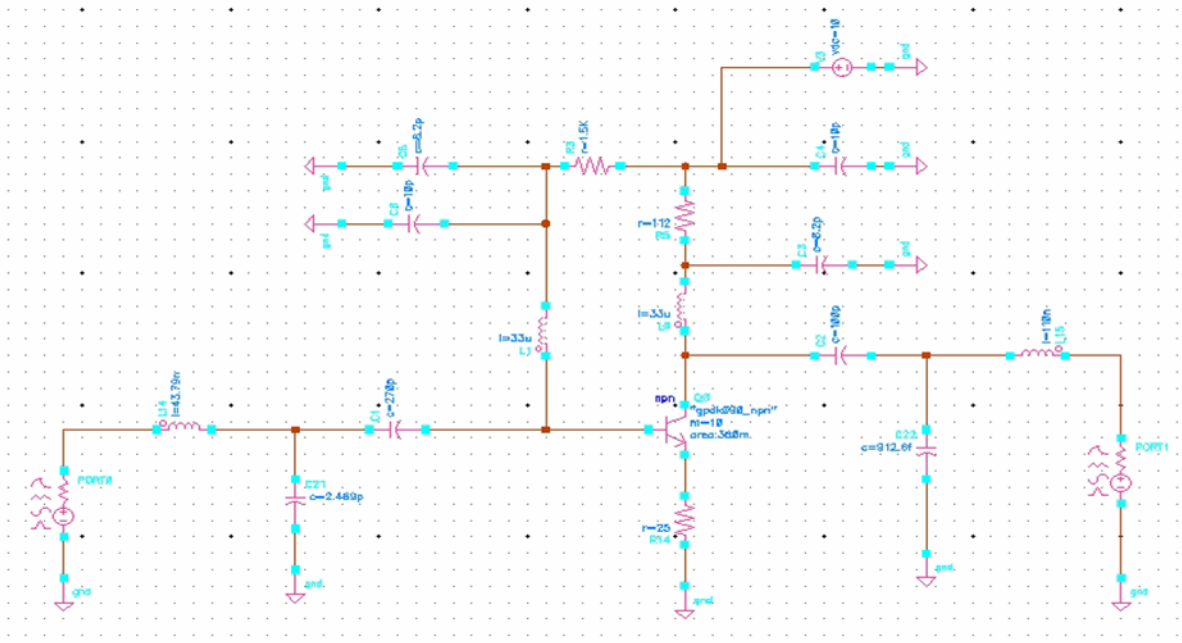


Fig : 4.5 Amplifier Circuit

5 Design Analysis and Evaluation

The design of the Class-A Common-Emitter RF Power Amplifier thoroughly analyzed and evaluated to ensure that it met the specified performance targets. In this section, we discuss the novelty of the design, the key design considerations, and the results of various investigations carried out during the evaluation process. The goal of this section is to assess the effectiveness of the design and evaluate its performance in terms of societal, health, safety, and sustainability impacts.

5.1Novelty

The design of the amplifier leverages traditional Class-A Common-Emitter topology, which is known for its simplicity and stable gain characteristics. The novelty of this project lies in the use of gpdk090 technology, a 90nm process, for the design of a low-power RF power amplifier at 433 MHz. This frequency range is commonly used in short-range communication systems like IoT devices, remote controls, and sensor networks, making the design particularly relevant to modern wireless applications. Additionally, the integration of LC matching networks for impedance matching and the optimization of power-added efficiency (PAE) were essential aspects that helped improve the performance and efficiency of the design. This amplifier not only meets the design goals but also demonstrates a practical approach to optimizing RF power amplification in a low-power and compact form.

5.2 Design Considerations (PO(c))

The design process required careful consideration of several factors to ensure that the final amplifier was both functional and safe for real-world applications. These factors included public health and

safety, environmental considerations, and societal needs.

5.2.1 Considerations to Public Health and Safety

The design of the amplifier took into account the potential risks associated with electromagnetic radiation, particularly since RF amplifiers are typically used in wireless communication systems that emit RF signals. To mitigate any health risks, the amplifier was designed to operate within the legal power output limits and comply with regulations on RF exposure, ensuring that it would be safe for consumers and users.

5.2.2 Considerations to Environment

From an environmental perspective, the design aimed to reduce power consumption while maintaining the required output power. By focusing on achieving a power-added efficiency (PAE) of 7.5%, the amplifier was designed to minimize energy waste, making it more environmentally friendly for applications such as IoT and remote sensors that require energy-efficient solutions. Furthermore, the choice of gpdk090 technology, which is a widely used CMOS process, is known for its relatively lower environmental impact during manufacturing, compared to other technologies.

5.2.3 Considerations to Cultural and Societal Needs

The amplifier design aligns with the growing demand for energy-efficient and cost-effective wireless communication solutions, especially in IoT and remote monitoring systems that are critical in both industrial and consumer applications. The amplifier's design can contribute to the development of smart cities, environmental monitoring, and healthcare systems, all of which are essential to meet societal needs in the modern world.

5.3Investigations (PO(d))

In this section, we describe the investigations carried out to validate the design and ensure that the amplifier met the required specifications

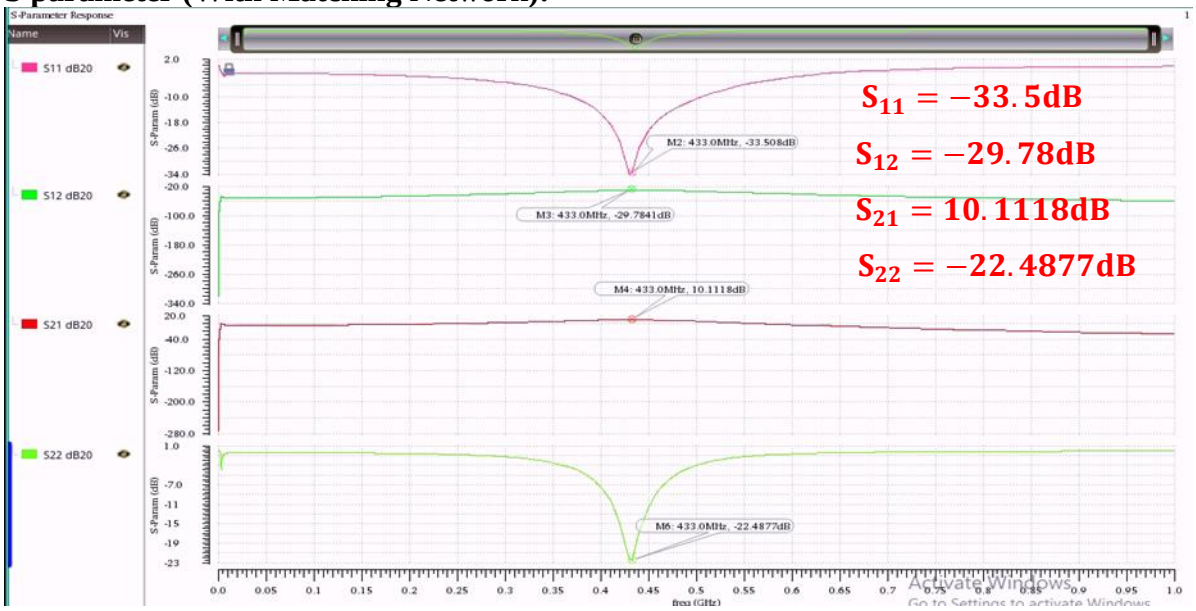
5.3.1 Design of Experiment

To validate the amplifier's performance, a comprehensive experiment was designed involving multiple phases of testing. The experiment included testing the amplifier under various operating conditions, such as varying input signals and supply voltages, to assess its behavior and stability. Performance measurements such as gain, output power, and efficiency were taken to compare against the simulation results.

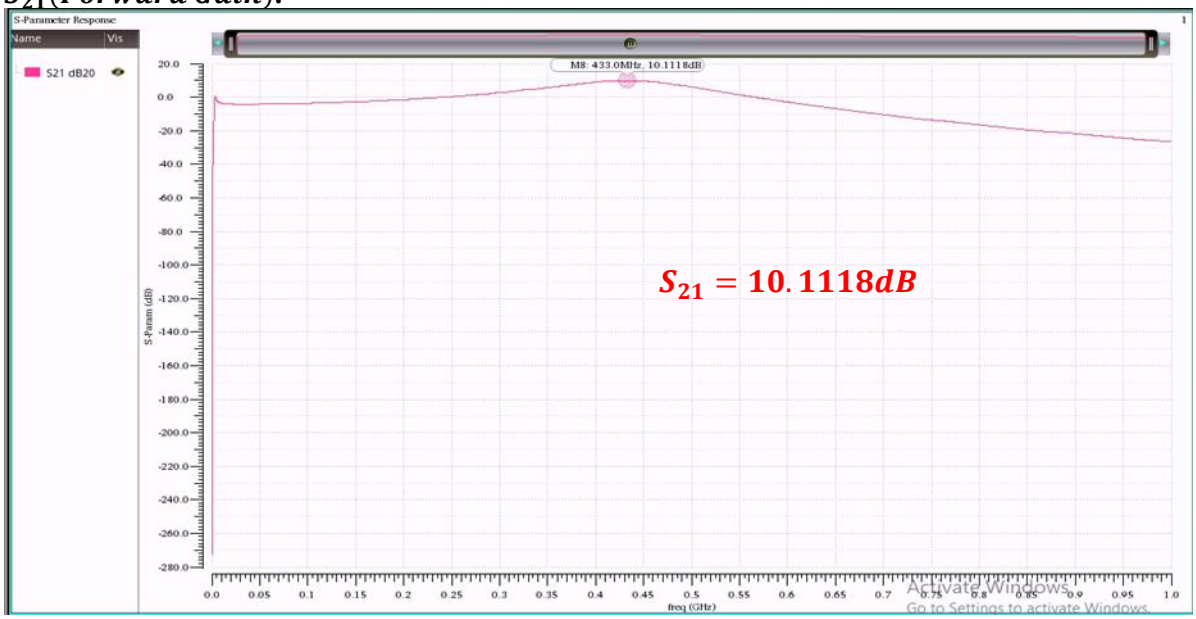
5.3.2 Data Collection

Data was collected through a series of tests using key data points recorded included the amplifier's voltage gain, output power at various frequencies, and S-parameters for impedance matching. These results were used to evaluate the overall performance and to identify any deviations from the expected performance.

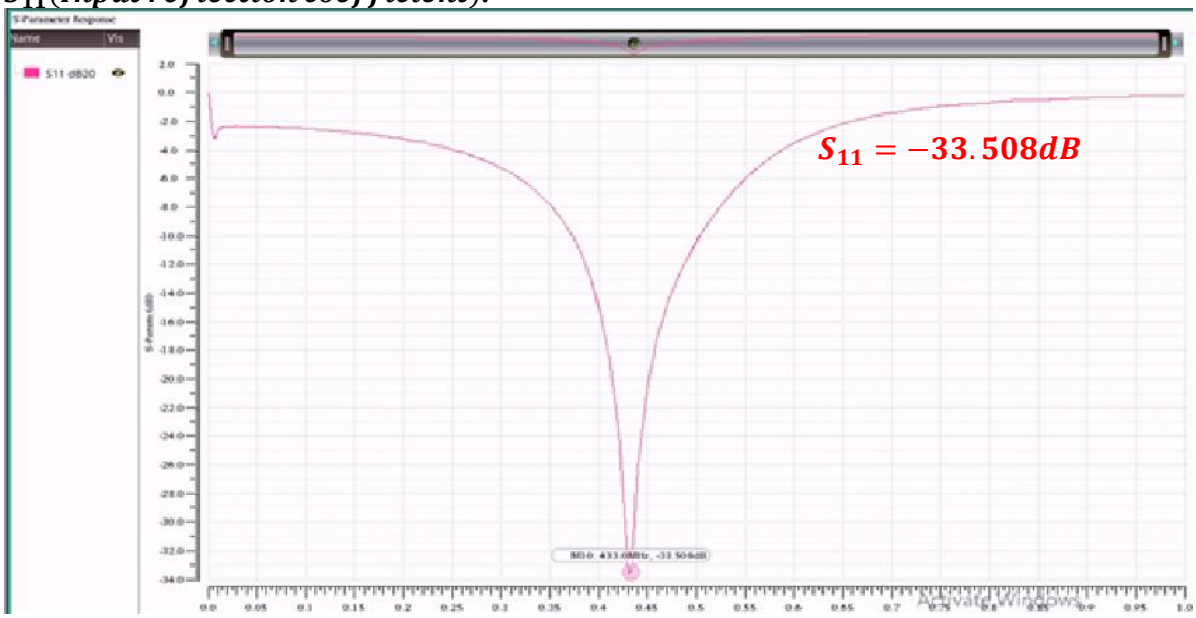
S parameter (With Matching Network):



$S_{21}(Forward\ Gain)$:



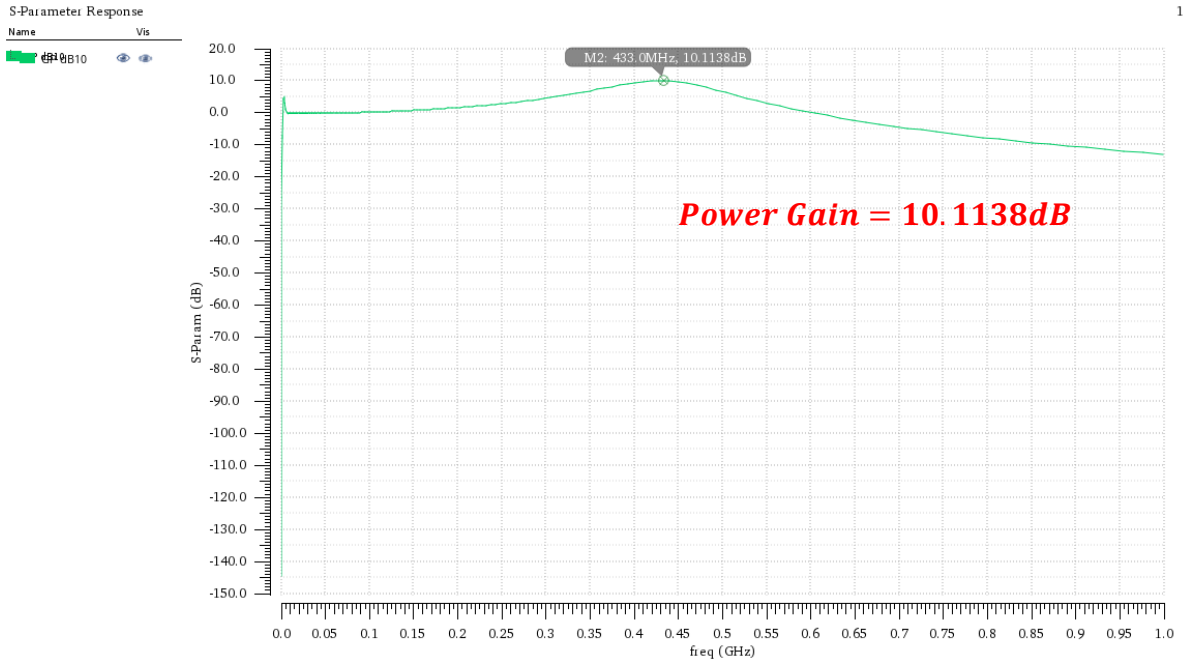
$S_{11}(Input\ reflection\ coefficient)$:



5.3.3 Results and Analysis

The data collected from the experiment confirmed that the design met the key performance specifications. The amplifier achieved 10.118 dB voltage gain, 18.01 dBm saturated output power, and a PAE of 7.5%, which is higher than the required 5%. The impedance matching was also found to be satisfactory, with minimal signal reflection at both the input and output ports, as confirmed by the S-parameter measurements.

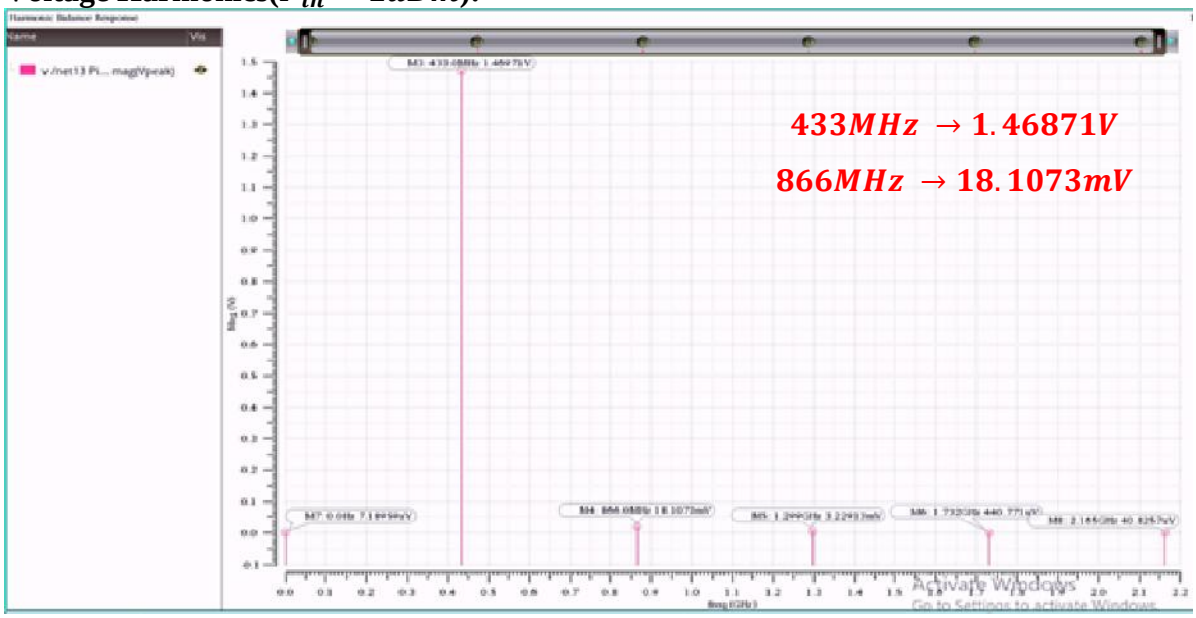
Power Gain:



Power Gain = 10.1138dB

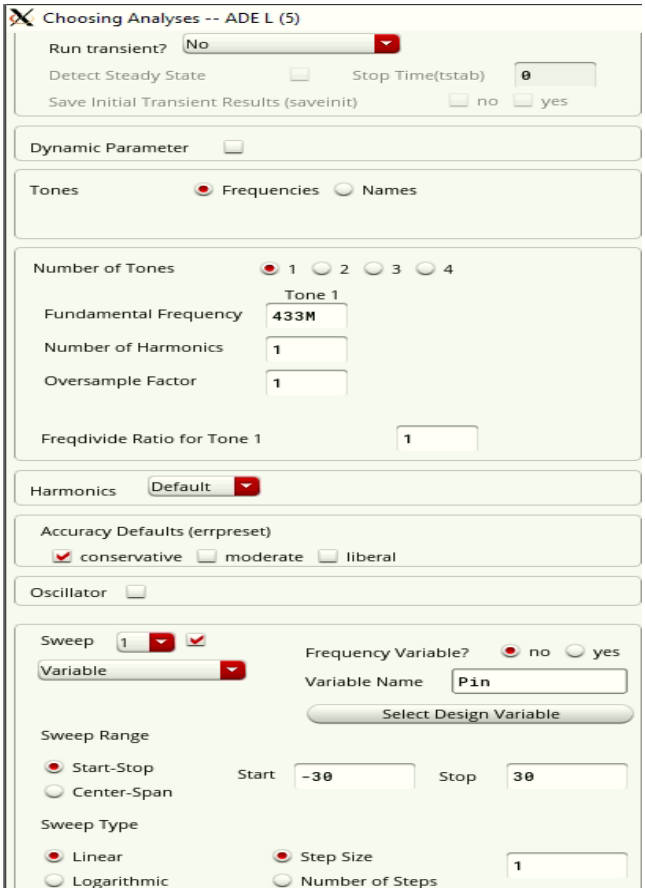
P_{sat} *Analysis*

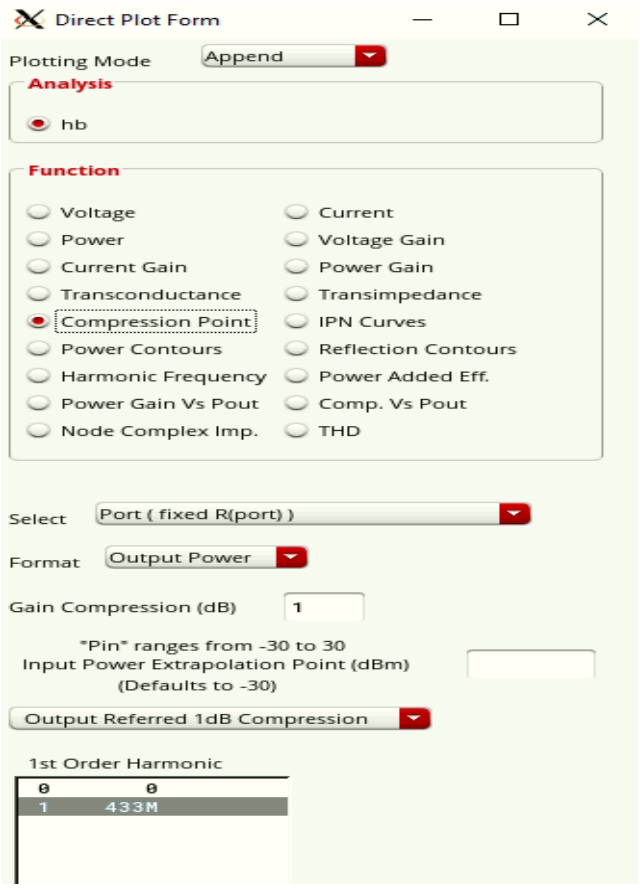
Voltage Harmonics($P_{in} = 1dBm$):



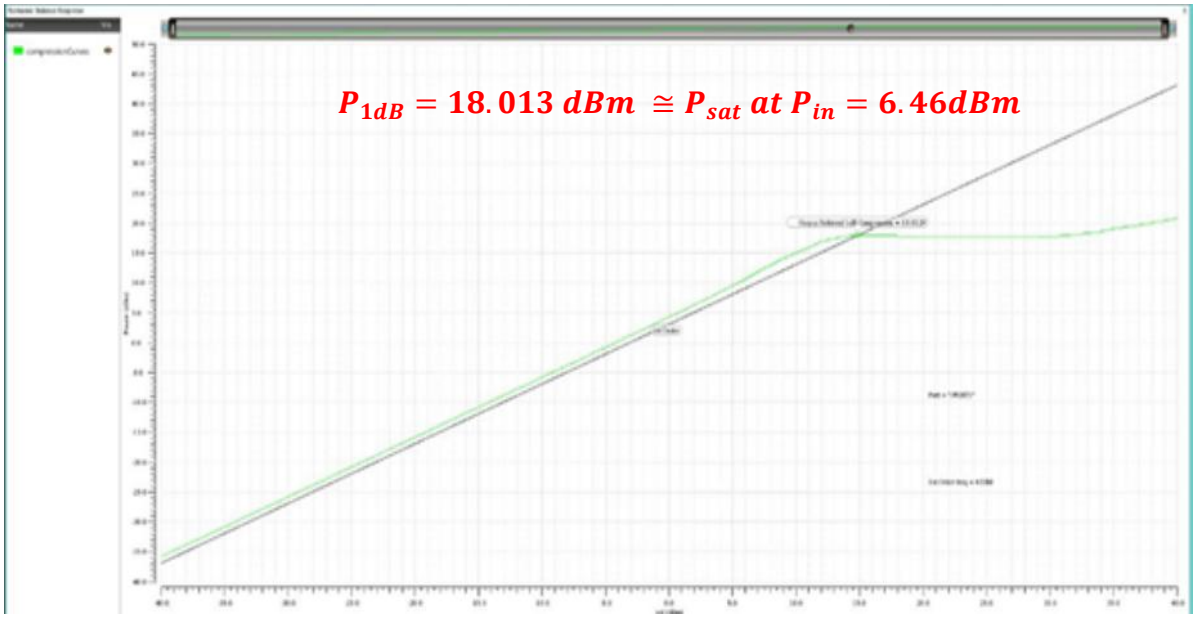
Power Harmonics($P_{in} = 1dBm$):

P_{in} vs P_{out} Simulation:



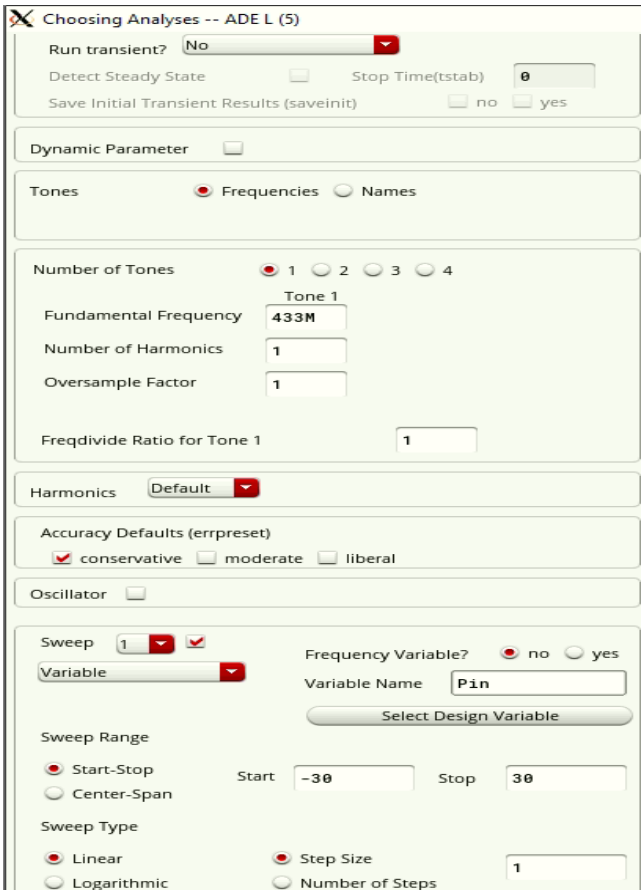


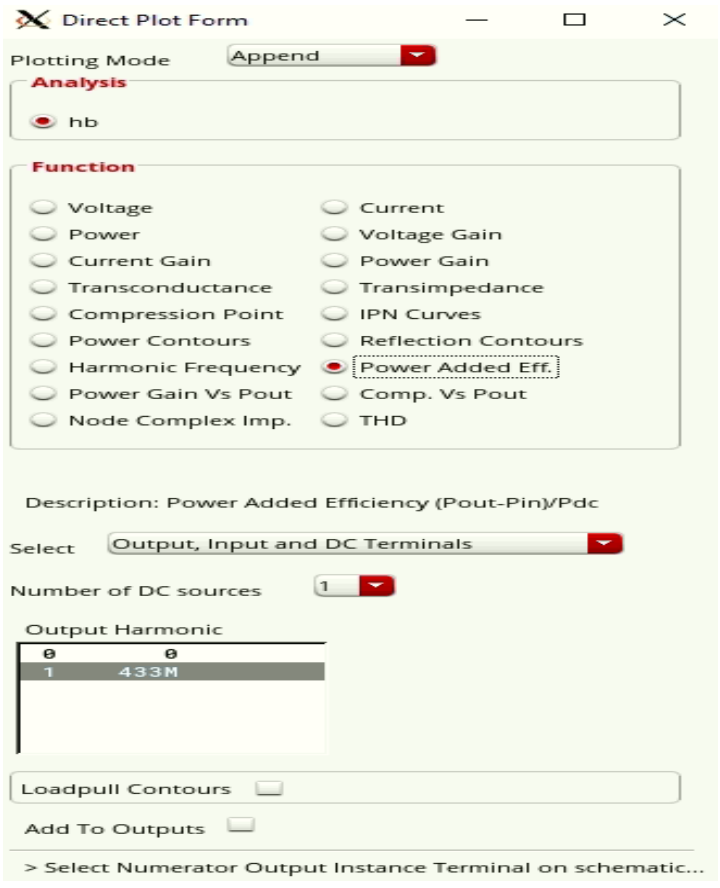
P_{out} *vs* P_{in}:



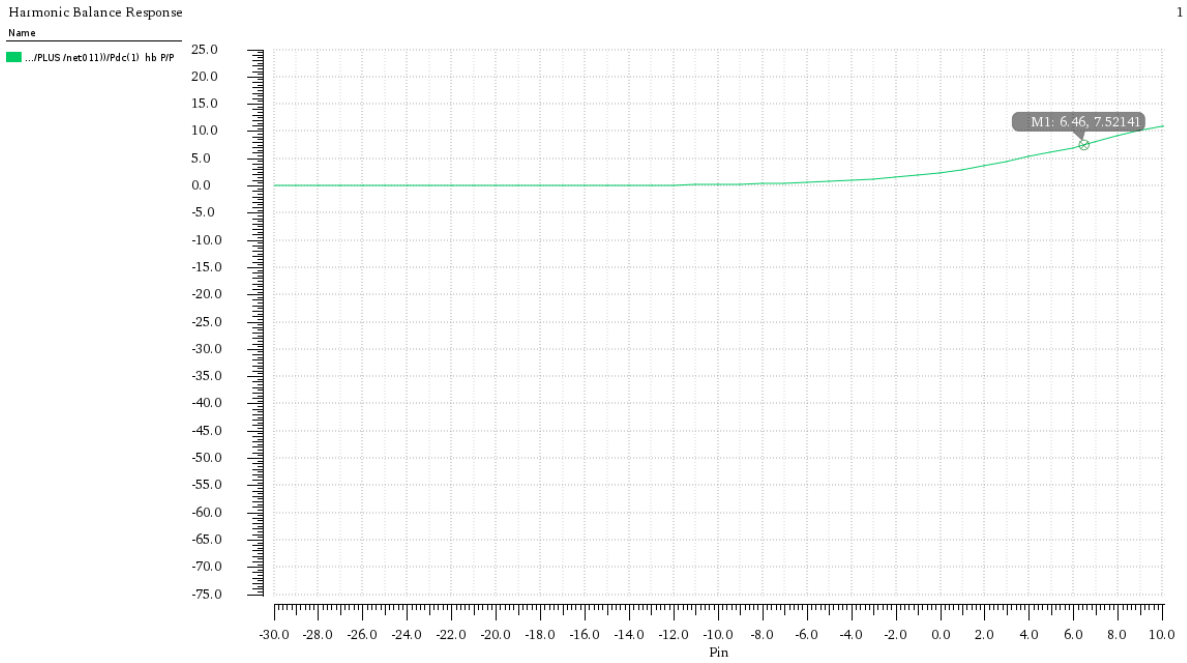
PAE Analysis

PAE Simulation Set up:





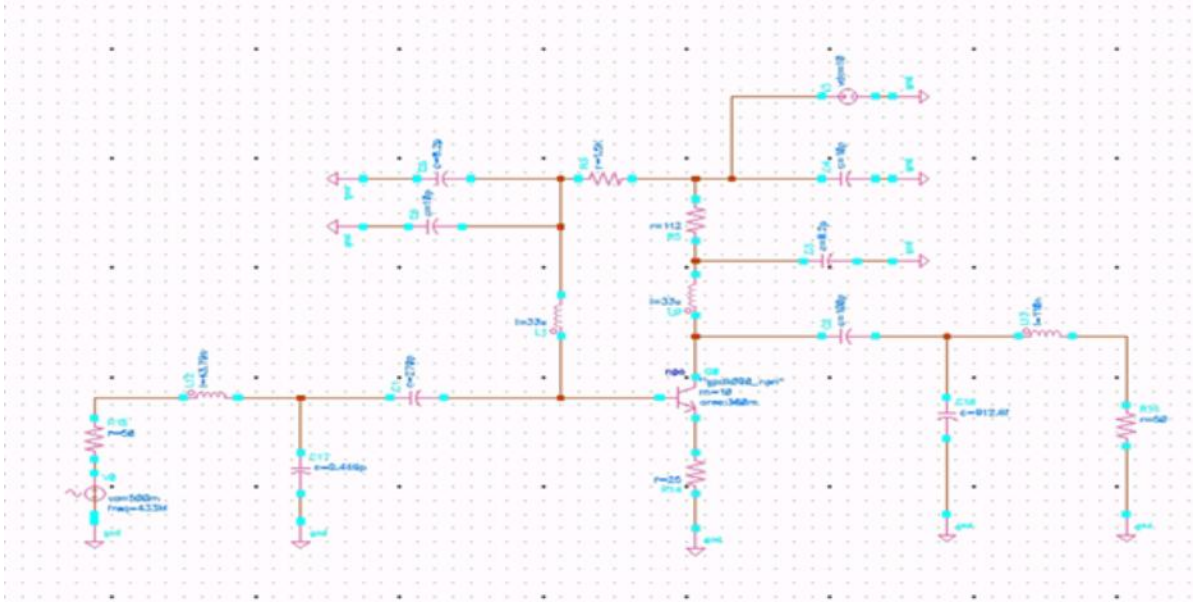
Plot



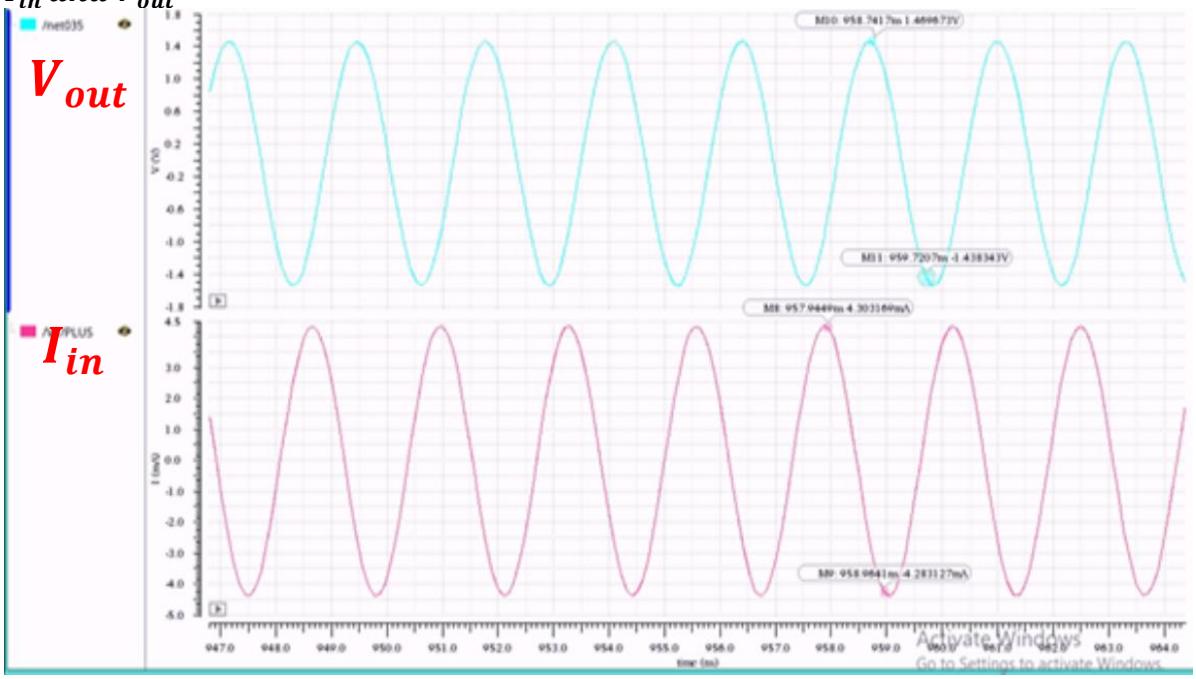
$$\boldsymbol{PAE = 7.52141\%}$$

PAE (Manual Calculation):

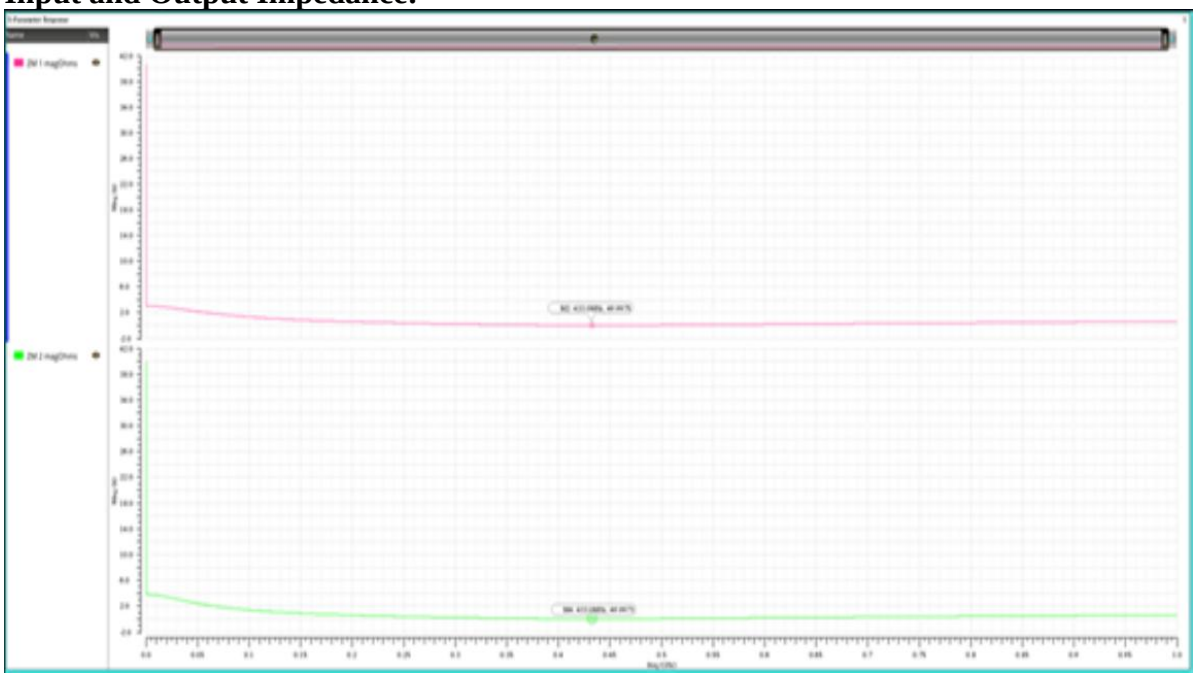
Modified circuit to calculate PAE at Vin = 500mV



I_{in} and V_{out}



Input and Output Impedance:



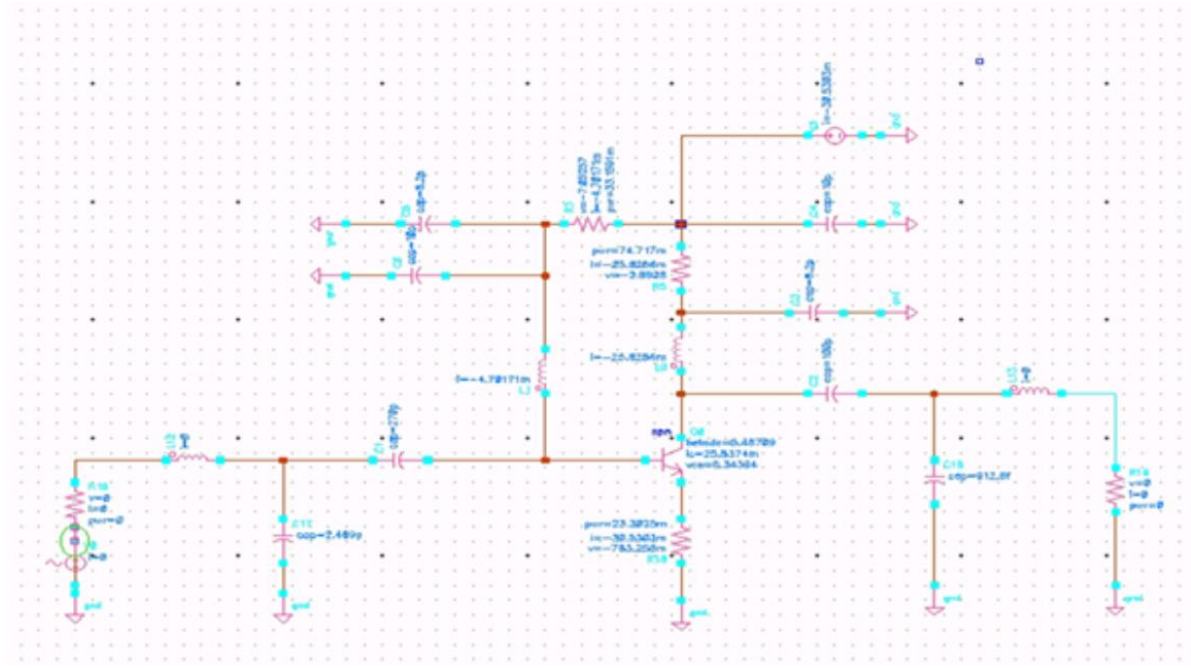
Input and Output Impedance, ZM1 = 49.9975Ω

Now,

$$P_{RF,in} = V_{in}I_{in} = \frac{0.5}{\sqrt{2}} \times \frac{4.29\times10^{-3}}{\sqrt{2}} = 1.0725mW$$

$$P_{RF,out} = \frac{{V_{out}}^2}{R} = \frac{\left(\frac{1.46}{\sqrt{2}}\right)^2}{50} = 21.316mW$$

***DC* Simulation:**



$$P_{DC} = V_{dc}I_{dc} = 10 \times 30.5303 \times 10^{-3} = 305.303mW$$

$$PAE = \frac{P_{RF,out} - P_{RF,in}}{P_{DC}} = \frac{21.316 - 1.0725}{305.303} = 6.63\%$$

Therefore,
PAE falls in the desired range and matches with the simulation result.

5.3.4 Interpretation and Conclusions on Data

The results of the experiment aligned with the simulation outcomes, validating the effectiveness of the design. The amplifier successfully met the performance targets and demonstrated stability during testing. The data also highlighted areas for potential improvement, such as optimizing the thermal management of the design to ensure long-term reliability.

Comparison table of target and achieved specifications

Parameter	Value (Required)	Value (Achived)
Frequency	**433 MHz**	**433MHz**
Gain	**≥ 10 dB**	**10.1138dB**
Power-Added Efficiency (PAE)	**≥ 5%**	**7.5%**
Saturation Power (Psat)	**≥ 17 dBm**	**18.01 dBm**
Technology	**gpdk090 or tsmc18**	**gpdk090**

Table : Comparison table of target and achieved specifications

5.4 Limitations of Tools (PO(e))

While the simulation and implementation processes provided useful insights, there were certain limitations to the tools used. The Cadence Virtuoso environment is powerful but requires significant computational resources for large-scale simulations. Additionally, the gpdk090 technology, while highly effective, has certain limitations in terms of scaling for high-frequency applications beyond the ISM bands. The amplifier design also faces limitations in terms of output power due to the nature of the Class-A topology, which is inherently less efficient compared to other amplifier classes such as Class-B or Class-AB.

5.5Impact Assessment (PO(f)

5.5.1 Assessment of Legal Issues

The amplifier design is expected to have a positive societal impact, especially in areas such as smart city development, healthcare monitoring, and environmental monitoring. By providing a cost-effective and energy-efficient solution for wireless communication, the amplifier supports the advancement of communication technologies that contribute to societal well-being.

5.5.2 Assessment of Health and Safety Issues

As mentioned earlier, the amplifier was designed to operate within safe limits of RF exposure, ensuring compliance with regulations. Furthermore, the potential risks of electromagnetic interference were mitigated through the careful design . Overall, the health and safety risks were minimized through design choices and adherence to regulatory guidelines.

5.5.3 Assessment of Legal Issues

The legal aspects of this design include ensuring that the amplifier meets the legal power output limits set by regulatory bodies, such as the Federal Communications Commission (FCC) and other relevant international standards for RF devices. The design was evaluated against these standards to ensure compliance, making it suitable for commercial and consumer use.

5.6 Sustainability Evaluation (PO(g))

The sustainability of the design was evaluated based on its power efficiency, material usage, and potential for long-term reliability. The choice of CMOS technology and the focus on maximizing power-added efficiency (PAE) contribute to the sustainability of the design, as it reduces energy consumption and minimizes waste heat generation. Additionally, the compact form factor and low power consumption make the amplifier suitable for battery-operated applications, enhancing its sustainability for portable devices.

5.7 Ethical Issues (PO(h))

Ethical considerations in the design process included ensuring that the amplifier operated within legal and safety limits, particularly concerning RF exposure. The design also adhered to the ethical standards related to intellectual property by ensuring that all sources of information, including design techniques and components, were properly cited. No ethical challenges related to environmental impact were encountered, as the design focused on energy efficiency and reducing waste.

6 Reflection on Individual and Team work (PO(i))

In this section, we reflect on the individual contributions of each team member and evaluate the mode of teamwork throughout the project. This section highlights the strengths of the team, how collaboration facilitated the design and implementation processes, and how we managed challenges. Additionally, we include a diversity statement to acknowledge the variety of perspectives and experiences within the team, as well as a logbook documenting key milestones and the role of each member in the project.

6.1 Individual Contribution of Each Member

Each member of the team played a crucial role in the successful completion of the project. Here is a breakdown of the contributions made by each member:

ID NO	Team Member	Contribution
2006068	Ilias Ahmad	Ilias was responsible for overseeing the overall progress of the project, ensuring that all tasks were completed on time, and coordinating team meetings. He focused on the design of the biasing network and input/output matching circuits, as well as leading the simulation and testing phases.
2006090	Mohammad Al Hosan	Hosan worked on the circuit design and simulation testing. He designed the LC-based matching networks in QUCS Studio, performed all simulations in Cadence Virtuoso, and validated key metrics like gain, Psat, and PAE through simulation and manual calculations.
2006116	Shohan Ahmed Rifat	Shohan contributed significantly to the simulation process, where he worked on fine-tuning the amplifier's performance in Cadence Virtuoso. He was also responsible for generating the S-parameter simulations and analyzing the results to ensure that the amplifier met the impedance matching and gain requirements.
2006122	Md. Alamgir Islam	Alamgir focused on the literature review and the theoretical aspects of the amplifier design. He also helped with the design of the biasing network and was involved

		in the data collection during the testing phase. Additionally, he assisted in writing the report and documenting the results.

Table: Individual Contribution of Each Member

Each team member took ownership of specific tasks, contributing to the project's success and ensuring that the design met the specified requirements.

6.2 Mode of Team Work

Our teamwork approach was highly collaborative, with each team member contributing their expertise in different areas of the project. We held regular meetings to discuss progress, resolve challenges, and ensure that everyone was on the same page. Communication was key, especially when troubleshooting issues in the design or when performing simulations and testing. We made use of shared files and project management tools to track milestones and keep all documentation up-to-date.

The mode of teamwork can be described as **distributed** yet **cohesive**, where individual responsibilities were clearly defined but efforts were aligned toward achieving a common goal. Each member's expertise complemented the others, which helped streamline the workflow and allowed us to effectively manage time and resources.

6.3 Diversity Statement of Team

Our team consisted of individuals with diverse academic backgrounds and skill sets, which played a vital role in the success of the project. The diversity in our team enabled us to approach problems from different perspectives, enhancing creativity and problem-solving. The ability to work collaboratively, combining our different strengths in areas like circuit design, simulation and testing, was one of the key factors that contributed to the completion of the project on time.

We value the different perspectives and experiences that each team member brought to the table, which made the team more dynamic and adaptable. This diversity of thought not only strengthened our technical capabilities but also improved our decision-making processes throughout the project.

6.4 Log Book of Project Implementation

The logbook serves as a record of key milestones, individual roles, and contributions made throughout the project. The logbook includes dates, the tasks completed on those dates, and any challenges or milestones reached. Below is a summary of the logbook:

Step	Milestone Achieved	Individual Role	Team Role	Comments
01	Initial design concept finalized	Ilias Ahmad (Concept)	All team members	Discussed amplifier design parameters.
02	Simulation model setup complete	Shohan Ahmed Rifat (Simulation)	All team members	Simulated DC, AC, and S-parameters.
03	Circuit Simulation and tunning	Mohammad Al Hosan (Tuning)	All team members	Completed ckt
04	Assembled amplifier on Virtuoso	Mohammad Al Hosan (Testing)	All team members	Finalize the ckt
05	Final testing and measurements	All team members	All team members	Performed gain, output power, and efficiency tests.

Phase	Date	Duration	Activities	Responsible Members
Phase 1	02 June 2025	Week 8	Literature Review, Background	Ilias(68), Rifat(116), Hosan(90), Alamgir(122)
Phase 2	09 June 2025	Week 9	Circuit Design and Simulation in Cadence Virtuoso	Ilias, Rifat, Hosan
Phase 3	16 June 2025	Week 10	S-parameters Extraction and Analysis, Matching Network Design in QUCS Studio	Hosan, Alamgir, Rifat
Phase 4	23 June 2025	Week 11	Optimization and Tuning of Matching Network	Rifat, Alamgir, Ilias
Phase 5	30 June 2025	Week 12	Testing and Validation of the Amplifier	Ilias, Rifat, Hosan
Phase 6	07 July 2025	Week 13	Final Adjustments, Documentation, Presentation and Final Report Writing	Ilias, Rifat, Hosan, Alamgir

The logbook ensured that we tracked each stage of the project, allowing us to maintain clear documentation of what was done and when. This helped identify areas of improvement and ensured transparency throughout the project.

7 Communication to External Stakeholders (PO(j))

In this section, we focus on how we communicated our project to external stakeholders, such as potential users and other interested parties. Effective communication ensures that the project's outcomes are shared, understood, and accessible to individuals or organizations who could benefit from the work. This section outlines the executive summary, user manual, and other communication tools used to engage with external stakeholders.

7.1Executive Summary

The Class-A Common-Emitter RF Power Amplifier designed for the 433 MHz ISM band is a crucial component for wireless communication systems, particularly in the Internet of Things (IoT) and short-range communication applications. This amplifier has been designed to achieve key performance specifications such as a voltage gain of at least 10 dB, a saturated output power of 17 dBm, and a power-added efficiency (PAE) greater than 5%. The design, developed using the **gpdk090** 90nm CMOS process, was tested and validated through simulations and real-world testing to ensure its efficiency and stability.

This amplifier meets the needs of low-power wireless systems by offering a compact, cost-effective solution for RF power amplification. Its efficiency and stable gain make it ideal for integration into various communication devices like sensor nodes, remote controls, and other wireless systems. Through detailed simulations and testing, we confirmed that the amplifier provides optimal performance in the 433 MHz frequency band, with minimal signal reflection and high power transfer efficiency. The design process, simulations, and results can help inform future designs for similar applications in low-power wireless communication.

7.2 User Manual

The User Manual serves as a comprehensive guide for stakeholders, including engineers and system integrators, who may want to use or integrate the amplifier into their systems. The manual includes the following sections:

Overview: A brief introduction to the amplifier and its intended applications.

Installation Instructions: Guidelines on how to install the amplifier into a communication system, including wiring and power connections.

Operation Instructions: A step-by-step guide on how to operate the amplifier, including input/output connections, power requirements, and gain adjustment.

Maintenance and Troubleshooting: Information on how to maintain the amplifier for optimal performance and how to troubleshoot common issues such as low output power or impedance mismatching.

7.2 Github Link

https://github.com/mohammad-al-hosan/Class_A_RF_Power_Amplifier_433MHz.git

7.3 YouTube Link

https://youtube.com/playlist?list=PLzSfhCfNVVm-tkZL3ung2yJLJry7UKSiI&si=5trGUQU66sjjjxlz

https://drive.google.com/drive/folders/1c4CzqFKPvqEVDD8nWDSwRVUpA5qGY1GG

8 Future Work (PO(l))

The project successfully demonstrated the design and simulation of the Class-A Common-Emitter RF Power Amplifier for the 433 MHz ISM band. However, there are several areas where future work can further enhance the design and improve performance. One area of future improvement could be optimizing the amplifier's efficiency to meet modern standards, especially for low-power applications. Additionally, experimenting with different transistor models or technologies, such as GaN (Gallium Nitride), may increase the power output and reduce the device size. Furthermore, incorporating a thermal management system to deal with heat dissipation issues would make the amplifier more robust and suitable for commercial use. Lastly, practical implementation and testing of the amplifier in real-world communication systems should be considered to validate the theoretical results.

9 References

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