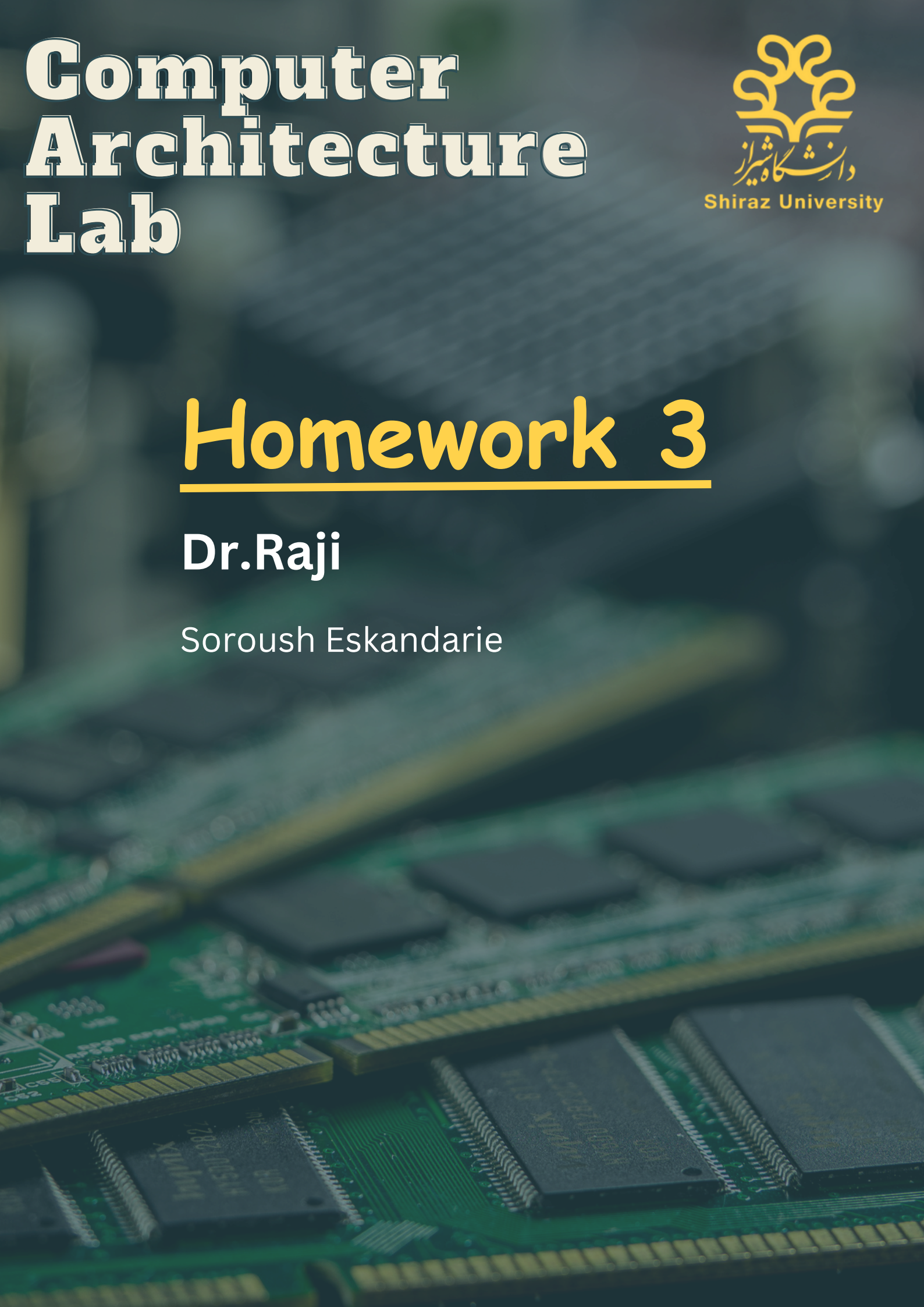
# Computer Architecture Lab

دانشگاه شیراز
Shiraz University

# Homework 3

## Dr.Raji

Soroush Eskandarie



# Modules:

```
module Memory(
    input [7:0] data,
    input clk,
    input [9:0] address,
    input writeSignal,
  , output[7:0] out_data
)
```

all of modules above with their test bench.v

## Memory:

You should Implement a memory module that contains 1024 , 8bit cells that saves data for us.

- you should initiate it with 0 value
- if writesignal == 1 we save the data into the addressed cell other wise we change the value of out_data to addressed cell
- all of these operations above take place by posedge of our clock