بنام خدا

طراحی سیستم های دیجیتال

نیم سال دوم 1403-1402

تمرین اول

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- جواب سوالات را در قالب فایل PDF، به آدرس "khu.dsd98@gmail.com" با عنوان "A_U_1: stdName 1, stdName 2"ارسال کنید.
- تمرین ها را می توانید در گروه های دو نفره ارسال کنید که stdName 1 , stdName 2 نام اعضای گروه است.
- فایل PDF باید شامل کدهای VHDL قابل سنتز و اسکرین شات‌های RTL، post-mapping و compilation report باشد.
- هر روز تاخیر در ارسال تکلیف شامل ۲۰ درصد جریمه خواهد شد.

- **IMPORTANT Note:** Synthesis your designs in Quartus Software as described in the tutorial video and extract the RTL form of your design. Take a screen shot of the RTLs. You can use the following link to get the tutorial video: https://drive.google.com/file/d/1J41ptyTsOxudNs4T1qDWQywa3E2Z7yIH/view?usp=sharing

1. Explain the basic blocks and interconnections of FPGA, CPLD, and PAL. Then, compare these chips in terms of area, performance, power, applications, and security.

2. In digital systems it is often necessary to have circuits that can shift the bits of a vector by one or more bit positions to the left or right. One kind of shifter circuit shifts more bit positions at a time. If the bits that are shifted out are placed into the vacated positions on the left, then the circuit effectively rotates the bits of the input vector by a specified number of bit positions. Such a circuit is often called a barrel shifter. Write a VHDL code to implement a four-bit barrel shifter that rotates the bits by 0, 1, 2, or 3 bit positions as determined by the valuation of two control signals s1 and s0.

s_1	s_0	y_3	y_2	y_1	y_0
0	0	w_3	w_2	w_1	w_0
0	1	w_0	w_3	w_2	w_1
1	0	w_1	w_0	w_3	w_2
1	1	w_2	w_1	w_0	w_3

Figure 1 Operation of Barrel Shifter

3. The purpose of the decoder and encoder circuits is to convert from one type of input encoding to a different output encoding. There are many possible types of code converters. One common example is a BCD-to-7-segment decoder, which converts one binary-coded decimal (BCD) digit into information suitable for driving a digit oriented display. As illustrated in Figure 2, the circuit converts the BCD digit into seven signals that are used to drive the segments in the display. Each segment is a small light-emitting diode (LED), which glows when driven by an electrical signal. The segments are labeled

from a tog in Figure 2. Write a VHDL code that implements this code converter using case statement.

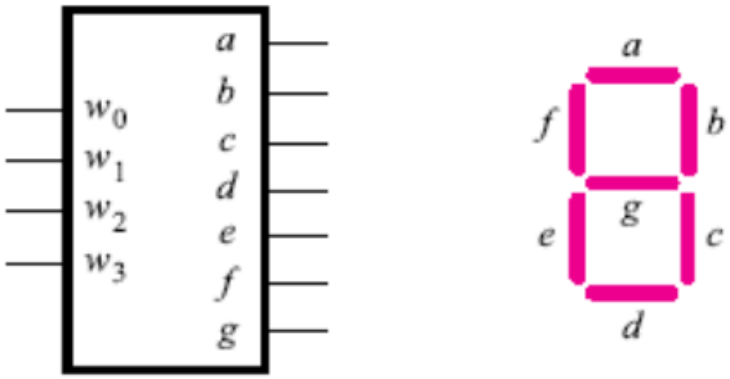
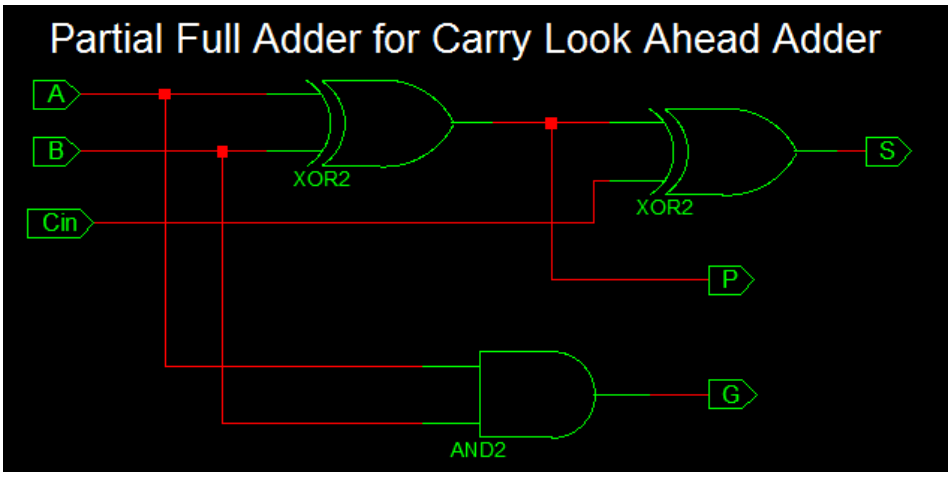


Figure 2 BCD to 7 segment

4. Have you ever heard anything about the Carry Look-ahead adder? These kinds of adders improve the speed of Ripple-Carry adders by reducing the waiting time for calculation of carry bits. For the purpose of carry propagation, carry look-ahead adder constructs partial full adder, propagation, and generation Carry block. Write a VHDL code to implement a partial full adder as follows:



5. In this question, we are going to learn about the implementation of a full adder, using a 3:8 decoder and OR gates. *X*, *Y*, and *C-in* are the input of the full adder. *Sum* and *C-out* outputs of a full adder have the following truth tables:

X	*Y*	*C-in*	*Sum*	*C-out*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Therefore, we have,

Sum = ∑(1, 2, 4, 7)
C-out = ∑(3, 5, 6, 7)

a) Draw architecture (model) of the full adder using a 3:8 decoder and OR gates

b) Write a VHDL code to implement the full adder.

6. Write a synthesizable VHDL description of the following combinational circuit using concurrent statements.