DPTF-PSPVTC-2239

**Feature:** Verify DGFC participant can have its power control capabilities changed in the UI

As a Validation Engineer

I want to assure that the power controls can be changed for DGFC in the UI

**Background:**

**Given** I have enabled the Power Share Policy

**Given** I have enabled all applicable Participants in BIOS

**And** I have launched the UI in Designer view

**Scenario:**  Verify that DGFC power controls can be found in the UI

**When** I open the UI and click on participants

**And** I click on the DGFC participant

**Then** I will see the power controls for DGFC

**Scenario:**  Verify that DGFC participant power controls can be changed in the UI

**When** I have the power levels for DGFC open

**And** I change PL1 min and max values and save

**Then** I should see a notification that table was saved.

**When** I open the DGFC participant in the UI in Monitor view

**Then** I will see the PL1 Min and Max value that I set in Designer view

[DPTF-PSPVTC-2245](https://jama4.intel.com/perspective.req?docId=16410121&projectId=104)

**Feature:** Verify that the GET\_PARTIPANT\_RESIDENCY\_UTILIZATION primitives are functional

As a Validation Engineer

I want to assure that the GET\_PARTIPANT\_RESIDENCY\_UTILIZATION primitives can perform a getp/setp operation without issue

**Background:**

**Given** I have enabled the Power Share Policy

**Given** I have enabled all applicable Participants in BIOS

**And** I have launched the UI in Designer view

**Scenario:**  Verify that TCPU participant can perform a getp operation without issue

**Given** That I have ESIF Shell open and the TCPU participant selected

**When** I type infofpc skl\_proc

**Then** I will see the primitive 443.D0.255 in the list under domain D0

**When** I type getp 443 D0 255

**Then** ESIF Shell will report the current residency utilization percentage for the TCPU participant

**Scenario:**  Verify that TCPU participant can perform a setp operation without issue

**Given** That I have ESIF Shell open and the TCPU participant selected

**When** I type infofpc skl\_proc

**Then** I will see the primitive 474.D0.255 in the list under domain D0

**When** I type setp 474 D0 255

**Then** ESIF Shell will report successful setting of the participant residency utilization primitive

**When** I type getp 443 D0 255

**Then** ESIF Shell will report the current residency utilization percentage and should match what I set previously

**Scenario:**  Verify that TCPU participant can perform a rstp operation without issue

**Given** That I have ESIF Shell open and the TCPU participant selected

**When** I type infofpc skl\_proc

**Then** I will see the primitive 474.D0.255 in the list under domain D0

**When** I type setp 474 D0 255

**Then** ESIF Shell will report successful setting of the participant residency utilization primitive

**When** I type getp 443 D0 255

**Then** ESIF Shell will report the current residency utilization percentage and should match what I set previously

**When** I type rstp 474 D0 255

**And** I perform a getp 443 D0 255

**Then** ESIF Shell should report the original value prior to performing the setp operation

[DPTF-PSPVTC-2256](https://jama4.intel.com/perspective.req?docId=16531858&projectId=104)

**Feature:** Verify that various PSHA primitives can be set via ESIF Shell

As a Validation Engineer

I want to assure that the PSHA table can be edited without issue in the ESIF Shell (rstp does not work so see table below for default values)

**Background:**

**Given** I have enabled the Power Share Policy

**Given** I enabled MCP, and DGFC in BIOS

**And** Once in the OS, I have launched the ESIF Shell

**Scenario:**  Verify that **PID Target** can be set in the ESIF Shell

**When** I open the ESIF Shell and type parts

**And** I select MCPP from the parts list

**And** I type getp 038 D0 000 (GET\_RAPL\_POWER\_LIMIT)

**Then** a value will be displayed in mW

**When** I type setp 130 D0 000 <A value 10% less than default> (SET\_RAPL\_POWER\_LIMIT)

**Then** ESIF shell will report value changed to new value

When I perform an appstop/appstart DPTF

Then DPTF will stop and then start again

**When** I type getp 038.D0.000 (GET\_RAPL\_POWER\_LIMIT)

**Then** the value reported will be the value I set with Primitive 130.D0.00

**Repeat for the following:**

**Kp**                  getp 456 D0 255 (GET\_PID\_KP\_TERM)  
                       setp 457 D0 255 (SET\_PID\_KP\_TERM)

**Ki**                   getp 458 D0 255 (GET\_PID\_KI\_TERM)  
                       setp 459 D0 255 (SET\_PID\_KI\_TERM)

**Tau**getp 460 D0 255 (GET\_PID\_TIME\_AVERAGE\_CONSTANT)  
                       setp 461 D0 255 (SET\_PID\_TIME\_AVERAGE\_CONSTANT)

**Scenario:**  Verify that **DGFx energy/power threshold** can be set in the ESIF Shell

**When** I open the ESIF Shell and type parts

**And** I select DGFC from the parts list

**And** I type getp 472 D0 255 (GET\_PARTICIPANT\_ENERGY\_THRESHOLD)

**Then** a value will be displayed in Joules

**When** I type setp 473 D0 255 <A value 10% less than default> (SET\_PARTICIPANT\_ENERGY\_THRESHOLD)

**Then** ESIF shell will report value changed to new value

When I perform an appstop/appstart DPTF

Then DPTF will stop and then start again

**When** I type getp 472 D0 000 (GET\_ PARTICIPANT\_ENERGY\_THRESHOLD)

**Then** the value reported will be the value I set with Primitive 473 D0 255

**Repeat for the following:**

**DGfx utilization threshold**getp 470 D0 255 (GET\_PARTICIPANT\_UTILIZATION\_THRESHOLD)  
                                               setp 471 D0 255 (SET\_PARTICIPANT\_UTILIZATION\_THRESHOLD)

**Scenario:**  Verify that **IA temp threshold** can be set in the ESIF Shell

**When** I open the ESIF Shell and type parts

**And** I select TCPU from the parts list

**And** I type getp 468 D0 255 (SET\_ GET\_POWER\_SHARE\_TEMPERATURE\_THRESHOLD)

**Then** a value will be displayed in temp C

**When** I type setp 469 D0 255 <A value 10% less than default> (SET\_ GET\_POWER\_SHARE\_TEMPERATURE\_THRESHOLD)

**Then** ESIF shell will report value changed to new value

When I perform an appstop/appstart DPTF

Then DPTF will stop and then start again

**When** I type getp 468 D0 000 (GET\_ GET\_POWER\_SHARE\_TEMPERATURE\_THRESHOLD)

**Then** the value reported will be the value I set with Primitive 469 D0 255

**Repeat for the following:**

**IA utilization threshold**getp 470 D0 255(GET\_PARTICIPANT\_UTILIZATION\_THRESHOLD)  
                                          setp 471 D0 255(SET\_PARTICIPANT\_UTILIZATION\_THRESHOLD)

[DPTF-PSPVTC-2256](https://jama4.intel.com/perspective.req?docId=16531858&projectId=104)

**Feature:** Verify that various PSHA primitives can be set via ESIF Shell

As a Validation Engineer

I want to assure that the PSHA table can be edited without issue in the ESIF Shell (rstp does not work so see table below for default values)

**Background:**

**Given** I have enabled the Power Share Policy

**Given** I enabled MCP, and DGFC in BIOS

**And** Once in the OS, I have launched the ESIF Shell

**Scenario:**  Verify that **PID Target** can be set in the ESIF Shell

**When** I open the ESIF Shell and type parts

**And** I select MCPP from the parts list

**And** I type getp 038 D0 000 (GET\_RAPL\_POWER\_LIMIT)

**Then** a value will be displayed in mW

**When** I type setp 130 D0 000 <A value 10% less than default> (SET\_RAPL\_POWER\_LIMIT)

**Then** ESIF shell will report value changed to new value

When I perform an appstop/appstart DPTF

Then DPTF will stop and then start again

**When** I type getp 038.D0.000 (GET\_RAPL\_POWER\_LIMIT)

**Then** the value reported will be the value I set with Primitive 130.D0.00

**Repeat for the following:**

**Kp**                  getp 456 D0 255 (GET\_PID\_KP\_TERM)  
                       setp 457 D0 255 (SET\_PID\_KP\_TERM)

**Ki**                   getp 458 D0 255 (GET\_PID\_KI\_TERM)  
                       setp 459 D0 255 (SET\_PID\_KI\_TERM)

**Tau**getp 460 D0 255 (GET\_PID\_TIME\_AVERAGE\_CONSTANT)  
                       setp 461 D0 255 (SET\_PID\_TIME\_AVERAGE\_CONSTANT)

**Scenario:**  Verify that **DGFx energy/power threshold** can be set in the ESIF Shell

**When** I open the ESIF Shell and type parts

**And** I select DGFC from the parts list

**And** I type getp 472 D0 255 (GET\_PARTICIPANT\_ENERGY\_THRESHOLD)

**Then** a value will be displayed in Joules

**When** I type setp 473 D0 255 <A value 10% less than default> (SET\_PARTICIPANT\_ENERGY\_THRESHOLD)

**Then** ESIF shell will report value changed to new value

When I perform an appstop/appstart DPTF

Then DPTF will stop and then start again

**When** I type getp 472 D0 000 (GET\_ PARTICIPANT\_ENERGY\_THRESHOLD)

**Then** the value reported will be the value I set with Primitive 473 D0 255

**Repeat for the following:**

**DGfx utilization threshold**getp 470 D0 255 (GET\_PARTICIPANT\_UTILIZATION\_THRESHOLD)  
                                               setp 471 D0 255 (SET\_PARTICIPANT\_UTILIZATION\_THRESHOLD)

**Scenario:**  Verify that **IA temp threshold** can be set in the ESIF Shell

**When** I open the ESIF Shell and type parts

**And** I select TCPU from the parts list

**And** I type getp 468 D0 255 (SET\_ GET\_POWER\_SHARE\_TEMPERATURE\_THRESHOLD)

**Then** a value will be displayed in temp C

**When** I type setp 469 D0 255 <A value 10% less than default> (SET\_ GET\_POWER\_SHARE\_TEMPERATURE\_THRESHOLD)

**Then** ESIF shell will report value changed to new value

When I perform an appstop/appstart DPTF

Then DPTF will stop and then start again

**When** I type getp 468 D0 000 (GET\_ GET\_POWER\_SHARE\_TEMPERATURE\_THRESHOLD)

**Then** the value reported will be the value I set with Primitive 469 D0 255

**Repeat for the following:**

**IA utilization threshold**getp 470 D0 255(GET\_PARTICIPANT\_UTILIZATION\_THRESHOLD)  
                                          setp 471 D0 255(SET\_PARTICIPANT\_UTILIZATION\_THRESHOLD)

[DPTF-PSPVTC-2265](https://jama4.intel.com/perspective.req?docId=16561995&projectId=104)

Description:

**Feature:** Verify PSHA actions are taken in the Adaptive Performance policy

As a user I want to be able to see PSHA Table actions taken in the Adaptive Performance Policy

**Background:**

**Given** I have enabled the Power Share Policy

And I have enabled MCP and DGFC in BIOS

And I have launched the UI in Monitor Mode on the Power Share Policy page

**And** I have saved as the following PSHA table as psha1

| *Participant Scope* | *Domain* | *Default Bias* |

| TCPU | Multifunction | 0.5 |

| DGFC | Dgfc Core | 0.5 |

And I have saved as the following PSHA table as psha2

| Participant Scope | Domain | *Default Bias* |

| MCPP | Multichip Package | |

| TCPU | Multifunction | 0.9 |

| DGFC | Dgfc Core | 0.1 |

And I have saved as the following PSHA table as psha3

| *Participant Scope* | *Domain* | *Default Bias* |

| TCPU | Multifunction | 0.7 |

           | DGFC                           |  Dgfc Core                    |  0.3                      |

**And** I have added an action set to APAT called psha\_one with actions

| *Participant Scope* | *Domain* | *Code* | *Arguments* |

| IETM | Other | PSHA | psha1 |

**And** I have added an action set to APAT called psha\_two with actions

| *Participant Scope* | *Domain* | *Code* | *Arguments* |

| IETM | Other | PSHA | psha2 |

And  I have added an action set to APAT called psha\_three with actions

| *Participant Scope* | *Domain* | *Code* | *Arguments* |

| IETM | Other | PSHA | psha3 |

**And** I have added an APCT condition using action psha\_one

​ | *Condition* | *Comparator* | *Argument* |

| OEM Variable 0 | == | 100 |

**And** I have added an APCT condition using action psha\_three

​ | *Condition* | *Comparator* | *Argument* |

| OEM Variable 0 | == | 101 |

**And** I have added an APCT condition using action psha\_two

​ | *Condition* | *Comparator* | *Argument* |

| OEM Variable 0 | == | 102 |

**Scenario:** Verify BIAS Changes when APCT conditions are met

**And** I have the UI Monitor running on the Power Share Policy page

**When** I set OEM Variable 0 to 100

**Then** the Power Share policy is shown using table with TCPU bias of 0.5

And the Power Share policy is shown using table with DGFC bias of 0.5

**And** the Power Share loop is not running

When I set OEM Variable 0 to 101

Then the Power Share policy is shown using table with TCPU bias of 0.9

And the Power Share policy is shown using table with DGFC bias of 0.1

**And** the Power Share loop is running

When I set OEM Variable 0 to 102

Then the Power Share policy is shown using table with TCPU bias of 0.7

And the Power Share policy is shown using table with DGFC bias of 0.3

**And** the Power Share loop is not running

Verify that the power share loop is active only under specific conditions

Global ID:

[4-8098308](https://jama4.intel.com/perspective.req?docId=16647947&projectId=104)

ID:

[DPTF-PSPVTC-2266](https://jama4.intel.com/perspective.req?docId=16647947&projectId=104)

Description:

**Feature**: Verify that the power share loop is active only under specific conditions

**Background**:

**Given** Power Share policy is enabled

**Scenario**: Power share loop is active when at least two Activity status participants and MCP are bound

**When** I start with a known PSHA table

 | Participant Scope                                       | Domain            | BIAS |  
 | MCPP: Intel DPTF Multi Chip Participant   | DGFXMCP    | N/A   |  
 | DGFC: Intel DPTF DGFX Core Participant | DGFXCORE | .6      |  
 | TCPU: DPTF CPU Device                          | Multifunction    | .4     |

**And** I start tracing with DEBUG level

**Then** the "Power Share Participant Status" table is updated at regular intervals

And the CPU utilization information is logged with tag PSP\_UTILIZATION to the trace log file at default 100ms intervals

And the DGFX utilization information is logged with tag PSP\_UTILIZATION to the trace log file at default 100ms intervals

Scenario: Power share loop is not active when no participants are bound

**When** I start with an empty PSHA table

And I start tracing with DEBUG level

Then the "Power Share Participant Status" table is not updated

And the Utilization information is not logged to the trace log file

**Scenario Outline**: Power share loop is not active when only two participants are bound

When I start with a known PSHA table with <two participants>

And I start tracing with DEBUG level

Then the "Power Share Participant Status" table is not updated

And the Utilization information is not logged to the trace log file

**Examples**:

| two participants    |

| MCPP and DGFC |

| TCPU and DGFC  |

| MCPP and TCPU  |

Scenario Outline: Power share loop is not active when only one participant is bound

**When** I start with a known PSHA table with <participant>

And I start tracing with DEBUG level

Then the "Power Share Participant Status" table is not updated

And the Utilization information is not logged to the trace log file

Examples:

| participant |

| MCPP      |

| DGFC       |

| TCPU       |

Verify power split with only one Activity status participant and MCP bound

Global ID:

[4-8098517](https://jama4.intel.com/perspective.req?docId=16648476&projectId=104)

ID:

[DPTF-PSPVTC-2267](https://jama4.intel.com/perspective.req?docId=16648476&projectId=104)

Description:

**Feature**: Verify power split with only one Activity status participant and MCP are bound

Note: Run this only on old build [8.3 /8.4]

Latest builds doesnt have option to create a table for

HSD: <https://hsdes.intel.com/appstore/article/#/2208072644>

**Scenario**: Power split set to 100% to CPU when only TCPU and MCPP are bound

**Given** Power Share policy is enabled

**And** the PSHA table consists of entries of only TCPU and MCPP

**And** the PSH PID Target is less than TCPU PL1 max

**When**I run a 3D workload

**Then** 100% share of power is set to the TCPU

**And** the power share control loop is not active

Scenario: Power split set to 100% to DGFC when only DGFC and MCPP are bound

**Given** Power Share policy is enabled

**And** the PSHA table consists of entries of only DGFC and MCPP

**And** the PSH PID Target is less than DGFC PL1 max

**When**I run a 3D workload

**Then** 100% share of power is set to the DGFC

**And** the power share control loop is not active

Scenario: No action taken if MCPP is not bound

**Given** Power Share policy is enabled

**And** the PSHA table consists of entries of only DGFC and TCPU

**And** the PSH PID Target is less than DGFC PL1 max

**And** the PSH PID Target is less than TCPU PL1 max

**When**I run a 3D workload

**Then** no power share power split action is taken

**And** the power share control loop is not active

Verify Power Share Participant Status values output to trace file log.docx

Global ID:

[4-8115504](https://jama4.intel.com/perspective.req?docId=16671696&projectId=104)

ID:

[DPTF-PSPVTC-2268](https://jama4.intel.com/perspective.req?docId=16671696&projectId=104)

Description:

**Feature:** Verify Power Share Participant Status outputs to trace file

As a user I want to be able to start/stop a trace and see the Power Share Participant Status output to a log file.

**Background:**

**Given** I have enabled the Power Share Policy

**Given** I enabled MCP and DGFC in BIOS

**Given** I have created a PSHA Tables (MCP, DGFC, TCPU) and assigned BIAS values

**And** once in the OS, I have launched the UI in Monitor Mode on the Power Share Policy page

**Scenario:** Verify Power Share Participant Status values appear in the policy monitor page.

**Given** I have the UI Monitor running and I’m on the Power Share Policy page

**Then** I should see activity in the PSP Status table for CPU Utilization, Graphics Utilization, CPU Utilization Threshold, Graphics Utilization Threshold, CPU Energy, Graphics Energy, Total MCP Power, Time Delta, and PID Budget information.

And all Utilization and Threshold Utilization values are shown in units of percent

And all Energy values are shown in units of joule

And all Power values are shown in units of milliwatts

And all Time and Delta values are shown in units of milliseconds

**Scenario:** Verify Power Share Participant Status values appear in a trace file log under PSP\_ENERGY, PSP\_TDP\_HR, PSP\_BIAS tags

**Given** that I start a trace and end the trace after 2 minutes

**And** I open the trace file

**Then** in the trace log file under PSP\_ENERGY tag, I will see PSP Status energy/power values that were captured

And under PSP\_TDP\_HR tab I will see the TDP headroom values

And under the PSP\_BIAS tag I will see the CPU/Graphics Effective BIAS values

**Story**[**DPTF-2057**](https://jira01.devtools.intel.com/browse/DPTF-2057)**Power Sharing Algorithm [Part 2] - Energy**

**Story**[**DPTF-205**](https://jira01.devtools.intel.com/browse/DPTF-2057)[**8**](https://jira01.devtools.intel.com/browse/DPTF-2058)**Power Sharing Algorithm [Part 2] - Energy**

**Story**[**DPTF-2059**](https://jira01.devtools.intel.com/browse/DPTF-2059)**Power Sharing Algorithm [Part 2] - Energy**

Verify that If GFX exists in PSHA and primitive fails, want to set Total MCP Power from just CPU participant

Global ID:

[4-8115606](https://jama4.intel.com/perspective.req?docId=16671939&projectId=104)

ID:

[DPTF-PSPVTC-2269](https://jama4.intel.com/perspective.req?docId=16671939&projectId=104)

Description:

**Feature:** Verify that If GFX exists in PSHA and primitive fails, want to set Total MCP Power from just CPU participant

As a user I want total MCP Power to be calculated from TCPU if GFx exists but the primitive fails.

**Background:**

**Given** I have enabled the Power Share Policy

**Given** I enabled MCP and DGFC in BIOS

**Given** I have created a PSHA Tables (MCP, DGFC, TCPU) and assigned BIAS values

**And** once in the OS, I have launched the UI in Monitor Mode on the Power Share Policy page

**Scenario:** Verify that Total MCP Power is calculated from CPU Energy

**Given** I have the UI Monitor running and I’m on the Power Share Policy page

**When** I perform a setp 476 D0 255 for SET\_RAPL\_ENERGY to zero

**Then** I should see Total MCP Power values still being calculated

Verify MCP assigns the same PL1 Limit to a participant if there is only one participant in the PSHA table

Global ID:

[4-8143503](https://jama4.intel.com/perspective.req?docId=16742233&projectId=104)

ID:

[DPTF-PSPVTC-2278](https://jama4.intel.com/perspective.req?docId=16742233&projectId=104)

Description:

**Feature:** Verify MCP assigns the same PL1 Limit to a participant if there is only one participant in the PSHA table

As a Validation engineer I want to ensure that if there is only 1 participant besides the MCPP that the MCPP’s PL1 limit is applied to the participant’s (such as TCPU) PL1 Limit

**Background:**

**Given** I have enabled the Power Share Policy

**Given** I enabled MCP and DGFC in BIOS

**Given** I have created a PSHA Table (MCPP, DGFC, and TCP as Participants) and assigned BIAS values

**And** once in the OS, I have launched the UI in Monitor Mode on the Power Share Policy page

**Scenario:** Verify when there is only 1 participant besides the MCPP in the PSHA table that MCPP assigns its PL1 Limit to the TCPU participants PL1 Limit

**Given** I have a PSHA table with three participant (MCPP, DGFC, and TCPU)

**When** I open the UI in Designer Mode and explore the TCPU Participant

**And** I set the PL1 Max to max settings and save

**Then** on the TCPU participant tab I will see that PL1 is at the max value I just saved earlier

**When**I remove the DGFC participant from the PSHA table and then save the changes

**Then** in the UI monitor I should see only the MCPP and TCPU in the PSHA table

**When** I click on the MCPP Participant tab

**Then** I will see the PL1 Limit for the MCPP

**When** I click on the TCPU Participant Tab

**And** I ensure that the TCPU is NOT being limited by any policy

**Then** the PL1 Limit for TCPU should match the MCPP PL1 limit

**REPEAT FOR MCP/DGFC, MCP/DGHM combinations**

Verify able to uninstall/re-install Power Share related participants

Global ID:

[4-8210614](https://jama4.intel.com/perspective.req?docId=16856505&projectId=104)

ID:

[DPTF-PSPVTC-2294](https://jama4.intel.com/perspective.req?docId=16856505&projectId=104)

Description:

**Feature**: Verify able to uninstall/re-install Power Share related participants

**Background:**

**Given** Power Share policy is enabled on the system

**And**MCPP, DGFC, and TCPU participants are enabled

**Scenario**: Verify no crash is observed when uninstalling multi-chip package participant driver

**When** I uninstall MCP device driver

**And** I uninstall the manager device driver

**Then** there are no application or system event log messages indicating that the user-mode driver crashed

<https://hsdes.intel.com/resource/1209994847>

**Scenario:** Verify graphics energy interrupt continues to work after uninstalling/re-installing manager driver

**Given**a valid PSHA table is active

**And**start a workload (ex: 3D Paint) such that PSH loop remains in slow poll mode but dGfx is active

**And**the graphics energy threshold is set low enough such that an interrupt consistently happens in less time that the slow poll interval

**When** I uninstall DPTF manager driver from the device manager

**And**I re-install DPTF manager driver in the device manager

**Then** I can see graphics energy interrupt is still consistently causing a PSH loop iteration at approximately same interval as before

<https://hsdes.intel.com/resource/220399940>

[DGFC Participant] [PSHA] Verify DGFC participant can have AC & DC PeakPower manipulated by the Power Boss Policy

Global ID:

[4-8221050](https://jama4.intel.com/perspective.req?docId=16880315&projectId=104)

ID:

[DPTF-PSPVTC-2300](https://jama4.intel.com/perspective.req?docId=16880315&projectId=104)

Description:

**Feature:** Verify DGFC participant can have AC & DC PeakPower manipulated by the Power Boss Policy

As a Validation Engineer

I want the Power Boss policy to have control over participants to allow my system to be more flexible in changing thermal conditions.

**Background:**

**Given** I have enabled the Power Share Policy

**And** I have the drivers for the graphics card installed to enable the “PowerShare Participant Status” table

**And** I have Power Boss enabled in BIOS

**Scenario:**  Verify that AC Peak Power can be changed in Power Boss

**When** I add “AC Peak Power” and a value from 0-35000 to the PBAT for the DGFC participant

**And** I add a condition to the PBCT

**And** I set the condition to “true” to activate the PBAT

**And**I start a 3D workload.

**And** I navigate to the DGFC participant and look for the “Peak Power Control” table

**Then** I will see a value NEAR\* the value I set for “AC Peak Power” in the PBAT

**Scenario:**  Verify that DC Peak Power can be changed in Power Boss

**When** I add “DC Peak Power” and a value from 0-35000 to the PBAT for the DGFC participant

**And** I add a condition to the PBCT

**And** I set the condition to “true” to activate the PBAT

**And**I start a 3D workload.

**And** I navigate to the DGFC participant and look for the “Peak Power Control” table

**Then** I will see a value NEAR\* the value I set for “DC Peak Power” in the PBAT

\*At the time this test was written, DPTF sets a value for peak power, reads the value back and updates the requested value back to the UI. This is due to the fact that what we request is not guaranteed by the driver.  The table under the hood for Peak Power is unknown at this time.  Story has note to update this test when more information is available.

Verify that PSHA table can be exported to BIOS

Global ID:

[4-7999535](https://jama4.intel.com/perspective.req?docId=16406973&projectId=104)

ID:

[DPTF-PSPVTC-2243](https://jama4.intel.com/perspective.req?docId=16406973&projectId=104)

Description:

**Feature:** Verify that PSHA table can be exported to BIOS

As a Validation Engineer:

I want to assure that the PSHA table can be exported without issue

**Scenario:**  Verify that PSHA table can be edited

**Given** I have enabled the Power Share Policy

**And** I have enabled all applicable Participants in BIOS

**And** that I have an existing PSHA Table

**When** I click on the Export icon

**And** I select yes, include override from Generate Data Vault (GDDV) option

**And** I click on Next

**And** I click on Export

**Then** DPTF will give the number of keys exported and the file location for the files

**And** I click on Finish

Verify Power Share logging entries

Global ID:

[4-8304008](https://jama4.intel.com/perspective.req?docId=17077340&projectId=104)

ID:

[DPTF-PSPVTC-2313](https://jama4.intel.com/perspective.req?docId=17077340&projectId=104)

Description:

**Feature:** Verify Power Share logging entries

**Background:**

**Given** I have enabled the Power Share Policy

**Given** I have enabled all applicable Participants in BIOS

**And** I have loaded a valid PSHA table

**Scenario:**  Verify Power Share logging entries

**When** I open the ESIF shell and enter "*trace module 4 dptf && trace route 4 log && trace level 4*"

And I open a command prompt in the C drive

**And** I enter the following commands

*logman trace create session1 -p EsifUmdf2EtwProvider 0x2 5 -o session1.etl*

*logman start session1*

*logman stop session1*

*tracerpt session1\_000001.etl -o session1\_000001.csv -of CSV*

**And** I will see session1\_000001.csv in the C drive

**Then** I run the powershell script pshEtwScrape.ps1\* against the session1\_000001.csv file

**When** I open the created session1\_000001.csv

**Then** there will be entries containing the following power share variables:

*PID Target (mW), Kp, Ki, Tau (ms), Fast Polling Interval (ms), Slow Polling Interval (ms), Graphics Energy Threshold (J), Processor Temperature Threshold (C), Graphics Utilization Threshold (%), Processor Utilization Threshold (%), Weighted Slow Poll Averaging Constant, Slow Poll Power Threshold (mW), Processor Default BIAS, Graphics Default BIAS, MCP PL1 Min (mW), MCP PL1 Max (mW), Processor PL1 Min (mW), Processor PL1 Max (mW), Graphics PL1 Min (mW), Graphics PL1 Max (mW), Processor Utilization (%), Graphics Utilization (%), Processor Energy (J), Graphics Energy (J), Total MCP Power (mW), Time Delta (ms), PID Budget (mW), Available Headroom (mW), iterm, Effective Processor BIAS, Effective Graphics BIAS, Processor TDP Budget (mW), Graphics TDP Budget (mW), Graphics Instantaneous Power (mW)*

\*Script located at \\chakotay\SoftVal\DPTF\_tools\pshEtwScrape.ps1. OR Use \\chakotay\Temp\osidletX\\_scripts and reg files\psh-log-to-csv.ps1 to convert the trace taken via UI instead of the commands listed above.

Note: Automatable when automation can deal with PowerShell script files.

Verify default values for PSH algorithm variables

Global ID:

[4-8304106](https://jama4.intel.com/perspective.req?docId=17077530&projectId=104)

ID:

[DPTF-PSPVTC-2314](https://jama4.intel.com/perspective.req?docId=17077530&projectId=104)

Description:

**Feature:** Verify default values for PSH algorithm variables

**Scenario Outline:** Verify default values for PSH algorithm variables

**Given** Power Share policy is enabled

**And** the MCPP participant is available

And the DGFC participant is available

And the TCPU participant is available

**When** I reset any potentially set value for <**variable name**> using esif command "<**reset command**>"

And I appstop dptf

And I appstart dptf

And I open Power Share monitor tab

**Then** the <variable name> value is <**default value**>

When I appstop dptf

And I appstart dptf

Then the <variable name> value is still <**default value**>

**​Examples:**

| **variable name**  | **reset command**  | **default value** |

| PID Target                 | dstn MCPP && rstp 130 D0 0 | 65000**\*** mW     |

| Kp                      | dstn MCPP && rstp 457 D0 255 | 0.8          |

| Ki             | dstn MCPP && rstp 459 D0 255 | 0.5       |

| Alpha               | dstn MCPP && rstp 461 D0 255 | 0.9 sec    |

| Graphics Energy Threshold | dstn DGFC && rstp 473 D0 255 | 25 J         |

| Processor Temperature Threshold  | dstn TCPU && rstp 469 D0 255 | 50.0C        |

| Graphics Utilization Threshold | dstn DGFC && rstp 471 D0 255 | 50.00%        |

| Processor Utilization Threshold | dstn TCPU && rstp 471 D0 255 | 70.00%        |

| Weighted SlowPoll Averaging Constant | dstn MCPP && rstp 467 D0 255 | 0.9 sec       |

| SlowPoll Power Threshold | dstn MCPP && rstp 480 D0 255 | 20000 mW      |

**\***default value on XL part: XT part should be 100W

Verify that Temp Control and Threshold knobs appear under DGFC Participant

Global ID:

[4-8386703](https://jama4.intel.com/perspective.req?docId=17223099&projectId=104)

ID:

[DPTF-PSPVTC-2328](https://jama4.intel.com/perspective.req?docId=17223099&projectId=104)

Description:

**Feature:** Verify that Temp Control and Threshold knobs appear under DGFC Participant

As a Validation Engineer, I want to ensure that when a GFX Workload is applied, that the correct temp statistics appear under the DGFC Participant

**Background:**

**Given** DPTF is enabled in BIOS

**And** that the UIv2 is open and that the DGFC participant is open

**And** that the latest Alto driver (graphics) is installed

**And** I have TAT installed

**Scenario:** Verify that temp control/threshold appear under DGFC participant

**When** I monitor the DGFC Participant

**And** I generate a GFX workload in TAT

**Then** I will see a temperature value under the “Temperature Control” table.

HSD:  https://hsdes.intel.com/resource/220138915

Verify policy still calculates power when DGFX energy is 0

Global ID:

[4-8447639](https://jama4.intel.com/perspective.req?docId=17335685&projectId=104)

ID:

[DPTF-PSPVTC-2333](https://jama4.intel.com/perspective.req?docId=17335685&projectId=104)

Description:

**Feature:**Verify policy still calculates power when participant energy is 0

HSD: [220178164](https://hsdes.intel.com/resource/220178164)

**Background:**

**Given** that I am using a platform that supports MCPP

**And** I have DPTF installed

**And** I have the Power Share Policy enabled

**And**I have a valid PSHA table is loaded

**And**I have a valid 3D workload

**Scenario:** Verify policy still calculates power when participant energy is 0

**When** I open the UI

**And** I select the "Power Share Policy" tab

**And** I open the ESIF shell

**And** I select the DGFC participant in the shell

And I get the current RAPL energy with "getp 128 D0 255"

And I set the same value with "setp 476 D0 255 <value>"

**Then** I see in the UI that the Graphics Energy is 0

And I see in the UI that the Graphics Power is 0

And I see all other power values continue to calculate and do not display "X"

Verify that Graphics Instantaneous Power field updates when running a workload

Global ID:

[4-8458712](https://jama4.intel.com/perspective.req?docId=17366939&projectId=104)

ID:

[DPTF-PSPVTC-2334](https://jama4.intel.com/perspective.req?docId=17366939&projectId=104)

Description:

**Feature:** Verify that Graphics Instantaneous Power field updates when running a workload

**Background:**

**Given** I have enabled Power Share Policy in BIOS

**And** I have launched UI in Monitor side with the Power Share Policy tab selected.

**Scenario:**  Verify that Graphics Instantaneous Power updates when running a workload

**When** I have no graphics workload running

**Then** there will be an X  in the Graphics Instantaneous Power field

**When** I start a graphics workload

**Then** Graphics Instantaneous Power will field will update per the polling period

Verify that CPU/Graphics power values are in line with other values when Time Deltas are greater than 200ms

Global ID:

[4-8458912](https://jama4.intel.com/perspective.req?docId=17367478&projectId=104)

ID:

[DPTF-PSPVTC-2335](https://jama4.intel.com/perspective.req?docId=17367478&projectId=104)

Description:

**Feature:** Verify that CPU/Graphics power values are in line with other values when Time Deltas are greater than 200ms

**Background:**

**Given** I have enabled Power Share Policy in BIOS

**And** I have launched the UI in Monitor side with the Power Share Policy tab selected.

**Scenario:**  Verify that cpu/graphics power and time delta values are saved to a log

**When** I create an ETW trace for the following:

|           logman create trace sess1 -p EsifUmdf2EtwProvider 0x2 5 -o output.etl          | \*\*\*

**And**I run a cpu workload on all cores

**And**I run a graphics workload

**And**I run a trace for 60 seconds while the SUT is under a cpu/graphics workload \*

**And**I convert the ETW output .etl to a .csv file

**And** I make that log readable\*\*

**And** I look for Processor Power Calculation Time Deltas and Graphics Power Calculation Time Deltas that are intermittently greater than 200ms

**Then** I should see that the Processor and Graphics Power values are not significantly larger when the Time Delta interval is larger when compared to Power values that have a Time Delta interval of approximately 100ms.

\* Suggested workloads TAT Tool with a 50% CPU-All workload and a 100% Graphics workload running simultaneously.

\*\* See: <https://wiki.ith.intel.com/display/DPTF/How+to+get+Power+Share+Participant+Status+Parameters>

\*\*\* You need to start the trace with the command: **logman start <sessionName>**and once it is done, stop it using **logman stop <sessionName>**

HSD-ES: [220147090](https://hsdes.intel.com/appstore/article/#/220147090)  
Test Case Review by Neil Davidson

Verify Power Share policy does not set a participant TDP Budget to less than PL1 min

Global ID:

[4-8508964](https://jama4.intel.com/perspective.req?docId=17461092&projectId=104)

ID:

[DPTF-PSPVTC-2341](https://jama4.intel.com/perspective.req?docId=17461092&projectId=104)

Description:

Feature: Verify Power Share policy does not set a participant TDP Budget to less than PL1 min

As a Validation Engineer

I want to assure that a participant will not be given a TDP budget less than PL1 min

(tests are automation only)

Background:

Given I have enabled the Power Share Policy​

Given I have enabled all applicable Participants in BIOS

And I have launched the UI in Designer view

And I have a PSHA with an evenly split bias between CPU and DGFX

Scenario:  Verify that DGFX TDP Budget is is not set to less than PL1 min

When I open the DGFC tab in the UI

And I set PL1 limits very high (min 60000, max 65000)

And I save my changes

And I open the Power Share Policy tab

And I confirm that the DGFX utilization is low

Then the DGFX TDP Budget will be equal to 60000

Scenario:  Verify that CPU TDP Budget is is not set to less than PL1 min

When I open the TCPU(0) tab in the UI

And I set PL1 limits very high (min 60000, max 65000)

And I save my changes

And I open the Power Share Policy tab

And I confirm that the CPU utilization is low

Then the CPU TDP Budget will be equal to 60000

Verify Power Share policy does not set a participant TDP Budget to more than PL1 max

Global ID:

[4-8509012](https://jama4.intel.com/perspective.req?docId=17461161&projectId=104)

ID:

[DPTF-PSPVTC-2342](https://jama4.intel.com/perspective.req?docId=17461161&projectId=104)

Description:

Feature: Verify Power Share policy does not set a participant TDP Budget to less than PL1 min

As a Validation Engineer

I want to assure that a participant will not be given a TDP budget more than PL1 max

(tests are automation only)

Background:

Given I have enabled the Power Share Policy​

Given I have enabled all applicable Participants in BIOS

And I have launched the UI in Designer view

And I have a PSHA with an evenly split bias between CPU and DGFX

Scenario:  Verify that DGFX TDP Budget is is not set to more than PL1 max

When I open the DGFC tab in the UI

And I set PL1 limits very low (min 125, max 4000)

And I save my changes

And I open the Power Share Policy tab

And I apply a DGFX load

Then the DGFX TDP Budget will be equal to 4000

Scenario:  Verify that CPU TDP Budget is is not set to more than PL1 max

When I open the TCPU(0) tab in the UI

And I set PL1 limits very low (min 125, man 4000)

And I save my changes

And I open the Power Share Policy tab

And I apply a CPU load

Then the CPU TDP Budget will be equal to 4000

Verify that the policy does not continue calculating CPU/Graphics TDP if Graphics energy is X

Global ID:

[4-8515708](https://jama4.intel.com/perspective.req?docId=17475715&projectId=104)

ID:

[DPTF-PSPVTC-2346](https://jama4.intel.com/perspective.req?docId=17475715&projectId=104)

Description:

**Feature:** Verify that the policy does not continue calculating CPU/Graphics TDP if Graphics energy is X

**Scenario:** Verify that the policy does not continue calculating CPU/Graphics TDP if Graphics energy is X

**Given** the SUT supports switchable graphics

And a valid PSHA table that causes the Power Share loop to run is active

And the system does not have a 3D workload running

**Then** the Graphics Energy shows X J

And CPU TDP Budget shows X mW

And Graphics TDP Budget shows X mW

**When** I start a 3D workload

**Then** the Graphics Energy shows a numeric value

And CPU TDP Budget shows a numeric value

And Graphics TDP Budget shows  a numeric value

**When** I stop the 3D workload

**Then** the Graphics Energy shows X J

And CPU TDP Budget shows X mW

**And** Graphics TDP Budget shows X mW

Verify able to load saved PSHA table

Global ID:

[4-8554502](https://jama4.intel.com/perspective.req?docId=17540937&projectId=104)

ID:

[DPTF-PSPVTC-2350](https://jama4.intel.com/perspective.req?docId=17540937&projectId=104)

Description:

**Feature:**Verify able to load saved PSHA table

**Scenario:**Verify able to load saved PSHA table

**Given** "Power Share Policy" is enabled  
**And**the MCPP participant exists on the system  
**And**the DGFC participant exists on the system

**When** I start with a known PSHA

| participant scope | domain | default bias |

| CPU ^name with description^ | Multifunction | 0.2 |

| DGFC ^name with description^ | DGfx Core | 0.8 |

| MCPP ^name with description^ | Multichip Package | |

**And** I save the table as "psha"

**And** I reset PSHA table to system defaults

**And**I load the saved table "psha"

**Then** the changes are seen on the Power Share Policy page

| participant scope | domain | default bias |

| CPU ^scope with index^ | MultiFunction (0) | 0.2 |

| DGFC ^scope with index^ | DgfxCore (0) | 0.8 |

| MCPP ^scope with index^ | DgfxMcp (0) | N/A |

[HSD 220232739](https://hsdes.intel.com/appstore/article/#/220232739)

Verify input validation for BIAS field

Global ID:

[4-8576521](https://jama4.intel.com/perspective.req?docId=17574074&projectId=104)

ID:

[DPTF-PSPVTC-2356](https://jama4.intel.com/perspective.req?docId=17574074&projectId=104)

Description:

**Feature:** Verify input validation for BIAS field

**Scenario Outline:**Verify input validation for BIAS field

**Given** Power Share policy is enabled

**And** the DGFC participant is available

**When** I start with an empty PSHA table

**And** I add row with Participant Scope set to DGFC

**And** I set Default BIAS to <**bad bias value**>

**Then** an error is displayed to the user

| message |

| Must be tenths decimal within this range: [0.1, 0.9] |

**And**the table Save button is disabled

**When**I update Default BIAS to <**good bias value**>

**Then**the error message is no longer visible

**Examples:**

**| bad bias value | good bias value |**

| 0.01 | 0.1 |

| -0.1 | 0.2 |

| 0 | 0.5 |

| 1.0 | 0.9 |

| 0.55 | 0.7 |

[HSD 220237429](https://hsdes.intel.com/appstore/article/#/220237429)

Verify PL1 limits are reset when PSHA table is unloaded

Global ID:

[4-8576604](https://jama4.intel.com/perspective.req?docId=17574169&projectId=104)

ID:

[DPTF-PSPVTC-2357](https://jama4.intel.com/perspective.req?docId=17574169&projectId=104)

Description:

**Feature:** Verify PL1 limits are reset when PSHA table is unloaded

**Scenario:** Verify PL1 limits are reset when PSHA table is unloaded

**Given** "Power Share Policy" is enabled  
**And**the MCPP participant exists on the system

And the TCPU participant exists on the system  
**And**the DGFC participant exists on the system

And no other policy is actively controlling TCPU or DGFC PL1 limit

**When** I start with a known PSHA

| participant scope | domain | default bias |

| CPU ^name with description^ | Multifunction | 0.2 |

| DGFC ^name with description^ | DGfx Core | 0.8 |

| MCPP ^name with description^ | Multichip Package | |

And I add either CPU or Graphics workload such that either TCPU/DGFC is throttled by Power Share below its PL1 max

And I clear and save the PSHA table\*

**Then** the TCPU PL1 limit is restored to its PL1 Max

**And**the DGFC PL1  limit is restored to its PL1 Max

**\***stops the Power Share loop from running: Power Share policy is no longer actively adjusting TCPU/DGFC budgets

Short Name:

Verify ability to disable re-balancing of unused PID Budget using config option

Global ID:

[4-8609803](https://jama4.intel.com/perspective.req?docId=17625935&projectId=104)

ID:

[DPTF-PSPVTC-2360](https://jama4.intel.com/perspective.req?docId=17625935&projectId=104)

Description:

Feature: Verify ability to disable re-balancing of unused PID Budget using config option

Background:

Given a known PSHA is loaded

| participant scope            | domain            | default bias |

| CPU ^name with description^  | Multifunction     | 0.1          |

| DGFC ^name with description^ | DGfx Core         | 0.9          |

| MCPP ^name with description^ | Multichip Package |              |

Scenario: Disable re-balancing config option not set

Given the disable re-balancing config option does not exist in the datavault

And the DPTF app has been restarted since the datavault change

When I start a 3D workload such that Effective Graphics Bias is consistently > 0.85

Then the Graphics TDP Budget set by PSH is equal to DGFC PL1 max

And CPU TDP Budget set by PSH is approximately equal to TDP\_Headroom - Graphics\_TDP\_Budget

Scenario: Disable re-balancing config option set to 0

Given the disable re-balancing config option has been set to 0

And the DPTF app has been restarted since the datavault change

When I start a 3D workload such that Effective Graphics Bias is consistently > 0.85

Then the Graphics TDP budget set by PSH is equal to DGFC PL1 max

And CPU TDP budget set by PSH is approximately equal to TDP\_Headroom - Graphics\_TDP\_Budget

Scenario: Disable re-balancing config option set to 1

Given the disable re-balancing config option has been set to 1

And the DPTF app has been restarted since the datavault change

When I start a 3D workload such that Effective Graphics Bias is consistently > 0.85

Then the Graphics TDP budget set by PSH is equal to DGFC PL1 max

And CPU TDP budget set by PSH is approximately equal to TDP\_Headroom \* CPU\_Effective\_bias

\* esif shell command to delete config option: config delete @dptf "/shared/export/do\_not\_rebalance\_unused\_pid\_budget/"

\* esif shell command to set config option to 1: config set @dptf "/shared/export/do\_not\_rebalance\_unused\_pid\_budget/" 1

\* esif shell command to set config option to 0: config set @dptf "/shared/export/do\_not\_rebalance\_unused\_pid\_budget/" 0

Verify that Power Share energy threshold interrupt disable executes

Global ID:

[4-8638322](https://jama4.intel.com/perspective.req?docId=17667655&projectId=104)

ID:

[DPTF-PSPVTC-2364](https://jama4.intel.com/perspective.req?docId=17667655&projectId=104)

Description:

**Feature:** Verify that Power Share energy threshold interrupt disable executes

**Background:**

**Given** I have enabled Power Share Policy in BIOS

**And** I have launched UI in Monitor side with the Power Share Policy tab selected.

**And** I have an existing PSHA table

**And** I have the ESIF Shell open and have switched focus to the DGFC Participant

**And** I have a Gfx workload running

**Scenario:**  Verify that Power Share energy threshold interrupt disable execute

**When** I set a future Energy Threshold Counter value \*

**And** I continue to take energy readings until the Energy Threshold counter value has been exceeded

**Then** I should see that the Energy Threshold Interrupt Disable has been executed

**When** I start a Graphics workload

**Then** I will see Power Share exit slow poll if any of one of the thresholds are exceeded \*

\* Go to the Power Share wiki by following the link below:

<https://wiki.ith.intel.com/display/DPTF/Power+Share+Policy#PowerSharePolicy-EnergyThresholdInterruptDisableExecution>

Once on the Power Share wiki, go to the section: **Energy Threshold Interrupt Disable Execution** which outline the exact process for testing the interrupt functionality

Verify that Power Share slow poll exits when Thresholds exceeded

Global ID:

[4-8638324](https://jama4.intel.com/perspective.req?docId=17667692&projectId=104)

ID:

[DPTF-PSPVTC-2365](https://jama4.intel.com/perspective.req?docId=17667692&projectId=104)

Description:

**Feature:** Verify that Power Share slow poll exits when Thresholds exceeded

**Background:**

**Given** I have enabled Power Share Policy in BIOS

**And** I have launched UI in Monitor side with the Power Share Policy tab selected.

**And** I have an existing PSHA table

**And** I have the ESIF Shell open

**Scenario:**  Verify that Power Share exits slow when threshold exceeded

**When** I look in the Power Share Variables table

**And** I have no graphics workload

**Then** I will see that Power Share is currently in slow poll (call back time delta will be X)

**When** I start a Graphics workload

**Then** I will see Power Share exit slow poll if any of one of the thresholds are exceeded \*

\* The thresholds that can be exceeded to exit slow poll are any one of the following:

Processor Temperature Threshold

Graphics Utilization Threshold

Processor Utilization Threshold

SlowPoll Power Threshold

STORY: [DV-2658](https://jira01.devtools.intel.com/browse/DV-2658) ET - Gfx Energy Interrupt & Slow Poll

Verify that DGFX energy thresholds that aren't crossed during the current polling period are cleared

Global ID:

[4-8668653](https://jama4.intel.com/perspective.req?docId=17716298&projectId=104)

ID:

[DPTF-PSPVTC-2369](https://jama4.intel.com/perspective.req?docId=17716298&projectId=104)

Description:

HSD: [220251638](https://hsdes.intel.com/appstore/article/#/220251638)

**Feature:** Verify that DGFX energy thresholds that aren't crossed during the current polling period are cleared

As a Validation Engineer

I want to assure that expired DGFX energy thresholds are cleared and don't trigger events

**Background:**

**Given** I have enabled the Power Share Policy

And I have enabled all applicable Participants in BIOS

**And** I have launched the UI in Designer view

And I have a valid PSHA loaded

**Scenario:**  Verify that crossing DGFX energy threshold during slowpoll causes a polling action

**Given** That I have UI open and the Power Share Policy tab selected

**And** I have set the DGFC slowpoll energy threshold to 150J (setp 473 d0 255 150)

And I have set the CPU temperature threshold high enought aht it won't be crossed (setp 469 d0 255 100)

And I appstop/appstart dptf to refresh the policy

**When** I wait for Power Share policy to enter slowpoll

Then the policy data in the UI will update at the end of the slowpoll period

And the policy will not update in the middle of any subsequent slowpoll periods

Verify PID target initialization and throttling

Global ID:

[4-8731611](https://jama4.intel.com/perspective.req?docId=17817316&projectId=104)

ID:

[DPTF-PSPVTC-2375](https://jama4.intel.com/perspective.req?docId=17817316&projectId=104)

Description:

**Feature:** Verify PID target is properly initialized and can be throttled

Derived from HSD: cTDP forces MCP PL1 limit to max on initialization (https://hsdes.intel.com/appstore/article/#/220324884)

**Background:**

**Given** Power Share policy, MCPP, DGFC, and TCPU participants are enabled

**And** the MCPP Power Limit has been reset

 | **command**                      |

 | dstn MCPP && rstp 130 D0 0 0 |

**Scenario:** Verify PID target initializes to 65W if MCPP PL1 Max > 65W

**Given** I have set MCPP PL1 Max > 65W (such as 85W) via UI designer mode

**And** I have restarted DPTF or the system

**Then** the PID target under Power Share policy is 65W

**Scenario:** Verify PID target initializes to MCPP PL1 Max

Given cTDP policy is disabled

**And** I have set MCPP PL1 Max to 50W (something less than <65W) via UI designer mode

**And** I have restarted DPTF or the system

**Then** the PID target under Power Share policy is 50W

Scenario: Verify PID target initializes to MCPP PL1 Max (cTDP enabled)

Given cTDP policy is enabled

And  I have set MCPP PL1 Max to 50W (something less than <65W) via UI designer mode

And I have restarted DPTF or the system

Then the PID target under Power Share policy is 50W

**Scenario:** Verify PID target can be set < MCPP PL1 Max

**Given** I have set MCPP PL1 Limit to 40W (something less than MCPP PL1 Max)

 | **command**                          |

 | dstn MCPP && setp 130 D0 0 40000 |

**And** I have restarted DPTF or the system

**Then** the PID target under Power Share policy is 40W

**And** the MCPP PL1 Max is unchanged

**Scenario:** Verify PID target can be throttled

**Given** I have configured another policy, such as Passive 2 or Adaptive Performance policy to throttle MCPP PL1 Limit

**When**I cause the policy to take action and throttle MCPP

**Then** the PID target under Power Share policy changes while the policy throttles and unthrottles MCPP PL1 Limit

Verify that Power Share loop stops when MCPP Participant is removed from PSHA table

Global ID:

[4-8781011](https://jama4.intel.com/perspective.req?docId=17900960&projectId=104)

ID:

[DPTF-PSPVTC-2382](https://jama4.intel.com/perspective.req?docId=17900960&projectId=104)

Description:

**Feature:** Verify that Power Share loop stops when MCPP Participant is removed from PSHA table

**Background:**

**Given** I have enabled Power Share Policy in BIOS

**And** I have launched UI in Monitor side with the Power Share Policy tab selected.

**And** I have an existing PSHA table

**And** I have a Gfx workload running

**Scenario:**  Verify that Power Share loops stops when MCPP Participant is removed from PSHA Table

**When** I switch to the designer side for an existing PSHA Table

**And** I remove the MCPP participant from the PSHA table and save

**Then** when I switch back to monitor side, I should not see the power share loop running (Power Share Participant Status will show all X’s)

**When** I switch back to the designer side

**And** I add the MCPP participant to the PSHA table and save

**Then** when I switch back to monitor side, I should see the power share loop running again (Power Share Participant Status will have real time values)

HSD-ES: [220378701](https://hsdes.intel.com/appstore/article/#/220378701) [KBL-G Beta][PSH] Power Share loop continues running after uninstalling MCP device from device manager

Verify that with no 3D workload running: Power Share reports that DGFC is sleeping

Global ID:

[4-8787506](https://jama4.intel.com/perspective.req?docId=17910922&projectId=104)

ID:

[DPTF-PSPVTC-2384](https://jama4.intel.com/perspective.req?docId=17910922&projectId=104)

Description:

**Feature:** Verify that with no 3D workload running: Power Share reports that DGFC is sleeping

**Background:**

Given my SUT supports Power Share policy

And Power Share policy is enabled

And  a valid PSHA table with MCPP, TCPU, and DGFC participants exists

And Switchable Graphics are set to optimize or maximize performance

**Scenario:** Verify that DGFC Utilization/Energy values change depending on whether 3D workload is running

**When**I start a 3D workload

**Then** Power Share status reports Graphics Energy > 0 J

And Power Share status reports Graphcis Utilization > 0 %

**When**I stop the 3D workload

And I wait for the next PSH loop iteration

**Then** Power Share status reports Graphics Energy = 0 J

And  Power Share status reports Graphcis Utilization = X %

When I log Power Share Status data for one minute

And  I examine the log

Then all Power Share Status log messages show Graphics Energy as 0

And all Power Share Status log messages show Graphics Power as X

**Scenario:** Verify that DGFC Utilization/Energy values are reasonable with light 3D workload

When I start a light 3D workload (such as Paint 3D)

Then Power Share status reports Graphics Energy > 0 J

And  Power Share status reports Graphcis Utilization is aproximatelly 0 %

When I stop the light 3D workload

And  I wait for the next PSH loop iteration

Then Power Share status reports Graphics Energy = 0 J

And  Power Share status reports Graphcis Utilization = X %

HSD: <https://hsdes.intel.com/appstore/article/#/220343551>

HSD: <https://hsdes.intel.com/appstore/article/#/220314036>

HSD: <https://hsdes.intel.com/appstore/article/#/220387297>

Verify that Power Share continues to function after an Sx cycle

Global ID:

[4-8787903](https://jama4.intel.com/perspective.req?docId=17911779&projectId=104)

ID:

[DPTF-PSPVTC-2388](https://jama4.intel.com/perspective.req?docId=17911779&projectId=104)

Description:

**Feature:** Verify that Power Share continues to function after an Sx cycle

**Scenario:** Verify that Power Share continues to function after an S3 cycle

**Given**the SUT support Power Share policy

**And**the Power Share policy is enabled

And a PSHA table with MCPP, TCPU, and DGFC participants is active

And no 3D workload is running

**When** I enter an **S3** cycles

And  I wait for a few seconds

And  I resume from the **S3** cycle\*\*

**When** I start a 3D workload

**Then** Graphics Utilization is around 100%

And Graphics Utilization changes with each loop iteration

And Graphics Energy is greater than 0 J

And Graphics Energy changes with each loop iteration

\*Re-run the test with **S4, Reboot,**and**Shutdown (S5)** cycles

\*\* You might notice the Power Share Is Active might be momentarily True after resuming from the sleep, which is expected.

HSD: <https://hsdes.intel.com/appstore/article/#/220179177>

Verify that Power Share remains in slow poll mode as much as possible

Global ID:

[4-8788006](https://jama4.intel.com/perspective.req?docId=17912078&projectId=104)

ID:

[DPTF-PSPVTC-2389](https://jama4.intel.com/perspective.req?docId=17912078&projectId=104)

Description:

**Feature:**Verify that Power Share remains  in slow poll mode as much as possible

**Scenario:**Verify that Power Share does not into fast poll unnecessarily

**Given**the SUT support Power Share policy

**And**the Power Share policy is enabled

And a PSHA table with MCPP, TCPU, and DGFC participants is active

**And**Graphics Energy Threshold is set to a high enough value that it will not cause an interrupt

**And**Processor Temperature Threshold is set to a high enough value that it will not cause an interrupt

**And**Graphics/Processor Utilization and SlowPoll Power Thresholds are at their default values

**And**the system is mostly idle

When I start a light 3D workload (such as Paint 3D)

**And** I observe the Callback Time Delta for a minute

**Then** I can see that it's always approx. equal to the slow poll interval

**And**I don't see any Callback Time Deltas in the fast poll interval range

**When** I log the Power Share Status messages for a minute

**And** I examine the log

Then the following conditions are true for all PSH status messages logged

| *condition* |

| Callback Time Delta >= slow poll interval |

| CPU Power Calculation Time Delta >= slow poll interval |

| Graphics Power Calculation Time Delta >= slow poll interval |

Verify thet Power Share Status table in UI does not show stale values

Global ID:

[4-8788009](https://jama4.intel.com/perspective.req?docId=17912134&projectId=104)

ID:

[DPTF-PSPVTC-2390](https://jama4.intel.com/perspective.req?docId=17912134&projectId=104)

Description:

**Feature:**Verify that Power Share Status table in UI does not show stale values

**Scenario:**Verify that Power Share Status table in UI does not show stale Graphics Calculation time delta

**Given**the SUT support Power Share policy

**And**the Power Share policy is enabled

And a PSHA table with MCPP, TCPU, and DGFC participants is active

When I start a 3D workload

**And**I wait for Power Share to go into fast poll mode

**And**I stop the 3D workload

**And** I wait for Graphics Energy to start displaying 0 J

**And**I wait for Power Share to go into slow poll mode\*

**Then**the Graphics Power Calculation Time Delta continues to update with each poll

**And**the Graphics Power Calculation Time Delta is approx. equal to the CPU Power Calculation Time Delta

\*Slowpoll can be achieved by using paint 3D and leaving it idle.

Verify able to use MCPP as a source in Passive Policy 2 together with Power Share

Global ID:

[4-8788102](https://jama4.intel.com/perspective.req?docId=17912172&projectId=104)

ID:

[DPTF-PSPVTC-2391](https://jama4.intel.com/perspective.req?docId=17912172&projectId=104)

Description:

**Feature:** Verify able to use MCPP as a source in Passive Policy 2 together with Power Share

**Background:**

**Given**the SUT has MCPP participant

**And**Power Share policy is running

And a valid PSHA table with MCPP, TCPU, and DGFC participants is active

And Passive Policy 2 is set to stepwise mode

**Scenario:**Verify that when using MCPP as source in PSVT: PP2 does not start setting PL1 from MCPP PL1 min (after loading table)

**When**I create a PSVT with MCPP source such that the target used is over temp when table is saved

**And** I save the PSVT table (making it become active)

**Then** Passive Policy 2 does not start setting MCPP PL1 limit from MCPP PL1 min (125 mW)

**But** instead Passive Policy 2 starts setting MCPP PL1 limit based on MCPP "Current Power"

Scenario: Verify that when using MCPP as source in PSVT: PP2 does not start setting PL1 from MCPP PL1 min (after appstarting DPTF)

When I create a PSVT with MCPP as source

And I save the PSVT table (making it become active)

And I make sure that the target used in PSVT is over temp

And I appstop DPTF

And  I appstart DPTF

Then Passive Policy 2 does not start setting MCPP PL1 limit from MCPP PL1 min (125 mW)

But instead Passive Policy 2 starts setting MCPP PL1 limit from MCPP PL1 max

**Scenario:**Verify that when using MCPP as source in PSVT: MCPP PL1 power limit does not get stuck

When I create a PSVT with MCPP source

And I save the PSVT table (making it become active)

When I cause the PSVT target temperature to be higher than lowest PSVT trip point temperature

Then MCPP PL1 power limit is limited to below MCPP PL1 max

When I cause the PSVT target temperature to be lower than lowest PSVT trip point temperature

Then MCPP PL1 power limit is eventually unlimited to MCPP PL1 max

And the current MCPP PL1 power limit is equal to MCPP PL1 max

HSD: <https://hsdes.intel.com/appstore/article/#/220391853>

HSD: <https://hsdes.intel.com/appstore/article/#/220400808>

HSD: <https://hsdes.intel.com/appstore/article/#/220672862>

PSHA Policy behavior while limiting the CPU participant

Global ID:

[4-8915803](https://jama4.intel.com/perspective.req?docId=18115840&projectId=104)

ID:

[DPTF-PSPVTC-2410](https://jama4.intel.com/perspective.req?docId=18115840&projectId=104)

Description:

**Feature:**  PSHA Policy behavior while limiting the CPU participant

As a Validation Engineer

I want to verify that PSHA Policy is not broken while limiting the CPU participant with other policies even though it is recommended to limit MCPP participant and not the CPU participant.

**Background:**

**Given** DPTF is enabled in BIOS

**And** I have a system that supports PSHA Policy

**And** I have a PSHA with an evenly split bias between CPU and DGFX

**And** I am running a high performance graphics application

**And**I monitoring the PSHA Policy in the UI

**Scenario:**  PSHA behavior while limiting the CPU participant

**Given** I have configured **PP1** with the TCPU participant as the source

**When** The TCPU participant is fully limited by **PP1**

**And** I am monitoring PSHA in the UI

**Then** I verify that CPU Power in PSHA has been limited

**And** I verify that Total MCP Power is also limited

**And** I see that the Available TDP headroom remains unchanged

**And** I see no abnormal PSHA behavior

**Repeat above for the following Policies:  AP, PB & PID**

JIRA:  DV-2518

Verify dGPU is able to use all power allotted by Power Share

Global ID:

[4-8947610](https://jama4.intel.com/perspective.req?docId=18172335&projectId=104)

ID:

[DPTF-PSPVTC-2418](https://jama4.intel.com/perspective.req?docId=18172335&projectId=104)

Description:

**Feature:** Verify dGPU is able to use all power allotted by Power Share

Based on defect: [KBLG][Power]: Alto GPU is not operating at the right TGP values <https://hsdes.intel.com/appstore/article/#/220509523>.

Example: Power Share setting dGPU budget at 55W but graphics only consuming 20W on XL SKU under workload

**Scenario:**Verify dGPU is able to use all power allotted by Power Share (DGFC biased)

**Given**Power Share policy is enabled

**And** MCPP participant exists on the SUT

And DGFC participant exists on the SUT

And the active PSHA table is **DGFC** biased

**And**MCPP PL1 max is less than TCPU PL1 max + DGFC PL1 max

**When** I run a graphics workload that fully utilizes the dGPU**\***

**Then** Graphics TDP budget gets set to DGFC PL1 max

And the Graphics Power is close or equal to the Graphics TDP Budget (>90% of budget)**\*\*\***

Scenario: Verify dGPU is able to use all power allotted by Power Share (TCPU biased)

Given Power Share policy is enabled

And MCPP participant exists on the SUT

And DGFC participant exists on the SUT

And the active PSHA table is **TCPU** biased

**And**MCPP PL1 max is less than TCPU PL1 max + DGFC PL1 max

When I run a graphics workload that fully utilizes the dGPU\*

Then Graphics TDP budget gets set to below DGFC PL1 max

And the Graphics Power is close or equal to the Graphics TDP Budget (>90% of budget)

**\***choose a benchmark that is not CPU-limited: such as UNIGINE Superposition running at resolution of >= 1080p with highest quality/detail settings and anti-aliasing set to Off**\*\***.

**\*\***setting anti-aliasing to 4x or 8x could cause the benchmark to become graphics memory bandwidth-limited, preventing the graphics core from being fully utilized.

**\*\*\***depending on platform you may need to have a battery attached as well as the AC charger in order to provide the energy needed. If you see the Graphics Power being limited, try this configuration.

[DV-2902](https://jira01.devtools.intel.com/browse/DV-2902)

Verify policy continues to function after DPTF is updated

Global ID:

[4-9006605](https://jama4.intel.com/perspective.req?docId=18265825&projectId=104)

ID:

[DPTF-PSPVTC-2437](https://jama4.intel.com/perspective.req?docId=18265825&projectId=104)

Description:

**Feature:** Verify the policy continues to function after DPTF is updated

**Background:**

**Given**Power Share policy is enabled

**And**DGFC participant is present

**And**MCPP participant is present

**And**a valid PSHA table is applied

**Scenario:** Verify policy continues to function after DPTF is updated with no 3D workload running

**Given**no 3D workload is running

**When**I uninstall DPTF

**And**I install a new (or same) version of DPTF

**And**I reload the UI

**And**I open Power Share policy tab is open in Monitor

**And**I start a 3D workload

**Then**Graphics Utilization is changing with each PSH loop iteration

**And**Graphics Utilization is a realistic value

**And**Graphics Energy is changing with each PSH loop iteration

**And**Graphics Energy is a realistic value

**Scenario:** Verify policy continues to function after DPTF is updated with 3D workload running

**Given**a 3D workload is running

**When**I uninstall DPTF

**And**I install a new (or same) version of DPTF

**And**I reload the UI

**And**I open Power Share policy tab is open in Monitor

**And**I start a 3D workload

**Then**Graphics Utilization is changing with each PSH loop iteration

**And**Graphics Utilization is a realistic value

**And**Graphics Energy is changing with each PSH loop iteration

**And**Graphics Energy is a realistic value

<https://hsdes.intel.com/appstore/article/#/220245749>

Verify time deltas are long enough for accurate energy/power calculations

Global ID:

[4-9070708](https://jama4.intel.com/perspective.req?docId=18366269&projectId=104)

ID:

[DPTF-PSPVTC-2447](https://jama4.intel.com/perspective.req?docId=18366269&projectId=104)

Description:

**Feature:** Verify time deltas are long enough for accurate energy/power calculations

*As a validation engineer, I want to ensure that PSH fast poll loops don't become so short*

*that they negatively impact accuracy of CPU and Graphics power calculations*

**Background:**

**Given** the Power Share policy is enable

**And** the SUT has DGFC and MCPP participants

**And** a valid PSHA table is loaded

**Scenario:** Verify that fast poll mode interval is ~ 100ms

**When** I set the Graphics utilization threshold to 0%

**And** I set the Processor utilization threshold to 0%

**And** I set the Power threshold to 0 mW

**And** I re-start the dptf application

**And** I run a 3D graphics workload

**And** I record PSH messages for one minute

**Then** all callback time deltas are 100ms (± 20ms)

**And** all CPU power calculation time deltas are 100ms (± 20ms)

**And** all Graphics power calculation time deltas are 100ms (± 20ms)

**Scenario:** Verify that fast poll mode interval is ~ 100ms (low CPU temp. threshold)

**When** I set the Graphics utilization threshold to 0%

**And** I set the Processor utilization threshold to 0%

**And** I set the Power threshold to 0 mW

**And** I set the Processor temperature threshold such that under load CPU temp. is frequently greater than the threshold

**And** I re-start the dptf application

**And** I run a 3D graphics workload

**And** I record PSH messages for one minute

**Then** all callback time deltas are 100ms (± 20ms)

**And** all CPU power calculation time deltas are 100ms (± 20ms)

**And** all Graphics power calculation time deltas are 100ms (± 20ms)

**Scenario:** Verify that fast poll mode interval is ~ 100ms (low Graphics energy threshold)

**When** I set the Graphics utilization threshold to 0%

**And** I set the Processor utilization threshold to 0%

**And** I set the Power threshold to 0 mW

**And** I set the Graphics energy threshold to lowest value possible

**And** I re-start the dptf application

**And** I run a 3D graphics workload

**And** I record PSH messages for one minute

**Then** all callback time deltas are 100ms (± 20ms)

**And** all CPU power calculation time deltas are 100ms (± 20ms)

**And** all Graphics power calculation time deltas are 100ms (± 20ms)

<https://hsdes.intel.com/appstore/article/#/220338280>

Verify status and participant logging supports dedicated graphics

Global ID:

[4-9087407](https://jama4.intel.com/perspective.req?docId=18393949&projectId=104)

ID:

[DPTF-PSPVTC-2450](https://jama4.intel.com/perspective.req?docId=18393949&projectId=104)

Description:

**Feature:** Verify status and participant logging supports new tags for DGFX

As a user,

I want the UI to inform me when I have typed something incorrectly

**Background**:

**Given** I am on a system with dedicated graphics

**And** the system is compatible with Power Share Policy

**And** Power Share Policy is enabled

**And** the DGFC participant is enabled

**Scenario**: Verify status command supports dedicated graphics

**Given** I start a graphics load

**And** I open the ESIF shell

**When** I run the "status" command in the shell

**Then** the output for the "DGFC" participant" contains "energyCounter", "instantaneousPower", "acPeakPower", and "dcPeakPower" tags

**And** the values in the tags are the approximately the same as the corresponding values in the Power Share Participant Status table in the monitor

**Scenario**: Verify participant logging supports dedicated graphics

**Given** I start a graphics load

**When** I start participant logging (UI or ESIF shell) for the "DGFC" participant

**And** I stop participant logging several seconds later

**And** I navigate to the participant log file

**Then** there are columns for "DGFC\_Energy Counter", "DGFC\_Instantaneous Power", "AC Peak Power", and "DC Peak Power"

**And** the values in the columns are approximately the same as the corresponding values in the Power Share Participant Status table in the monitor

Jira Story: [DPTF-2425](https://jira01.devtools.intel.com/browse/DPTF-2425)

Verify default PID target and Kp values

Global ID:

[4-9156806](https://jama4.intel.com/perspective.req?docId=18535720&projectId=104)

ID:

[DPTF-PSPVTC-2474](https://jama4.intel.com/perspective.req?docId=18535720&projectId=104)

Description:

**Feature:** Verify default PID target and Kp values

As a user,

I want the default PID target and Kp values to stay the same

**Background**:

**Given** I am on a system with dedicated graphics

**And** the system is compatible with Power Share Policy

**And** Power Share Policy is enabled

**And** there are **no** overrides for DPTF

**Scenario**: Verify default PID target and Kp values

**Given** I open Power Share Policy in the monitor

**When** I take note of the value for MCPP PL1 Max Power Limit

**And** I check the PID target

**Then** I see the value for MCPP PL1 Max Power Limit

**When** I check the Kp value

**Then** I see a value of 0.8

Jira Story: [DPTF-2480](https://jira01.devtools.intel.com/browse/DPTF-2480)

Verify that the DGFC participant is not listed as a source in Passive Policy 2 or PID Policies

Global ID:

[4-9157217](https://jama4.intel.com/perspective.req?docId=18536470&projectId=104)

ID:

[DPTF-PSPVTC-2475](https://jama4.intel.com/perspective.req?docId=18536470&projectId=104)

Description:

**Feature:** Verify that the DGFC participant is not listed as a source in any policy

**Background:**

**Given** I have enabled Power Share Policy in BIOS

**And**I have launched UI in Monitor side with the Power Share Policy tab selected.

**And**I have an existing PSHA table

**Scenario:**  Verify that the DGFC participant is not listed as a source in Passive Policy 2

**When**I look in all the Passive Policy 2 designer tab

**And**I click on the source drop down menu

**Then** I will NOT see the DGFC Participant

**Repeat for all policies that support a Source**

HSD-ES: [[MUST FIX][KBL-G Beta] Cannot use DGFC as a \*target\* + cannot change AC/DC peak power in PB](https://hsdes.intel.com/appstore/article/#/220647303)

Verify that PlxPowerLimit for DGFC participant have been filtered out from the AP/PB policies.

Global ID:

[4-9157307](https://jama4.intel.com/perspective.req?docId=18536536&projectId=104)

ID:

[DPTF-PSPVTC-2476](https://jama4.intel.com/perspective.req?docId=18536536&projectId=104)

Description:

**Feature:** Verify that PlxPowerLimit for DGFC participant have been filtered out from the AP/PB policies.

**Background:**

**Given** I have enabled Power Share Policy in BIOS

**And**I have launched UI in the designer side

**And**I have an existing PSHA table

**Scenario:**  Verify that DGFC participant does not have the PlxPowerLimit  in the APAT Code drop down menu

**When**I look in the Adaptive Performance designer tab

**And**I click on the APAT Code dropdown menu

**Then** I will NOT see PlxPowerLimit in the Code dropdown menu

**Scenario:**  Verify that DGFC participant does not have the PlxPowerLimit  in the PBAT Code drop down menu

**When**I look in the PowerBoss designer tab

**And**I click on the PBAT Code dropdown menu

**Then** I will NOT see PlxPowerLimit in the Code dropdown menu

HSD-ES: [[MUST FIX][KBL-G Beta] Cannot use DGFC as a \*target\* + cannot change AC/DC peak power in PB](https://hsdes.intel.com/appstore/article/#/220647303)

Verify policy does not react to temperature threshold crossed events caused by other policies

Global ID:

[4-9171699](https://jama4.intel.com/perspective.req?docId=18561488&projectId=104)

ID:

[DPTF-PSPVTC-2479](https://jama4.intel.com/perspective.req?docId=18561488&projectId=104)

Description:

**Feature:** Verify the policy does not react to temperature threshold crossed events caused by other policies

**Scenario:**Verify the policy does not react to temperature threshold crossed events caused by other policies

**Given**PSH policy is enabled

**And**Passive Policy 2 is enabled

**And**MCPP, DGFC, and TCPU participants are present

**And**a valid PSH table is active

**And**PSH policy is not in fast poll mode

**And**PSVT is set to use TCPU as target with a temperature trip point well below the PSH processor temperature threshold

**When**I increase the TCPU temperature just above the PSVT trip point temperature

**Then**the temperature threshold crossed event does not cause PSH to perform an iteration of the control loop

**And**the PSH policy does not disable its TCPU temperature threshold

**Scenario:**Verify the policy does not react to temperature threshold crossed events caused by other policies (fast poll mode)

**Given**PSH policy is enabled

**And**Passive Policy 2 is enabled

**And**MCPP, DGFC, and TCPU participants are present

**And**a valid PSH table is active

**And**PSH policy is in fast poll mode

**And**PSVT is set to use TCPU as target with a temperature trip point well below the PSH processor temperature threshold

**When**I increase the TCPU temperature just above the PSVT trip point temperature

**And**I observe the PSH behavior for at least one minute

**Then**the temperature threshold crossed event does not cause PSH to perform an iteration of the control loop

**And**the callback time delta is consistently about 100ms\*

\*the idea is to make sure that callback time delta is never a really low value: like 10ms or less

<https://hsdes.intel.com/appstore/article/#/220642221>

<https://hsdes.intel.com/appstore/article/#/220994759>

Verify Power Share loop stays in slow poll mode when DGFC is not active

Global ID:

[4-9229812](https://jama4.intel.com/perspective.req?docId=18641940&projectId=104)

ID:

[DPTF-PSPVTC-2489](https://jama4.intel.com/perspective.req?docId=18641940&projectId=104)

Description:

**Feature:** Verify Power Share loop stays in slow poll mode when DGFC is not active

**Scenario:** Slow Poll mode with high CPU utilization

**Given**Power Share Policy is enabled

**And**MCPP, DGFC, and TCPU participants are present

**And**a valid PSHA table is active

**And**I start a CPU workload

**And** CPU utilization is greater than Processor Utilization Threshold

**And** I log Power Share status messages for 1 minute

**And** I analyze Power Share loop frequency

**Then**the Power Share loop ran once per Slow Polling Interval

<https://hsdes.intel.com/appstore/article/#/220700866>

DPTF sets PID target defined in dptf.dv

Global ID:

[4-9240407](https://jama4.intel.com/perspective.req?docId=18664869&projectId=104)

ID:

[DPTF-PSPVTC-2497](https://jama4.intel.com/perspective.req?docId=18664869&projectId=104)

Description:

**Feature:**DPTF sets PID target defined in dptf.dv

**Background:**

**Given**I’m using a platform with MCPP (Multi Chip Participant)

**And** MCP PL1 power limit key exists in dptf.dv and is less than MCP PL1 Max\*

**Scenario:**On DPTF startup MCP PL1 Max set to value in dptf.dv

**Given**I have uninstalled the DPTF Manger (don’t delete)

**And** I delete the override.dv

**When**I click “scan for hardware changes” in Device Manager (starts DPTF manager)

**Then** I see the PID target set in Power Share Policy is equal to MCP PL1 power limit in dptf.dv

**And** The PID target is not set equal to MCP PL1 Max

**Scenario:**Policy sets MCP PL1 power limit less than value in dptf.dv, lower value is honored

**When**I use **<a policy>** to set MCP PL1 power limit less than the value in dptf.dv

**Then** I see the PID target set in Power Share Policy is set to that value

**And** The PID target is not equal to MCP PL1 Power Limit in dptf.dv

**When**I use **<a policy>** to set MCP PL1 power limit greater than the value in dptf.dv

**Then** I see the PID target set in Power Share Policy is NOT set to that value

**And** The PID target is equal to MCP PL1 Power Limit in dptf.dv

**REPEAT: Using multiple policies (Power Boss, Adaptive Performance, etc)**

\*To set MCP PL1 Power Limit in Esif shell run “config set @dptf /participants/MCPP.D0/rpl0 <value>”

[HSD: 220674303](https://hsdes.intel.com/appstore/article/#/220674303)

Verify that discrete graphics participants report temperature

Global ID:

[4-9325495](https://jama4.intel.com/perspective.req?docId=18801460&projectId=104)

ID:

[DPTF-PSPVTC-2503](https://jama4.intel.com/perspective.req?docId=18801460&projectId=104)

Description:

**Feature:** Verify that discrete graphics participants report temperature

**Scenario:** Verify that **DGFC**participant reports temperature

**Given**that **DGFC**participant is enabled

**And**a 3D workload app is open

**Then DGFC**is reporting a realistic temperature

**When**I start running the 3D workload

**Then**the **DGFC**temperature increases

**When**I stop running the 3D workload

**But**the 3D workload app is still open

**Then**the **DGFC**temperature decreases

Repeat for the **DGHM**participant

<https://hsdes.intel.com/appstore/article/#/220336898>

<https://hsdes.intel.com/appstore/article/#/220677307>

Verify PSHA Policy behavior with switchable graphics

Global ID:

[4-9443420](https://jama4.intel.com/perspective.req?docId=18993215&projectId=104)

ID:

[DPTF-PSPVTC-2518](https://jama4.intel.com/perspective.req?docId=18993215&projectId=104)

Description:

**Feature:** Verify PSHA Policy behavior with switchable graphics

As a Validation Engineer

I want to verify that PSHA Policy reacts properly to OS Power Options switchable graphics settings.

**Background:**

**Given** I have a system that supports PSHA Policy

**And** I have configured a PSHA table

**And** I have set the Power Options switchable graphics on battery to Force power-saving graphics

**And** I have set the Power Options switchable graphics on plugged in to Optimize Performance

**And**I monitoring the PSHA Policy in the UI

**Scenario:** PSHA behavior with switchable graphics

**Given** I have installed a 3D graphics benchmark

**And** The system is powered by AC

**When** I launch a 3D benchmark

**Then** I see the PSHA policy is monitoring CPU and Gfx power

**And** I verify that the Alto graphics driver is being used

**When** I **change** the system power to DC

**And** I launch a 3D graphics benchmark

**Then** I see the PSHA policy is not active

**And** I verify that the Intel graphics driver is selected

**When** I **change** the system power back to AC

**And** I launch a 3D graphics benchmark

**Then** I see the PSHA policy is monitoring CPU and Gfx power

**And** I verify that the Alto graphics driver is being used

Repeat scenario: by **changing** power source while in S3, CS & S4

Note: FurMark 3D benchmark shows which graphics driver is active. [\\chakotay\SoftVal\DPTF\_tools\Benchmark\_Tools](file:///\\chakotay\SoftVal\DPTF_tools\Benchmark_Tools)

JIRA: DV-2798

Verify PSHA Policy behavior during CPU Temperature Threshold Crossing

Global ID:

[4-9443711](https://jama4.intel.com/perspective.req?docId=18993718&projectId=104)

ID:

[DPTF-PSPVTC-2519](https://jama4.intel.com/perspective.req?docId=18993718&projectId=104)

Description:

**Feature:** Verify PSHA Policy behavior during CPU Temperature Threshold Crossing

**Background:**

**Given** I have a system that supports PSHA Policy

**And** I have configured a PSHA table

**And**I monitoring the PSHA Policy in the UI

**Scenario:** PSHA behavior while CPU threshold crossing during slow polling

**Given** I am running a low level graphics benchmark **\*\***

**And** I confirm PSHA is running in slow polling mode

**And** I have configured any other policy to generate a CPU temperature threshold crossing event **\*\*\***

**When** I generate a CPU temperature threshold crossing event

**Then** I see the PSHA policy remains unchanged and is still in slow polling mode

**And** I do not see any abnormal PSHA behavior

**Scenario:** PSHA behavior while CPU threshold crossing during fast polling

**Given** I am running a 3D graphics benchmark

**And** I confirm PSHA is running in fast polling mode

**And** I have configured any other policy to generate a CPU temperature threshold crossing event **\*\*\***

**When** I generate a CPU temperature threshold crossing event

**Then** I see the PSHA policy remains unchanged and is still in fast polling mode

**And** I do not see any abnormal PSHA behavior

**\*\* Note:** Power Share Variables can also be adjusted to force slow polling

**\*\*\* Note:**Policies that can generate CPU temp threshold events (ACT2, AP, PP2, PID and VIRT)

JIRA: DV-2910

Verify PSHA Policy Tau changes when discrete Gfx is active

Global ID:

[4-9544508](https://jama4.intel.com/perspective.req?docId=19181453&projectId=104)

ID:

[DPTF-PSPVTC-2529](https://jama4.intel.com/perspective.req?docId=19181453&projectId=104)

Description:

**Feature:** Verify PSHA Policy Tau changes when discrete Gfx is active

**Background:**

**Given** I have a system that supports PSHA Policy

**And** I have configured a PSHA table

**And**I monitoring the PSHA Policy and CPU Participant in the UI

**And** I have installed a 3D graphics benchmark

**Scenario:** PSHA behavior with combined discrete/integrated Gfx

**Given** I have a monitor connected to the combined discrete/integrated Gfx port\*

**When** I launch a 3D benchmark

**Then** I see the PSHA policy “Power Share is Active” = true

**And** I see that PL1 Time Window (Tau) has been set to 5 seconds

**When** I stop the 3D benchmark

**Then** I see the PSHA policy “Power Share is Active” = false

**And** I see that PL1 Time Window (Tau) has been set to 28 seconds\*\*

**Scenario:** PSHA behavior with discrete only Gfx

**Given** I have a monitor connected to the discrete only Gfx port

**When** I launch a 3D benchmark

**Then** I see the PSHA policy “Power Share is Active” = true

**And** I see that PL1 Time Window (Tau) has been set to 5 seconds

**When** I stop the 3D benchmark

**Then** I still see the PSHA policy “Power Share is Active” = True

**And** I see that PL1 Time window (Tau) is still set to 5 seconds

JIRA: DV-2592

Verify that Power Share resets TCPU aux1 when 3D workload is stopped

Global ID:

[4-9562213](https://jama4.intel.com/perspective.req?docId=19208502&projectId=104)

ID:

[DPTF-PSPVTC-2536](https://jama4.intel.com/perspective.req?docId=19208502&projectId=104)

Description:

**Feature:** Verify that Power Share resets TCPU aux1 when 3D workload is stopped

**Scenario:** Verify that Power Share resets TCPU aux1 when 3D workload is stopped

**Given**the Power Share policy is enabled on the system\*\*  
**And**a valid PSHA table is defined and active  
**When**I start a low-intensity 3D workload (such as Paint 3D)  
**And**I start another more-intensive 3D workload (such as x29.exe)  
**And**I wait for Power Share to go into fast poll mode  
**And**I stop the more-intensive 3D workload  
**And**I wait for Power Share to go into slow poll mode  
**And**I leave the system idle such that CPU temperature drops below 50.0**\*** deg. C  
**Then**I see PSH set TCPU aux1 to 50.0**\*** deg. C  
**When**I stop the low-intensity workload  
**Then**I see PSH set TCPU aux1 to 200.0 deg. C\*\*\*

**\***default "Processor temperature threshold value" for Power Share

\*\* make sure there are no other policies are enabled to avoid any policy setting its own CPU Aux1 values.

\*\*\* Could be 199.0 deg C instead of 200.

<https://hsdes.intel.com/appstore/article/#/220999361>

Verify PSHA Policy default Tau after Sx cycle

Global ID:

[4-9562308](https://jama4.intel.com/perspective.req?docId=19208646&projectId=104)

ID:

[DPTF-PSPVTC-2537](https://jama4.intel.com/perspective.req?docId=19208646&projectId=104)

Description:

**Feature:** Verify PSHA Policy default Tau after Sx cycle

**Background:**

**Given** I have a system that supports PSHA Policy

**And** I have configured a PSHA table

**And** I have system that does not support cTDP (i.e. QS chipset)

**And** I have no Policies configured to change PL1 Time Window (Tau)

**And** I have not made any changes affecting the PPCC

**Scenario:** TCPU Tau behavior after Sx cycle

**When** I view the TCPU(0) Participant in the Monitor UI

**Then** I see the current PL1 Time Window = PL1 Max Time Window

**When** I perform an **S3**power cycle

**Then** I see the current PL1 Time Window remains unchanged

Repeat: **S4**

https://hsdes.intel.com/appstore/article/#/2201032630

Verify Power Share policy works without having the UI/shell installed/available

Global ID:

[4-9922304](https://jama4.intel.com/perspective.req?docId=19794985&projectId=104)

ID:

[DPTF-PSPVTC-2588](https://jama4.intel.com/perspective.req?docId=19794985&projectId=104)

Description:

**Scenario:**

**Given** I have a PSHA table with some BIAS

**And** I do not have any DPTF UI installed on the SUT  
**And** the ESIF shell is not enabled in a start or startup.dv file

**And** no tracing or logging is on

**And** I am monitoring PL1 values for discrete graphics and CPU in TAT

**When** I start a 3D graphics workload

**Then** the PL1 values between CPU and discrete graphics fluctuate

**When** I stop the workload

**Then** the controls eventually reach the initial limit values

Verify BIAS fields must sum to 1.0

Global ID:

[4-11694778](https://jama4.intel.com/perspective.req?docId=22536308&projectId=104)

ID:

[DPTF-PSPVTC-2989](https://jama4.intel.com/perspective.req?docId=22536308&projectId=104)

Description:

**Feature:** Verify that BIAS fields must sum to 1.0

**Scenario:**Verify BIAS fields cannot sum to greater than 1.0

**Given** Power Share policy is enabled

**And** the PSHA table is configured with some default state (MCPP, DGFC, TCPU)

**When** I edit the table so that the total Default BIAS sum for the table is >1.0 (0.9 and 0.9 for example)

**Then**an error is displayed to the user

| message |

| Must be tenths decimal within this range [0.1, 0.9] and Total Default Bias of all participants must be = 1 |

**And** the table Save button is disabled

**When** I update the Default BIAS so that the total sum equals 1

**Then**the table Save button is enabled

**And** there is no error message

**REPEAT using at least 4 editable BIAS fields**

**Scenario:**Verify BIAS fields cannot sum to less than 1.0

**Given** Power Share policy is enabled

**And** the PSHA table is configured with some default state (MCPP, DGFC, TCPU)

**When** I edit the table so that the total Default BIAS sum for the table is <1.0 (0.3 and 0.2 for example)

**Then**an error is displayed to the user

| message |

| Must be tenths decimal within this range [0.1, 0.9] and Total Default Bias of all participants must be = 1 |

**And** the table Save button is disabled

**When** I update the Default BIAS so that the total sum equals 1

**Then**the table Save button is enabled

**And** there is no error message

**REPEAT using at least 4 editable BIAS fields**

**HSD: https://hsdes.intel.com/appstore/article/#/2206199802**

Automation Story:

https://jira.devtools.intel.com/browse/DV-4825

Verify Input validation error message disappears when field becomes disabled

Global ID:

[4-11694980](https://jama4.intel.com/perspective.req?docId=22536512&projectId=104)

ID:

[DPTF-PSPVTC-2990](https://jama4.intel.com/perspective.req?docId=22536512&projectId=104)

Description:

**Feature:**Verify Input validation error message disappears when field becomes disabled

**Scenario:**Verify the input validation error message disappears when the errored field becomes disabled

**Given** I have a KBL-G with Power Share enabled

**And**I have configured a valid PSHA table

**When**I input an invalid value for the DGFC/TCPU participant

**Then**an error message appears

**When**I change the participant for the errored row to MCPP

**Then**the input field is disabled

**And**the error message is removed

Automation Story: https://jira.devtools.intel.com/browse/DV-4826

HSD: https://hsdes.intel.com/appstore/article/#/2206201120

Verify PPCC Input Validation Button States for DGFC

Global ID:

[4-11664019](https://jama4.intel.com/perspective.req?docId=22482228&projectId=104)

ID:

[DPTF-PSPVTC-2970](https://jama4.intel.com/perspective.req?docId=22482228&projectId=104)

Description:

**Scenario:** Verify PPCC Input Validation Button States for DGFC

**Given** the DGFC participant exists in the participant dropdown  
**When** I open the "DGFC" Participants tab in Designer mode  
**Then** the PPCC table's buttons are presented as expected

| *tableName* | *buttonName* | *buttonContext* | *clickability* | *tooltip* |

| PPCC | Save | table | clickable | Save |

| PPCC | Reset | table | clickable | Reset this table to system defaults |

| PPCC | Cancel | table | not clickable | Cancel all changes in this table |

**When** I change MIN to -8564865 for row 0 of PPCC  
**Then** there is an input error with message "Must be an integer within this range: [0, PLMax]"  
**And** the PPCC table's data row cells are editable as expected except for

| *tableName* | *columnName* | *row* |

**And** the PPCC table's buttons are presented as expected

| *tableName* | *buttonName* | *buttonContext* | *clickability* | *tooltip* |

| PPCC | Save | table | not clickable | Errors in table |

| PPCC | Reset | table | clickable | Reset this table to system defaults |

| PPCC | Cancel | table | clickable | Cancel all changes in this table |

**When** I change MIN to 150 for row 0 of PPCC  
**Then** there is no input error message  
**And** the PPCC table's buttons are presented as expected

| *tableName* | *buttonName* | *buttonContext* | *clickability* | *tooltip* |

| PPCC | Save | table | clickable | Save |

| PPCC | Reset | table | clickable | Reset this table to system defaults |

| PPCC | Cancel | table | clickable | Cancel all changes in this table |

Verify PPCC Input Validation Button States for MCPP

Global ID:

[4-11664020](https://jama4.intel.com/perspective.req?docId=22482239&projectId=104)

ID:

[DPTF-PSPVTC-2971](https://jama4.intel.com/perspective.req?docId=22482239&projectId=104)

Description:

**Scenario:**Verify PPCC Input Validation Button States for MCPP

**Given** the MCPP participant exists in the participant dropdown  
**When** I open the "MCPP" Participants tab in Designer mode  
**Then** the PPCC table's buttons are presented as expected

| *tableName* | *buttonName* | *buttonContext* | *clickability* | *tooltip* |

| PPCC | Save | table | clickable | Save |

| PPCC | Reset | table | clickable | Reset this table to system defaults |

| PPCC | Cancel | table | not clickable | Cancel all changes in this table |

**When** I change MIN to -8564865 for row 0 of PPCC  
**Then** there is an input error with message "Must be an integer within this range: [0, PLMax]"  
**And** the PPCC table's data row cells are editable as expected except for

| *tableName* | *columnName* | *row* |

**And** the PPCC table's buttons are presented as expected

| *tableName* | *buttonName* | *buttonContext* | *clickability* | *tooltip* |

| PPCC | Save | table | not clickable | Errors in table |

| PPCC | Reset | table | clickable | Reset this table to system defaults |

| PPCC | Cancel | table | clickable | Cancel all changes in this table |

**When** I change MIN to 150 for row 0 of PPCC  
**Then** there is no input error message  
**And** the PPCC table's buttons are presented as expected

| *tableName* | *buttonName* | *buttonContext* | *clickability* | *tooltip* |

| PPCC | Save | table | clickable | Save |

| PPCC | Reset | table | clickable | Reset this table to system defaults |

| PPCC | Cancel | table | clickable | Cancel all changes in this table |

Short Name:

Verify PPCC Input Validation Button States for TCPU

Global ID:

[4-11663973](https://jama4.intel.com/perspective.req?docId=22482071&projectId=104)

ID:

[DPTF-PSPVTC-2968](https://jama4.intel.com/perspective.req?docId=22482071&projectId=104)

Description:

**Scenario:**Verify PPCC Input Validation Button States for TCPU

**Given** the TCPU participant exists in the participant dropdown  
**When** I open the "TCPU" Participants tab in Designer mode  
**Then** the PPCC table's buttons are presented as expected

| *tableName* | *buttonName* | *buttonContext* | *clickability* | *tooltip* |

| PPCC | Save | table | clickable | Save |

| PPCC | Reset | table | clickable | Reset this table to system defaults |

| PPCC | Cancel | table | not clickable | Cancel all changes in this table |

**When** I change Step to -500 for row 0 of PPCC  
**Then** there is an input error with message "Must be an integer within this range: [0, 999000]"  
**And** the PPCC table's data row cells are editable as expected except for

| *tableName* | *columnName* | *row* |

**And** the PPCC table's buttons are presented as expected

| *tableName* | *buttonName* | *buttonContext* | *clickability* | *tooltip* |

| PPCC | Save | table | not clickable | Errors in table |

| PPCC | Reset | table | clickable | Reset this table to system defaults |

| PPCC | Cancel | table | clickable | Cancel all changes in this table |

**When** I change Step to 150 for row 0 of PPCC  
**Then** there is no input error message  
**And** the PPCC table's buttons are presented as expected

| *tableName* | *buttonName* | *buttonContext* | *clickability* | *tooltip* |

| PPCC | Save | table | clickable | Save |

| PPCC | Reset | table | clickable | Reset this table to system defaults |

| PPCC | Cancel | table | clickable | Cancel all changes in this table |

verify power share table requires both TCPU and Graphics participants

Global ID:

[4-13212773](https://jama4.intel.com/perspective.req?docId=25008641&projectId=104)

ID:

[DPTF-PSPVTC-3291](https://jama4.intel.com/perspective.req?docId=25008641&projectId=104)

Description:

**Feature**: Verify that power share table requires both MCPP, TCPU  and graphics participants.

**Scenario**: Power split set to 100% to CPU when only TCPU and MCPP are bound

**Given** Power Share policy is enabled

**When**the PSHA table consists of entries of only TCPU and MCPP

**Then**table can not be saved pops an error message**.**

**When**the PSHA table consists of entries of only DGFC and MCPP

**Then** table can not be saved pops an error message**.**