Ethernet / TCP-IP - Training Suite

01 – Ethernet Background

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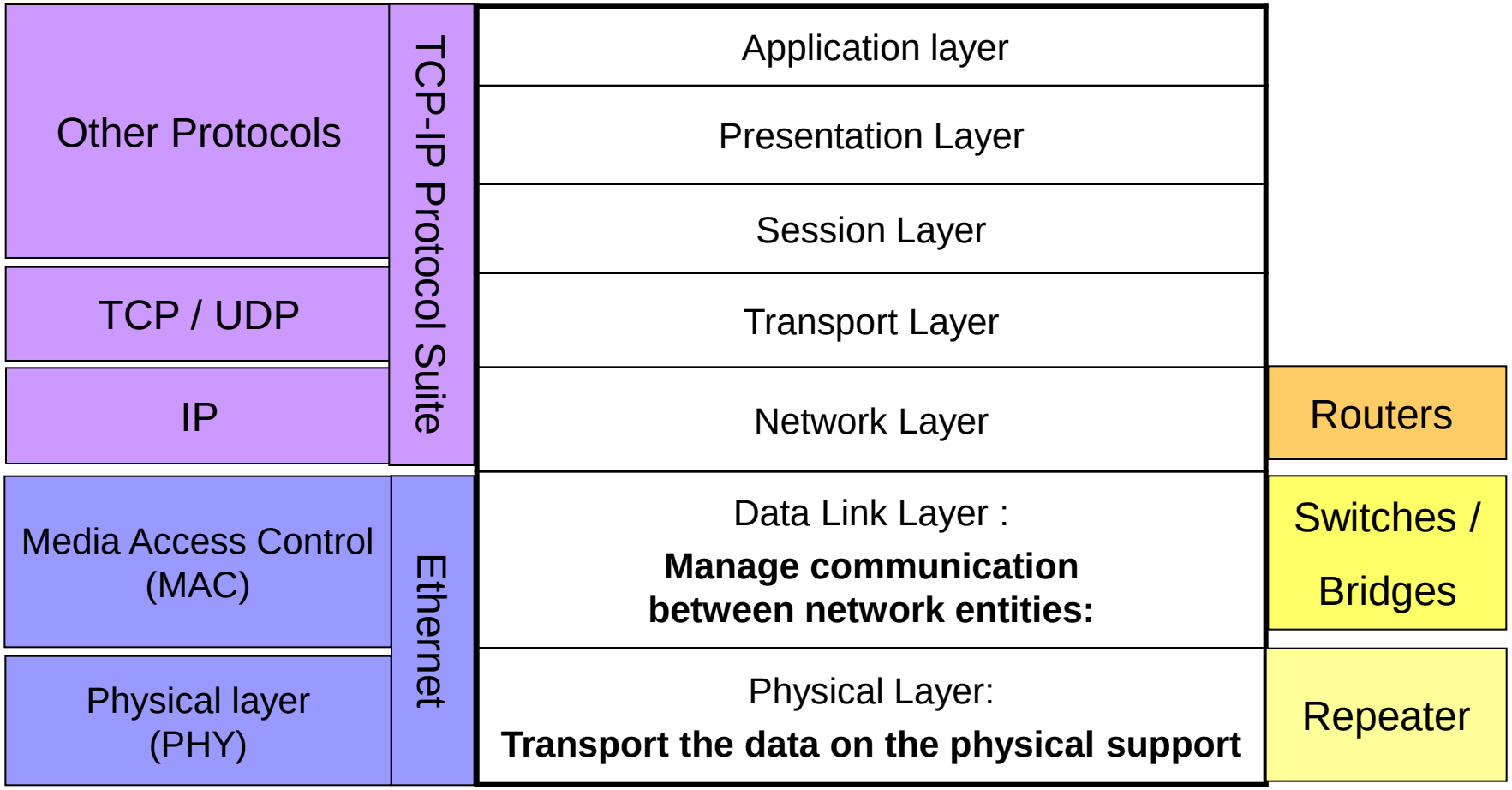
Content

What is Ethernet

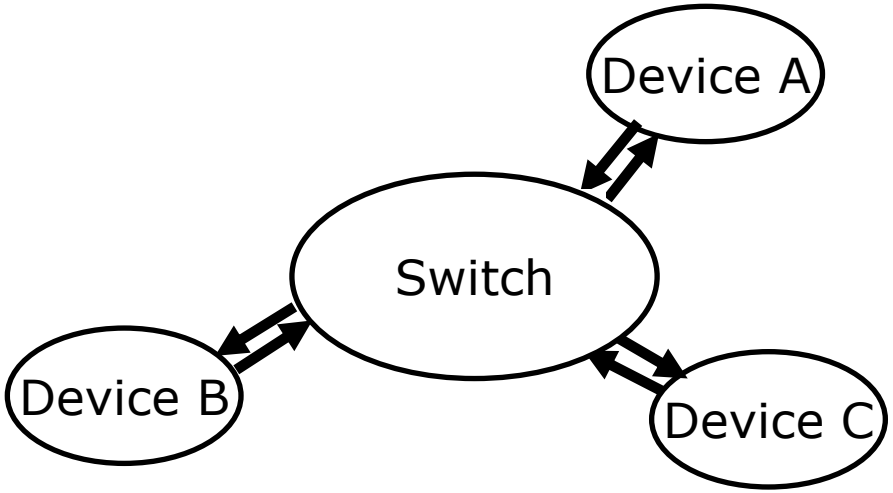
- Ethernet and OSI model
- Full Duplex Vs. Half Duplex
- Ethernet Frame Format
- Mac addresses

The OSI model

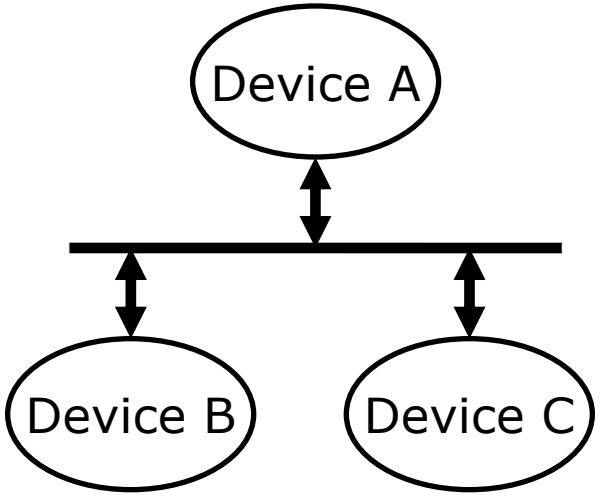


Full Duplex Vs. Half Duplex

- Full Duplex
  - A network with a star architecture
  - Point to point connection between each device

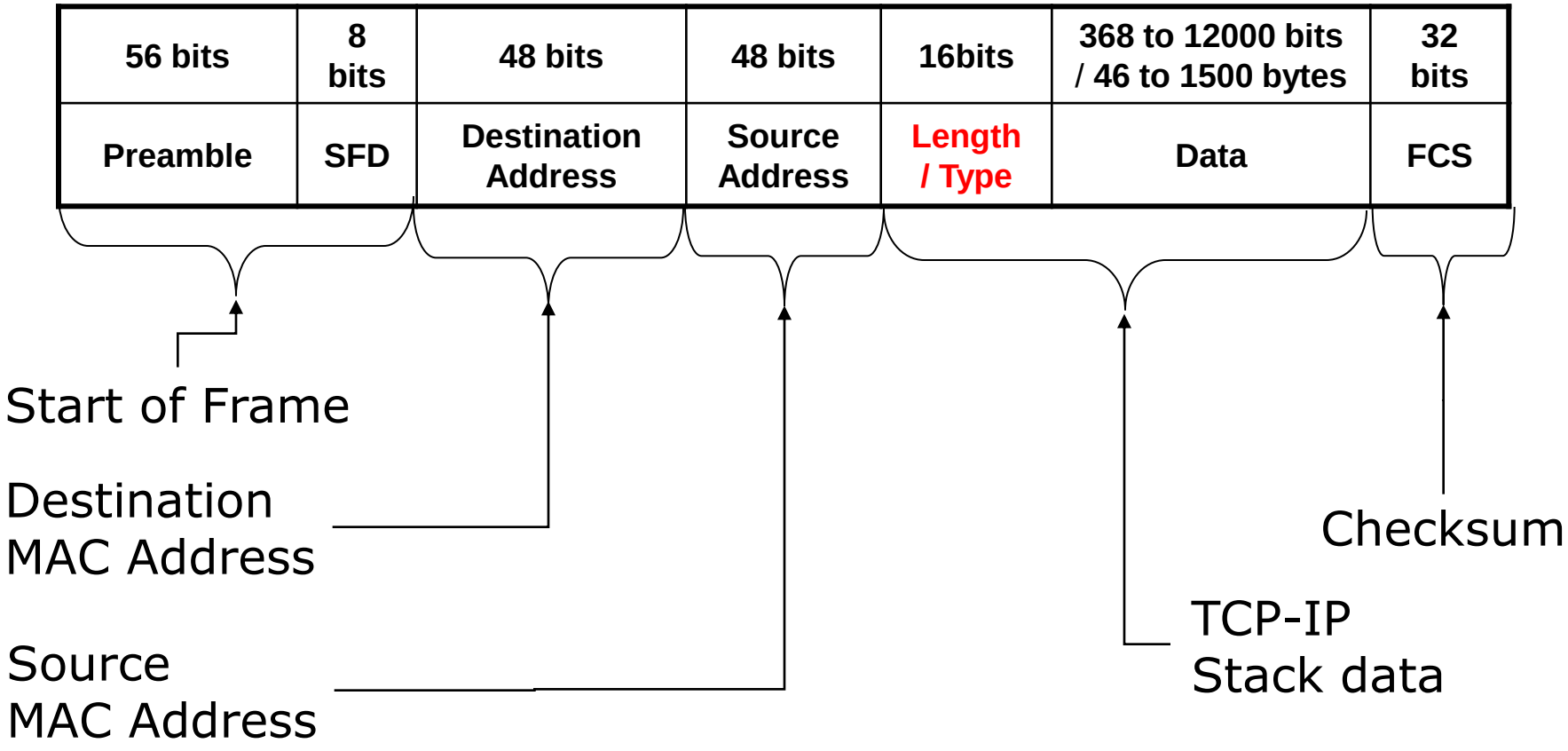


- Half Duplex
  - A network with a bus architecture
  - Use a carrier sensing scheme with collision detection CSMA/CD



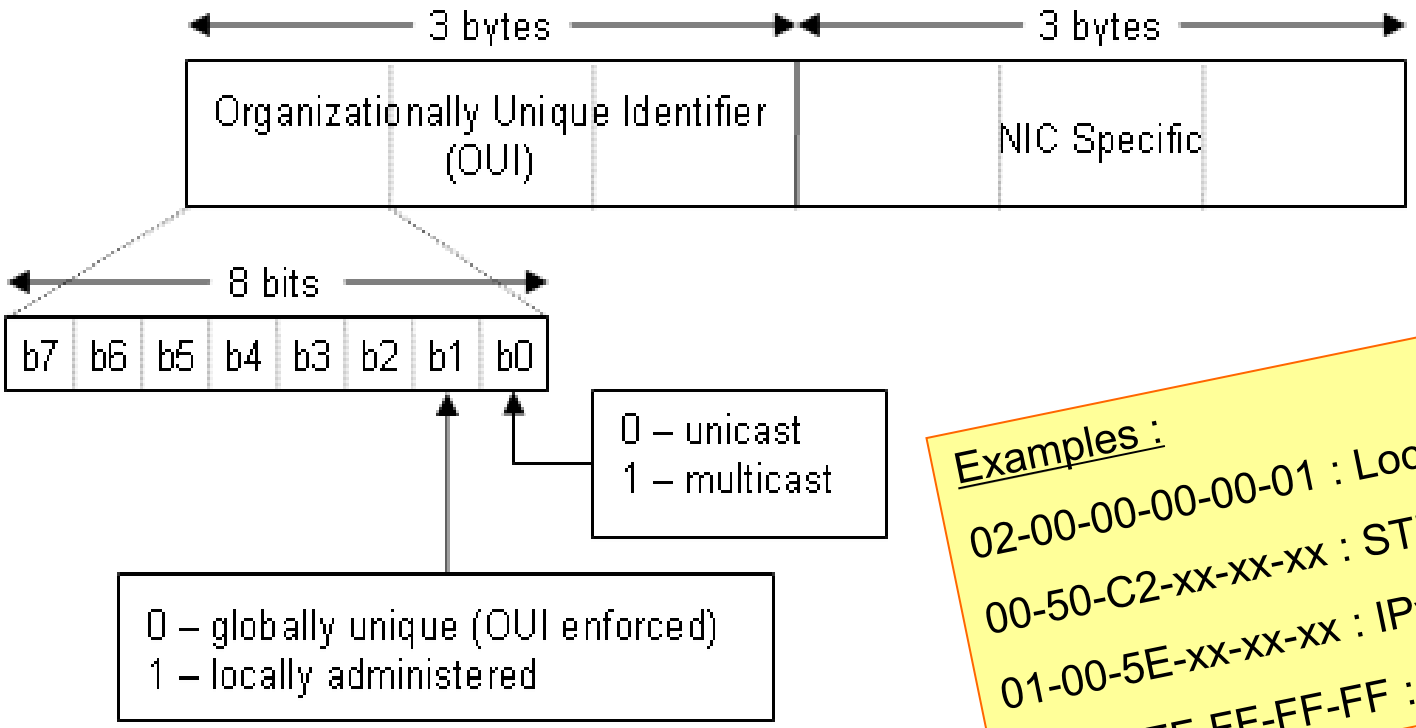
MAC 802.3 Operation : the frame format

Basic MAC 802.3 frame format



Ethernet Frames (MAC Addresses)

It is a number (XX-XX-XX-XX-XX-XX) that acts like a name for a particular network adapter



Examples :

02-00-00-00-00-01 : Locally assigned

00-50-C2-xx-xx-xx : STMicroelectronics

01-00-5E-xx-xx-xx : IPv4 Multicast

FF-FF-FF-FF-FF-FF : Broadcast

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02 – Ethernet schematics

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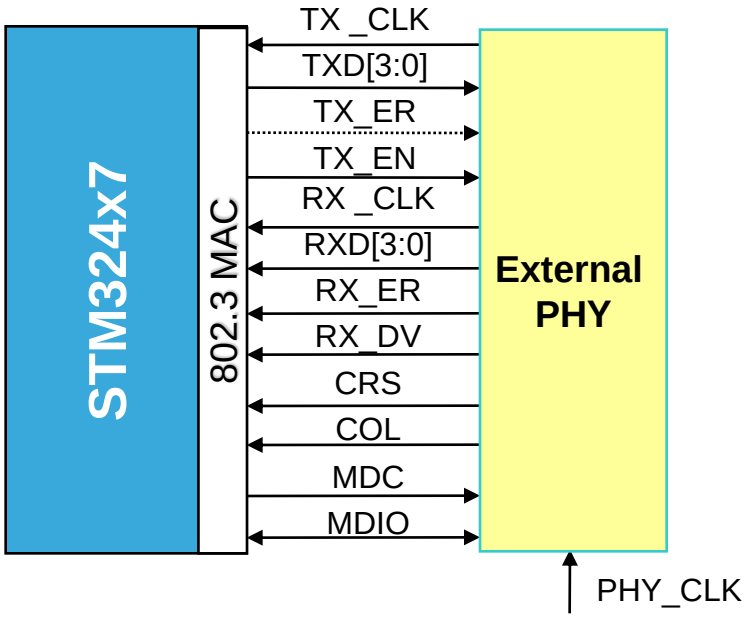
Content

STM32F4x7 Ethernet schematic examples

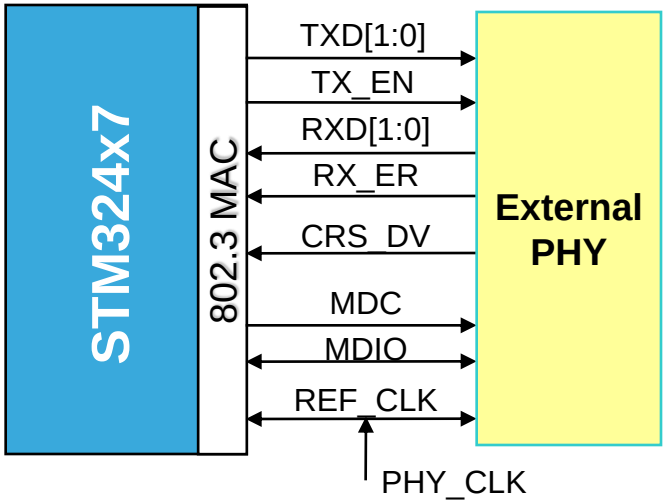
- MII vs. RMII
- Block Diagrams
- Ethernet PHY

Physical Layer Interface

- MII = 18 pins
  - 8 data pins
  - 6 control pins
  - 2 Clock signals
  - 2 for PHY configuration
  - TX_ER(optional, rarely used，STM32 don’t have this pin)

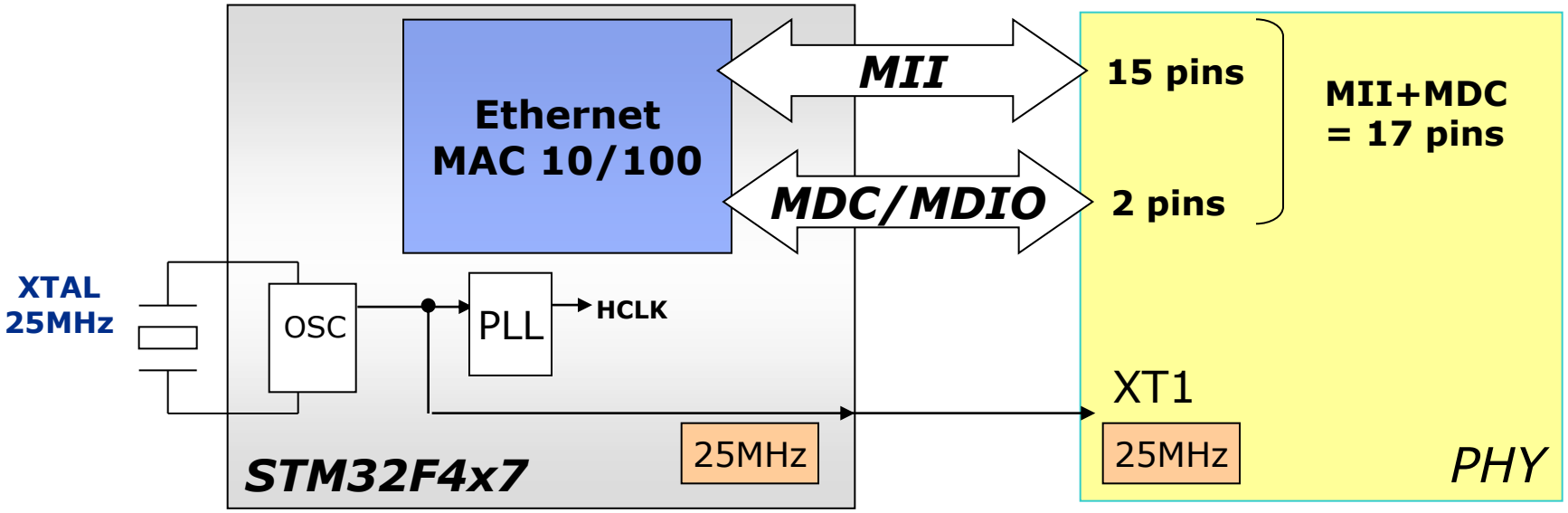


- RMII = 10 pins
  - 4 data
  - 3 control
  - 1 for the clock
  - 2 for PHY configuration
  - RX_ER(optional on switches)



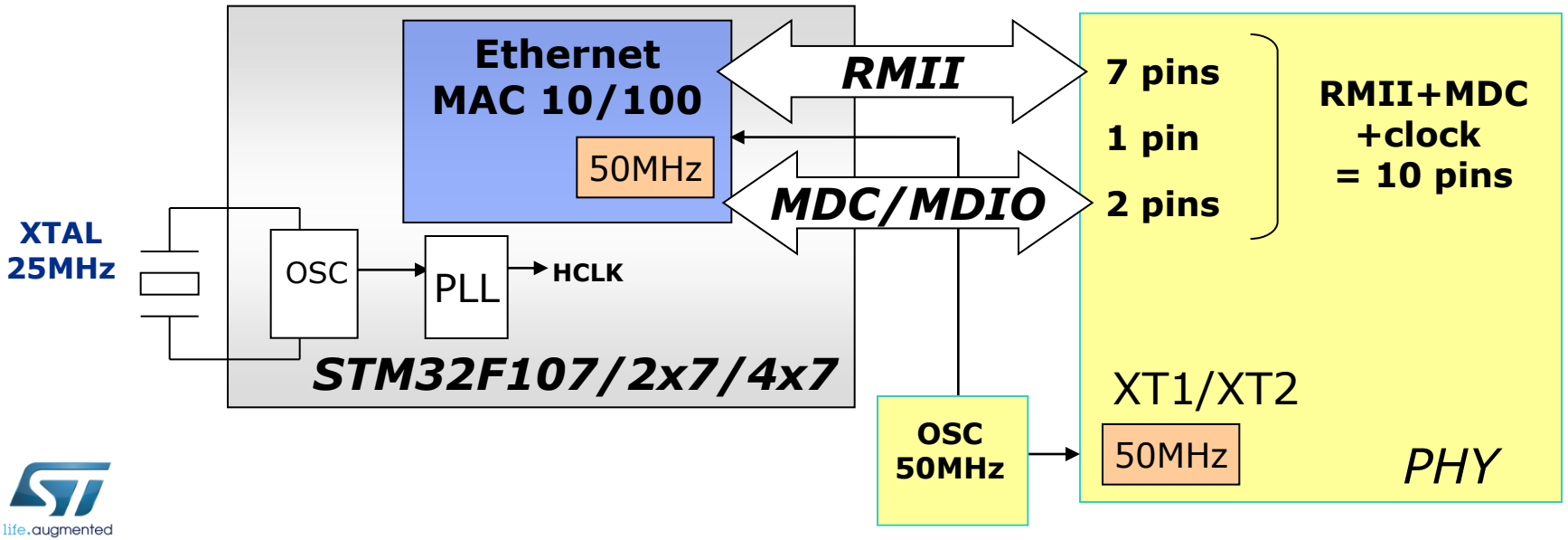
Ethernet Interface Block Diagram (1/4)

- One 25Mhz external crystal (internal oscillator)
  - The internal PLL to generate HCLK (Core, peripherals…)
  - Connected to the MCO to provide the 25Mhz to the PHY



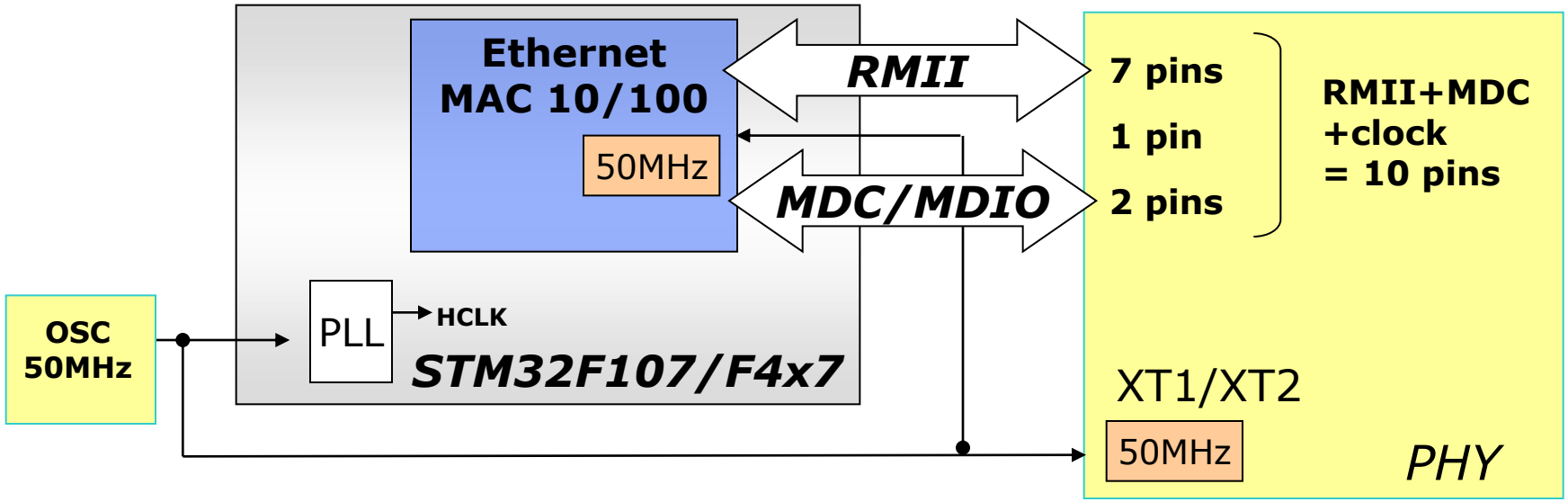
Ethernet Interface Block Diagram (2/4)

- One 50Mhz external oscillator
  - This 50Mhz output clock is provided to the MAC & the PHY
- One 25Mhz external crystal (internal oscillator)
  - The internal PLL to generate HCLK (Core, peripherals…)
- RMII interface
  - 7 pins for the communication between the MAC & PHY
  - 2 pins for the MDC (PHY control)
  - 1 pin for the 50Mhz clock input



Ethernet Interface Block Diagram (3/4)

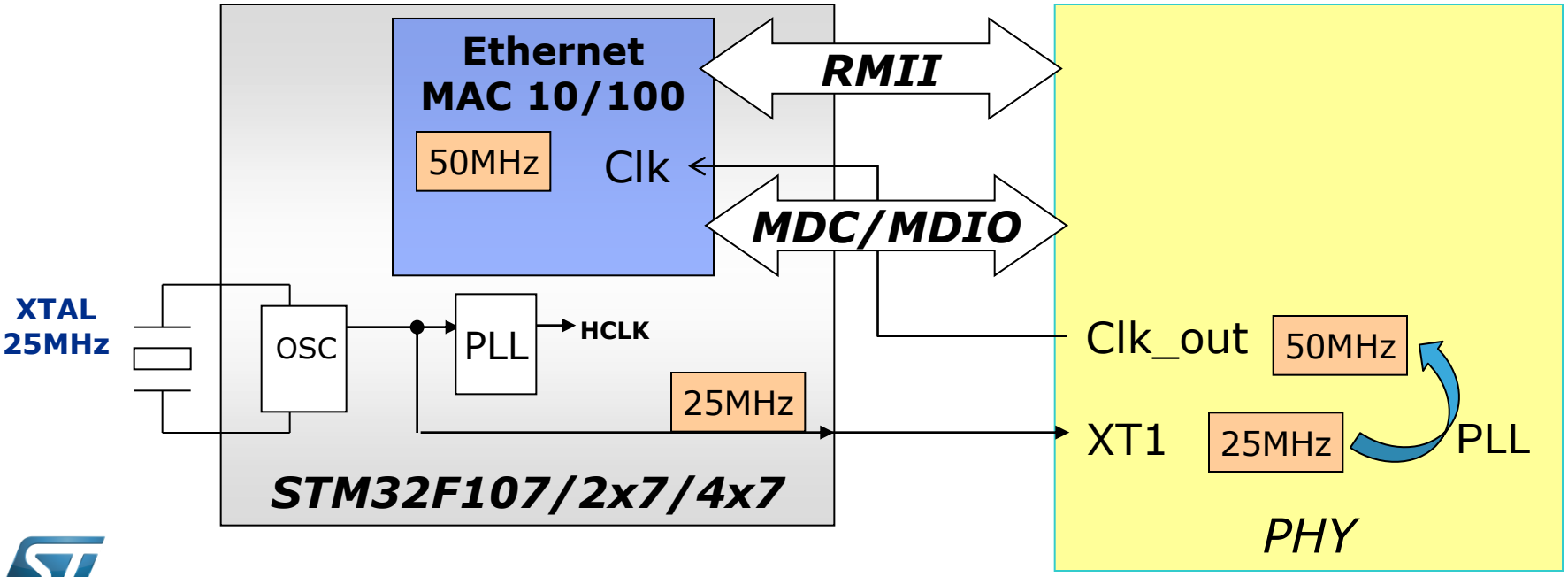
- One 50Mhz external oscillator
  - Connected to the PLL to generate HCLK (Core, peripherals…)
  - This 50Mhz output clock is provided to the MAC & the PHY



Ethernet Interface Block Diagram (4/4)

- One 25Mhz external crystal (internal oscillator)
  - The internal PLL to generate HCLK (Core, peripherals…)
  - Connected to the MCO to provide the 25Mhz to the PHY
  - The PHY then generate the 50MHz clock reference clock

- RMII interface
  - 7 pins for the communication between the MAC & PHY
  - 2 pins for the MDC (PHY control)
  - 1 pin for the 50Mhz clock input



PHY Registers

- The PHY Registers are :
  - Initialized by the Bootstrap configuration
  - Can be accessed by the MCU (providing that the PHY Address is correct)
- There are 3 types of Registers :
  - Basic
  - Extended
  - Vendor Specific
- How to change PHY when using ST’s driver

Example LAN 8720

Table 4.2 SMI Register Map

REGISTER INDEX (DECIMAL)	REGISTER NAME	GROUP
0	Basic Control Register	Basic
1	Basic Status Register	Basic
2	PHY Identifier 1	Extended
3	PHY Identifier 2	Extended
4	Auto-Negotiation Advertisement Register	Extended
5	Auto-Negotiation Link Partner Ability Register	Extended
6	Auto-Negotiation Expansion Register	Extended
17	Mode Control/Status Register	Vendor-specific
18	Special Modes	Vendor-specific
26	Symbol Error Counter Register	Vendor-specific
27	Control / Status Indication Register	Vendor-specific
29	Interrupt Source Register	Vendor-specific
30	Interrupt Mask Register	Vendor-specific
31	PHY Special Control/Status Register	Vendor-specific

Read the Auto-negotiation's result of DP83848C (1/3)

Table 21. PHY Status Register (PHYSTS), address 0x10 (Continued)

Bit	Bit Name	Default	Description
5	Jabber Detect	0, RO	**Jabber Detect:** This bit only has meaning in 10 Mb/s mode This bit is a duplicate of the Jabber Detect bit in the BMSR register, except that it is not cleared upon a read of the PHYSTS register. 1 = Jabber condition detected. 0 = No Jabber.
4	Auto-Neg Complete	0, RO	**Auto-Negotiation Complete:** 1 = Auto-Negotiation complete. 0 = Auto-Negotiation not complete.
3	Loopback Status	0, RO	**Loopback:** 1 = Loopback enabled. 0 = Normal operation.
2	Duplex Status	0, RO	**Duplex:** This bit indicates duplex status and is determined from Auto-Negotiation or Forced Modes. 1 = Full duplex mode. 0 = Half duplex mode. Note: This bit is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.
1	Speed Status	0, RO	**Speed10:** This bit indicates the status of the speed and is determined from Auto-Negotiation or Forced Modes. 1 = 10 Mb/s mode. 0 = 100 Mb/s mode. Note: This bit is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.
0	Link Status	0, RO	**Link Status:** This bit is a duplicate of the Link Status bit in the BMSR register, except that it will not be cleared upon a read of the PHYSTS register. 1 = Valid link established (for either 10 or 100 Mb/s operation) 0 = Link not established.

Read the Auto-negotiation's result of LAN8710 (2/3)

4.2.14 PHY Special Control/Status Register

Index (In Decimal): 31 Size: 16 bits

BITS	DESCRIPTION	TYPE	DEFAULT
15:13	**RESERVED**	RO	-
12	**Autodone** Auto-negotiation done indication: 0 = Auto-negotiation is not done or disabled (or not active) 1 = Auto-negotiation is done	RO	0b
11:7	**RESERVED**	R/W	-
6	**Enable 4B5B** 0 = bypass encoder/decoder 1 = enable 4B5B encoding/decoding. MAC Interface must be configured in MII mode.	R/W	1b
5	**RESERVED**	RO	-
4:2	**Speed Indication** HCDSPEED value: 001 = 10BASE-T half-duplex 101 = 10BASE-T full-duplex 010 = 100BASE-TX half-duplex 110 = 100BASE-TX full-duplex	RO	XXX
1:0	**RESERVED**	RO	-

How to change PHY when using ST's driver (3/3)

- So when you change from PHY to another, the user have to update this value depending on the used external PHY.
- In file "stm32f4x7_eth_conf.h"

```
/* The DP83848 PHY status register  */

#define PHY_SR                  ((uint16_t)0x10)     /* PHY status register Offset */

#define PHY_SPEED_STATUS    ((uint16_t)0x0002)  /* PHY Speed mask

#define PHY_DUPLEX_STATUS ((uint16_t)0x0004)  /* PHY Duplex mask */
```

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02 – Ethernet design

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