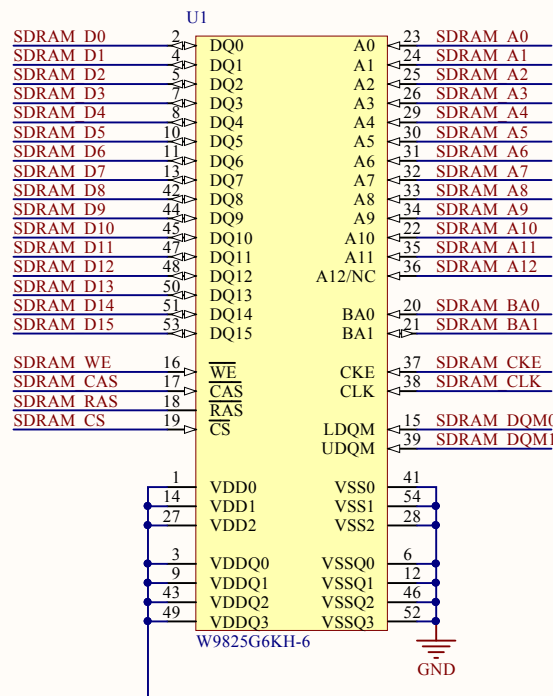
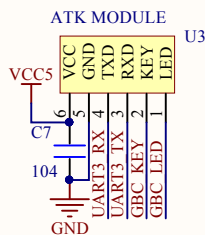


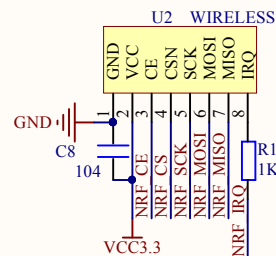
SDRAM



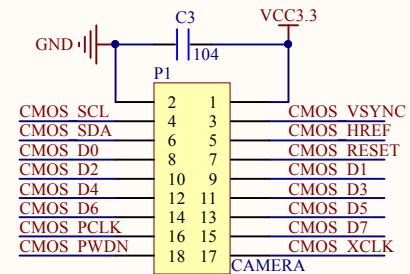
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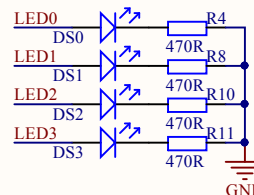
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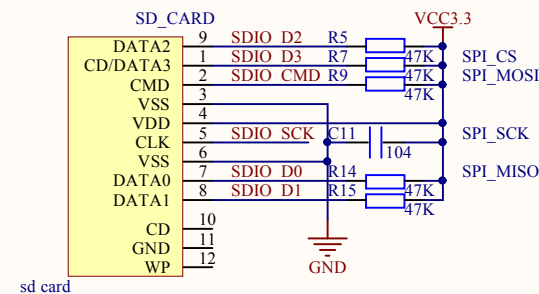
OLED&CAMERA



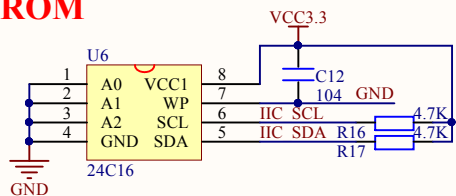
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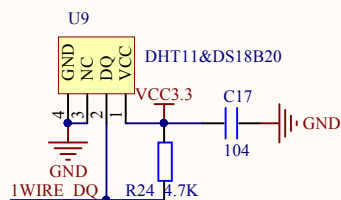
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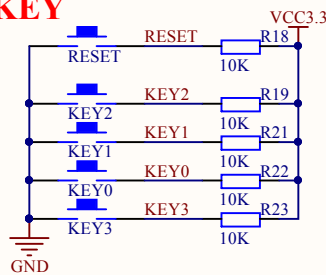
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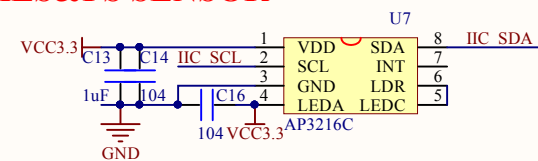
TEMP&HUMI SENSOR



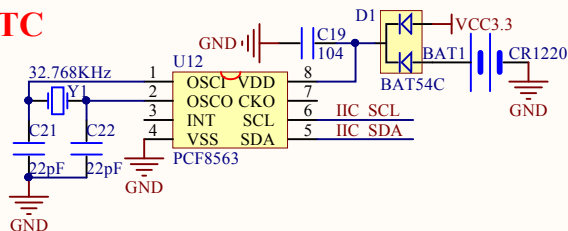
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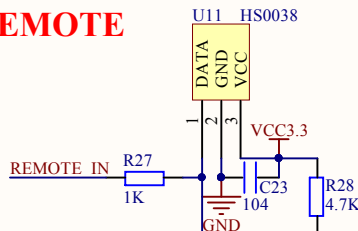
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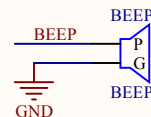
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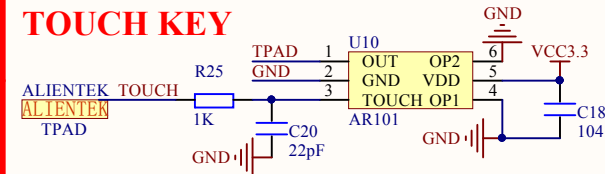
REMOTE



BEEP



TOUCH KEY



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	Version	

FPGA

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BANK 1

IO	D4	B1	D4	UART3_TX
IO	B1	E5		
IO	B1	F3		
IO	B1	B1	SDIO D2	
IO	B1	C2	SDIO D3	
IO	B1	C1	EPSC ASDO	
IO	B1	F3	NRF MISO	
IO	B1	D2	EPSC CS	
IO, DIFFIO_L2p, (FLASH_nCE,nCS0)	D2	B1	SDIO CMD	
IO, DIFFIO_L2n	D1	B1	SDIO CMD	
IO	D5	B1	G5	NRF SCK
IO, DIFFIO_L3p	D1	B1	E2	NRF MOSI
IO, DIFFIO_L3n	D2	B1	G2	NRF CS
IO, DIFFIO_L4p, (DQS0L/CQ1L,DPCLK0)/(DQS0L/CQ1L,DPCLK0)	D1	B1	G1	NRF IRO
IO, DIFFIO_L4n	D2	B1	H2	EPSC DATA0
IO, (DATA0)				

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BANK 2

IO, DIFFIO_L5p, (DQ1L)/(DQ1L)	D2	B2	J2	SDIO SCK
IO, DIFFIO_L5n, (DQ1L)/(DQ1L)	D1	B2	J1	NRF CE
IO	D6	B2	J6	
IO, DIFFIO_L6p	D6	B2	K6	
IO, DIFFIO_L6n	D6	B2	L6	
IO, DIFFIO_L7p	D2	B2	K2	SDIO D1
IO, DIFFIO_L7n, (DQ51L/CQ1L#,(DPCLK1)/(DQ51L/CQ1L#,(DPCLK1)	D1	B2	K1	SDIO D0
IO, DIFFIO_L8n, (DQ51L/CQ1L#,(DPCLK1)/(DQ51L/CQ1L#,(DPCLK1)	D1	B2	L1	LCD RST
IO, VREFB2N0	D3	B2	L3	
IO, DIFFIO_L9p, (DQ1L)/(DQ1L)	D2	B2	N2	T MISO
IO, DIFFIO_L9n, (DQ1L)/(DQ1L)	D1	B2	N1	T SCK
IO, DIFFIO_L8p, (DQ1L)/(DQ1L)	D5	B2	K5	
IO, DIFFIO_L8n, (DQ1L)/(DQ1L)	D4	B2	L4	
IO, (DQS3L/CQ3L#)/(DQS3L/CQ3L#)	D1	B2	R1	LCD BL
IO, DIFFIO_L10p, (DQ1L)/(DQ1L)	D2	B2	P2	T CS
IO, DIFFIO_L10n, (DM1L/BWS#1L)/(DM1L/BWS#1L)	D1	B2	P1	T MOSI

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BANK 3

IO, DIFFIO_B1p, (DM3B/BWS#3B)/(DM3B/BWS#3B)	N3	B3	N3	CAN TX
IO, DIFFIO_B2p, (DQ3B)/(DQ3B)	D3	B3	P3	LCD VSYNC
IO, DIFFIO_B2n, (DQ3B)/(DQ3B)	D3	B3	R3	LCD CLK
IO, (DQS1B/CQ1B#,(DPCLK2)/(DQS1B/CQ1B#,(DPCLK2)	D2	B3	T3	LCD HSYNC
IO, PLL1_CLKOUTp	D2	B3	T2	LCD DE
IO, PLL1_CLKOUTn	D4	B3	R4	LCD B3
IO, DIFFIO_B4p, (DQ3B)/(DQ3B)	D4	B3	T4	LCD B4
IO, DIFFIO_B4n, (DQ3B)/(DQ3B)	D5	B3	N5	CH340 TXD
IO, (DQ3B)/(DQ3B)	D6	B3	N6	CMOS D5
IO, VREFB3N0	D6	B3	M6	CAN RX
IO, DIFFIO_B5p, (DQS3B/CQ3B#)/(DQS3B/CQ3B#)	D6	B3	P6	CMOS D4
IO, DIFFIO_B5n, (DQS3B/CQ3B#)/(DQS3B/CQ3B#)	D7	B3	M7	CH340 RXD
IO, DIFFIO_B6p, (DQ3B)/(DQ3B)	D8	B3	K8	
IO, DIFFIO_B6n, (DQ3B)/(DQ3B)	D5	B3	R5	LCD B1
IO, DIFFIO_B7p, (DQ3B)/(DQ3B)	D5	B3	T5	LCD B2
IO, DIFFIO_B7n, (DQ3B)/(DQ3B)	D6	B3	R6	LCD G5
IO, DIFFIO_B8n, (DQ5B/CQ5B#)/(DQ5B/CQ5B#)	D6	B3	T6	LCD B0
IO, DIFFIO_B8p, (DQ5B/CQ5B#)/(DQ5B/CQ5B#)	D7	B3	L7	LCD G3
IO, DIFFIO_B9n, (DQ5B/CQ5B#)/(DQ5B/CQ5B#)	D7	B3	R7	LCD G4
IO, DIFFIO_B9p, (DQ5B/CQ5B#)/(DQ5B/CQ5B#)	D8	B3	L8	LCD D0
IO, DIFFIO_B10n, (DQ5B)/(DQ5B)	D8	B3	M8	CMOS D3
IO, DIFFIO_B10p, (DQ5B)/(DQ5B)	D8	B3	N8	CMOS D2
IO, DIFFIO_B11n, (DQ5B)/(DQ5B)	D8	B3	P8	CMOS D1
IO, DIFFIO_B11p, (DQ5B)/(DQ5B)	D8	B3	R8	LCD G1
IO, DIFFIO_B12n, (DQ5B)/(DQ5B)	D8	B3	T8	LCD G2
IO, DIFFIO_B12p, (DQ5B)/(DQ5B)	D8	B3	T8	LCD G2

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BANK 4

IO, DIFFIO_B12p, (DQ5B)/(DQ5B)	D9	B4	R9	LCD R4
IO, DIFFIO_B12n, (DQ5B)/(DQ5B)	D9	B4	T9	LCD G6
IO, DIFFIO_B13p, (DQ5B)/(DQ5B)	D9	B4	K9	CMOS D0
IO, DIFFIO_B13n, (DQ5B)/(DQ5B)	D9	B4	L9	CMOS RESET
IO, DIFFIO_B14p, (DQ5B)/(DQ5B)	D9	B4	M9	CMOS HREF
IO, DIFFIO_B14n, (DQ5B)/(DQ5B)	D9	B4	N9	CMOS SCL
IO, DIFFIO_B15p, (DQ5B)/(DQ5B)	D10	B4	R10	LCD R2
IO, DIFFIO_B15n, (DQ5B)/(DQ5B)	D10	B4	T10	LCD R3
IO, DIFFIO_B16p, (DQ5B)/(DQ5B)	D11	B4	R11	LCD R0
IO, DIFFIO_B16n, (DQ5B)/(DQ5B)	D11	B4	T11	LCD R1
IO, DIFFIO_B17p, (DQ5B)/(DQ5B)	D12	B4	R12	CMOS PWDN
IO, DIFFIO_B17n, (DQ5B)/(DQ5B)	D12	B4	T12	CMOS PWDN
IO, DIFFIO_B18p, (DQ5B)/(DQ5B)	D10	B4	K10	SDRAM CS
IO, DIFFIO_B18n, (DQ5B)/(DQ5B)	D10	B4	L10	CMOS SDA
IO, (DQS2B/CQ2B#)/(DQS2B/CQ2B#)	D9	B4	P10	CMOS VSYNC
IO, VREFB4N0	D11	B4	P11	LEDSEG G
IO, DIFFIO_B19p, (DQ5B)/(DQ5B)	D13	B4	R13	CMOS PCLK
IO, DIFFIO_B19n, (DQ5B)/(DQ5B)	D13	B4	T13	CMOS XCLK
IO, DIFFIO_B20p, (DQ5B)/(DQ5B)	D10	B4	M10	LEDSEG E
IO, DIFFIO_B20n, (DQ5B)/(DQ5B)	D11	B4	N11	LEDSEG F
IO, DIFFIO_B21p, (DQ5B)/(DQ5B)	D14	B4	T14	CMOS D7
IO, DIFFIO_B21n, (DQ5B)/(DQ5B)	D15	B4	T15	LEDSEG CH1
IO, DIFFIO_B22p, (DQ5B)/(DQ5B)	D14	B4	R14	CMOS D6
IO, DIFFIO_B22n, (DQ5B)/(DQ5B)	D14	B4	P14	SDRAM D0
IO, DIFFIO_B23p, (DQ5B)/(DQ5B)	D11	B4	L11	SDRAM D6
IO, DIFFIO_B23n, (DQ5B)/(DQ5B)	D11	B4	M11	LEDSEG A
IO, DIFFIO_B24p, (DQ5B)/(DQ5B)	D12	B4	N12	LEDSEG B

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BANK 5

IO, RUP3, (DM1R/BWS#1R)/(DM1R/BWS#1R)	N13	B5	N13	LEDSEG D
IO, RDN3, (DQ1R)/(DQ1R)	M12	B5	M12	SDRAM D1
IO, DIFFIO_R11n, (DQS3R/CQ3R#)/(DQS3R/CQ3R#)	D12	B5	L12	SDRAM D3
IO, DIFFIO_R11p, (DQ1R)/(DQ1R)	D12	B5	K12	SDRAM D7
IO, DIFFIO_R10n, (DQ1R)/(DQ1R)	N14	B5	N14	SDRAM D2
IO, DIFFIO_R10p, (DQ1R)/(DQ1R)	D15	B5	P15	LEDSEG CH3
IO, VREFB5N0	D16	B5	P16	LEDSEG CH4
IO, DIFFIO_R9n, (DQ1R)/(DQ1R)	R16	B5	R16	LEDSEG CH2
IO, DIFFIO_R9p, (DQ1R)/(DQ1R)	D11	B5	K11	SDRAM RAS
IO, DIFFIO_R8n, (DQ1R)/(DQ1R)	N16	B5	N16	LEDSEG CH6
IO, DIFFIO_R8p, (DQ1R)/(DQ1R)	D15	B5	N15	LEDSEG CH5
IO, DIFFIO_R7n, (DEV_OE)/(DEV_OE)	D14	B5	L14	SDRAM D5
IO, DIFFIO_R7p, (DEV_OE)/(DEV_OE)	D13	B5	L13	SDRAM D4
IO, DIFFIO_R6n, (DQ1R)/(DQ1R)	D16	B5	L16	SDRAM D14
IO, DIFFIO_R6p, (DQ1R)/(DQ1R)	D15	B5	L15	SDRAM D15
IO, DIFFIO_R5n, (DQ1R)/(DQ1R)	D11	B5	J11	SDRAM D9
IO, DIFFIO_R5p, (DQ1R)/(DQ1R)	D16	B5	K16	SDRAM D12
IO, DIFFIO_R4n, (INIT_DONE)/(INIT_DONE)	D15	B5	K15	SDRAM D13
IO, DIFFIO_R4p, (CRC_ERROR)/(CRC_ERROR)	D16	B5	J16	SDRAM D10
IO, DIFFIO_R3n, (nCEO)/(nCEO)	D15	B5	J15	SDRAM D11
IO, DIFFIO_R3p, (CLKUSR)/(CLKUSR)	D14	B5	J14	SDRAM D0M0
IO, (DQS0R/CQ1R,DPCLK5)/(DQS0R/CQ1R,DPCLK5)	D12	B5	J12	SDRAM CAS
IO, DIFFIO_R1n, (DQS2R/CQ3R)/(DQS2R/CQ3R)	D13	B5	J13	SDRAM WE

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BANK 6

IO, DIFFIO_R4n, (INIT_DONE)/(INIT_DONE)	G16	B6	G16	SDRAM D8
IO, DIFFIO_R4p, (CRC_ERROR)/(CRC_ERROR)	G15	B6	G15	SDRAM D0M1
IO, DIFFIO_R3n, (nCEO)/(nCEO)	D13	B6	F13	SDRAM BA1
IO, DIFFIO_R3p, (CLKUSR)/(CLKUSR)	D16	B6	F16	SDRAM CKE
IO, (DQS0R/CQ1R,DPCLK5)/(DQS0R/CQ1R,DPCLK5)	D15	B6	F15	SDRAM A12
IO, DIFFIO_R2n, (DQ1R)/(DQ1R)	D16	B6	D16	SDRAM A6
IO, DIFFIO_R2p, (DQ1R)/(DQ1R)	D14	B6	F14	SDRAM A10
IO, DIFFIO_R1n, (DQS2R/CQ3R)/(DQS2R/CQ3R)	D16	B6	D16	SDRAM A11
IO, DIFFIO_R1p, (DQS2R/CQ3R)/(DQS2R/CQ3R)	D15	B6	D15	SDRAM A9
IO, DIFFIO_R0n, (DQ1R)/(DQ1R)	D11	B6	G11	SDRAM BA0
IO, DIFFIO_R0p, (DQ1R)/(DQ1R)	D16	B6	C16	SDRAM A8
IO, DIFFIO_R0n, (DQ1R)/(DQ1R)	D15	B6	C15	SDRAM A7

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BANK 7

IO, DIFFIO_T21n, (DQ5T)/(DQ5T)	C14	B7	C14	SDRAM A3
IO, DIFFIO_T21p, (DQ5T)/(DQ5T)	D14	B7	D14	SDRAM A2
IO, DIFFIO_T20n, (DQ5T)/(DQ5T)	D11	B7	D11	LED0
IO, DIFFIO_T20p, (DQ5T)/(DQ5T)	D12	B7	D12	BEEP
IO, DIFFIO_T19n, (DQ5T)/(DQ5T)	D13	B7	A13	GBC KEY
IO, DIFFIO_T19p, (DQ5T)/(DQ5T)	D13	B7	B13	GBC LED
IO, DIFFIO_T18n, (DQ5T)/(DQ5T)	D14	B7	A14	SDRAM A4
IO, DIFFIO_T18p, (DQ5T)/(DQ5T)	D14	B7	B14	SDRAM CLK
IO, DIFFIO_T17n, (DQ5T)/(DQ5T)	D11	B7	E11	SDRAM A1
IO, DIFFIO_T17p, (DQ5T)/(DQ5T)	D10	B7	E10	LED2
IO, DIFFIO_T16n, (DQ5T)/(DQ5T)	D12	B7	A12	UART2_RX
IO, DIFFIO_T16p, (DQ5T)/(DQ5T)	D12	B7	B12	UART2_TX
IO, DIFFIO_T15n, (DQ5T)/(DQ5T)	D11	B7	A11	RS485 DE
IO, DIFFIO_T15p, (DQ5T)/(DQ5T)	D11	B7	B11	VGA HSYNC
IO, DIFFIO_T14n, (DQ5T)/(DQ5T)	D11	B7	C11	LED1
IO, DIFFIO_T14p, (DQ5T)/(DQ5T)	D10	B7	F10	TWIRE DQ
IO, DIFFIO_T13n, (DQ5T)/(DQ5T)	D9	B7	F9	LED3
IO, DIFFIO_T13p, (DQ5T)/(DQ5T)	D11	B7	F11	SDRAM A0
IO, DIFFIO_T12n, (DQ5T)/(DQ5T)	D15	B7	A15	SDRAM A5
IO, DIFFIO_T12p, (DQ5T)/(DQ5T)	D10	B7	A10	VGA D11
IO, DIFFIO_T11n, (DQ5T)/(DQ5T)	D10	B7	B10	VGA VSYNC
IO, DIFFIO_T11p, (DQ5T)/(DQ5T)	D9	B7	C9	LEDSEG C
IO, DIFFIO_T10n, (DQ5T)/(DQ5T)	D9	B7	D9	LEDSEG DOT
IO, DIFFIO_T10p, (DQ5T)/(DQ5T)	D9	B7	E9	
IO, DIFFIO_T9n, (DQ5T)/(DQ5T)	D9	B7	A9	VGA D13
IO, DIFFIO_T9p, (DQ5T)/(DQ5T)	D9	B7	B9	VGA D12

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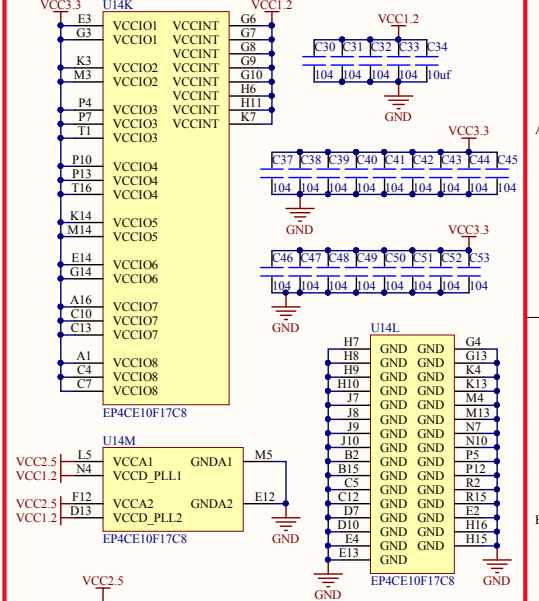
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BANK 8

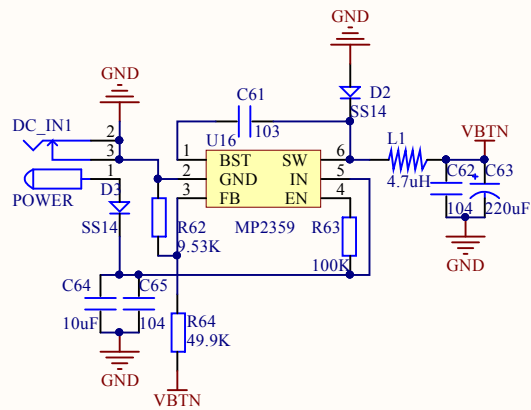
IO, DIFFIO_T11n, (DQ5T)/(DQ5T)	A8	B8	A8	VGA D15
IO, DIFFIO_T11p, (DQ5T)/(DQ5T)	D8	B8	B8	VGA D14
IO, (DQS5T/CQ5T#)/(DQS5T/CQ5T#)	D8	B8	C8	IIC SDA
IO, (DQ5T)/(DQ5T)	D8	B8	D8	IIC SCL
IO, DIFFIO_T10n, (DQ5T)/(DQ5T)	D8	B8	E8	
IO, DIFFIO_T10p, (DQ5T)/(DQ5T)	D8	B8	F8	TPAD
IO, DIFFIO_T9n, (DQ5T)/(DQ5T)	A7	B8	A7	VGA D6
IO, DIFFIO_T9p, (DQ5T)/(DQ5T)	D7	B8	B7	VGA D5
IO, DIFFIO_T8n, (DQ5T)/(DQ5T)	D6	B8	F6	
IO, DIFFIO_T8p, (DQ5T)/(DQ5T)	D7	B8	E7	
IO, DIFFIO_T7n, (DQ5T)/(DQ5T)	D6	B8	C6	I2S DACDAT
IO, DIFFIO_T7p, (DQ5T)/(DQ5T)	D6	B8	A6	VGA D8
IO, (DATA5)/(DATA5)	D6	B8	B6	VGA D7
IO, (DATA6)/(DATA6)	D6	B8	E6	I2S LRCLK
IO, DIFFIO_T6n, (DQ5T)/(DQ5T)	A5	B8	A5	VGA D10
IO, DIFFIO_T6p, (DQ5T)/(DQ5T)	A2	B8	A2	VGA D4
IO, DIFFIO_T5n, (DQ5T)/(DQ5T)	D5	B8	B5	VGA D9
IO, DIFFIO_T5p, (DQ5T)/(DQ5T)	D4	B8	A4	VGA D1
IO, DIFFIO_T4n, (DM3T/BWS#3T)/(DM3T/BWS#3T)	D4	B8	P4	VGA D0
IO, DIFFIO_T4p, (DM3T/BWS#3T)/(DM3T/BWS#3T)	D5	B8	D5	I2S DACDAT
IO, DIFFIO_T3n, (DQ5T)/(DQ5T)	D6	B8	D6	I2S ADCDAT
IO, DIFFIO_T3p, (DQ5T)/(DQ5T)	A3	B8	A3	VGA D3
IO, DIFFIO_T2n, (DQ5T)/(DQ5T)	D3	B8	B3	VGA D2
IO, DIFFIO_T2p, (DQ5T)/(DQ5T)	D3	B8	C3	UART3_RX
IO, DIFFIO_T1n, (DQ5T)/(DQ5T)	D3	B8	D3	

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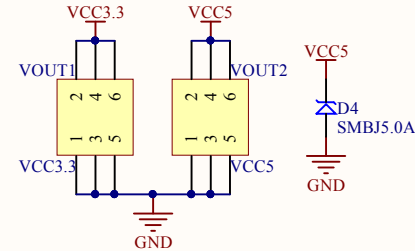
POWER&JTAG



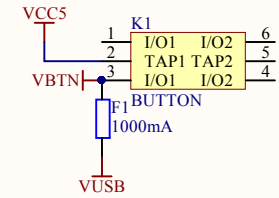
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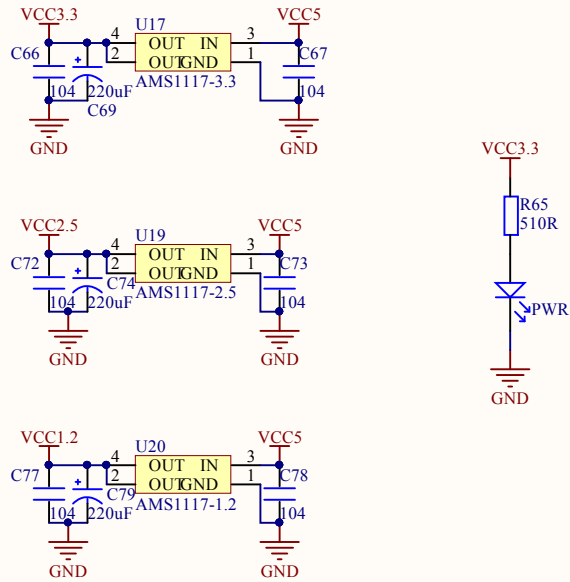
ON BOARD POWER SOURCE



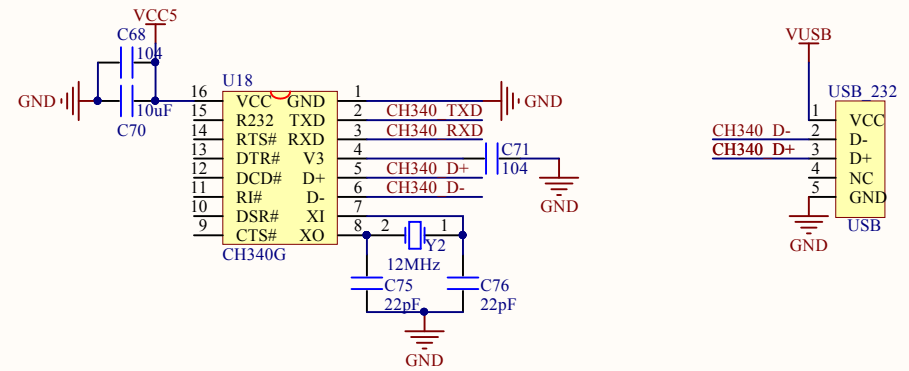
POWER SWITCH



3.3V/2.5V/1.2V/ POWER



USB USART&USB POWER



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