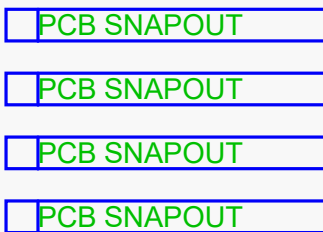
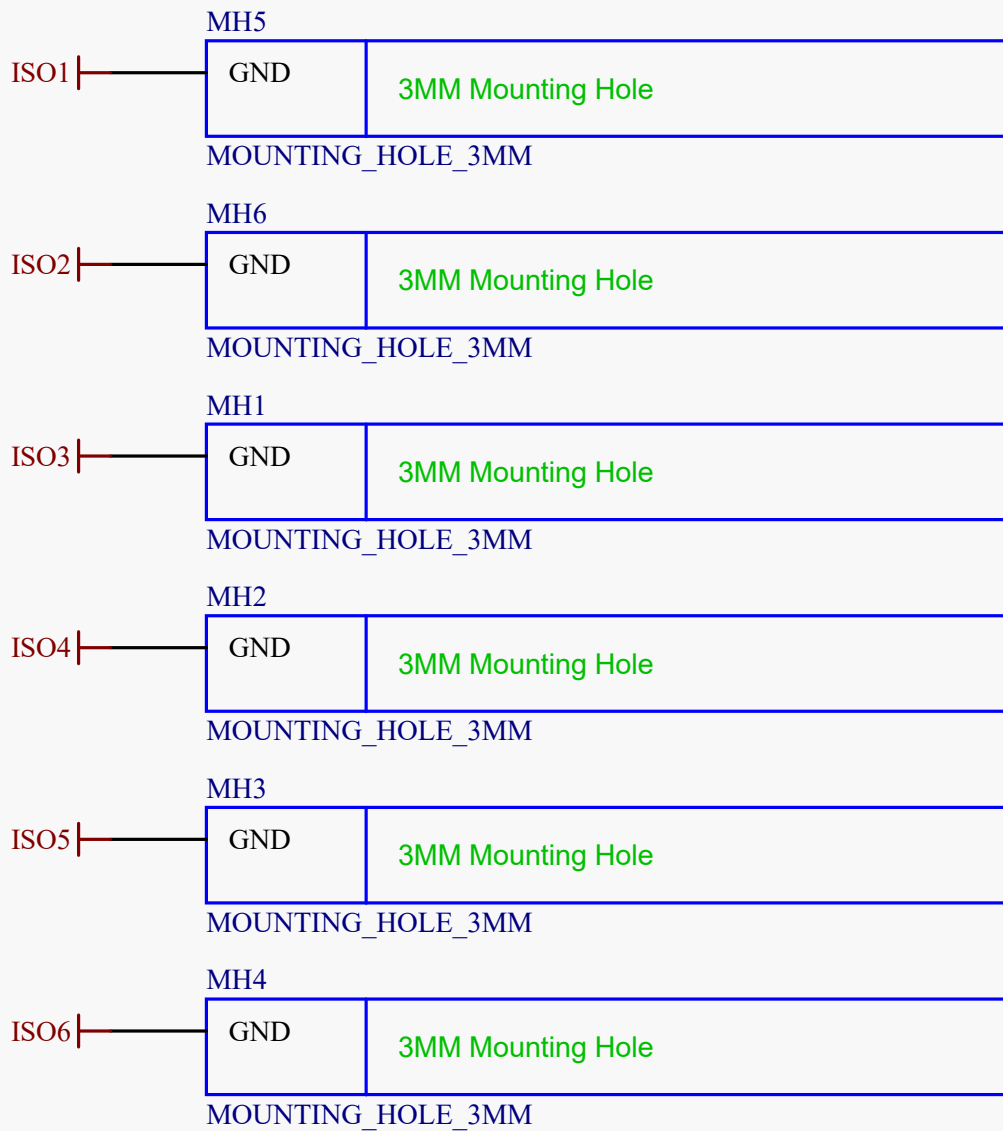
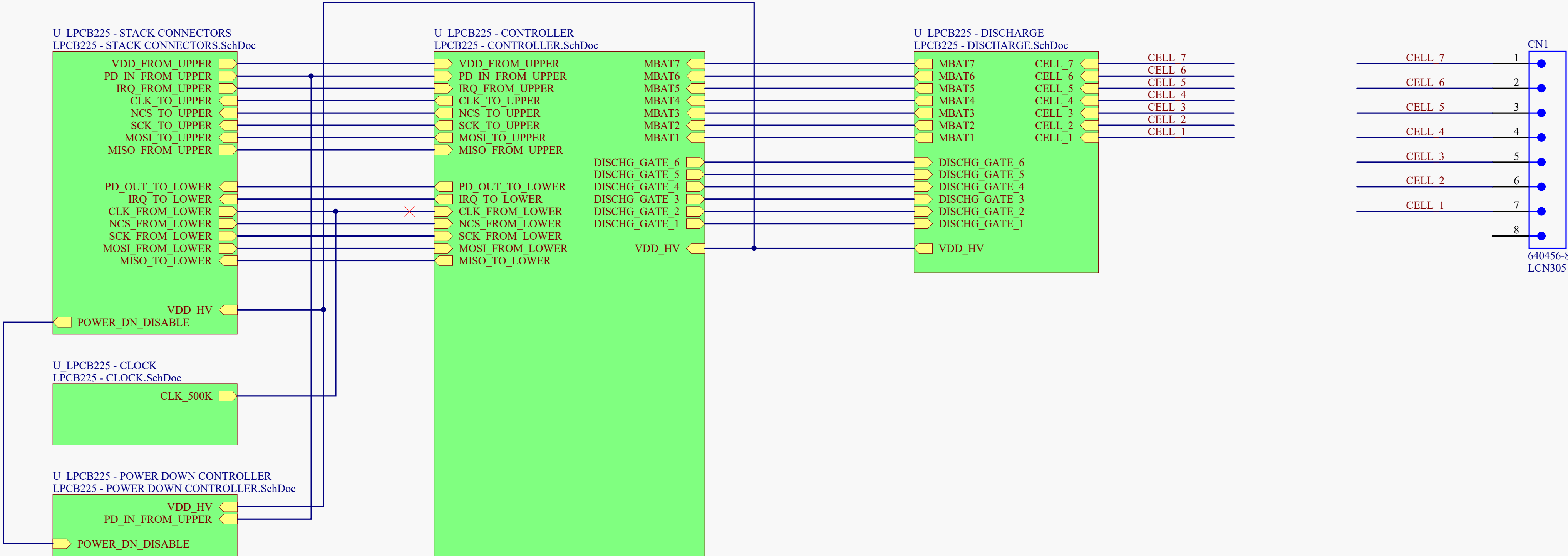



A

B

C

D



| | | | |
|--|---------------------------|-------------------|------------|
|  http://rloop.org | PCB COMPONENT DESCRIPTION | | LDL NUMBER |
| | BMS Module | | LPCB225 |
| | Assembly Details | | |
| | Module Overview | | |
| | Size | Drawing File Name | Revision |
| A3 | LPCB225 - OVERVIEW.SchDoc | 1 | |
| Scale | | Sheet Details | |
| N.T.S | | Sheet: 1 Of: 6 | |

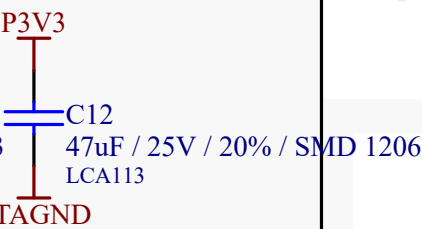
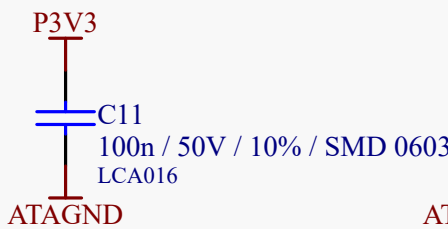
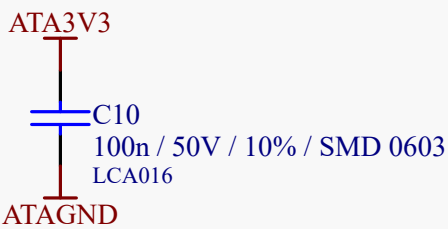
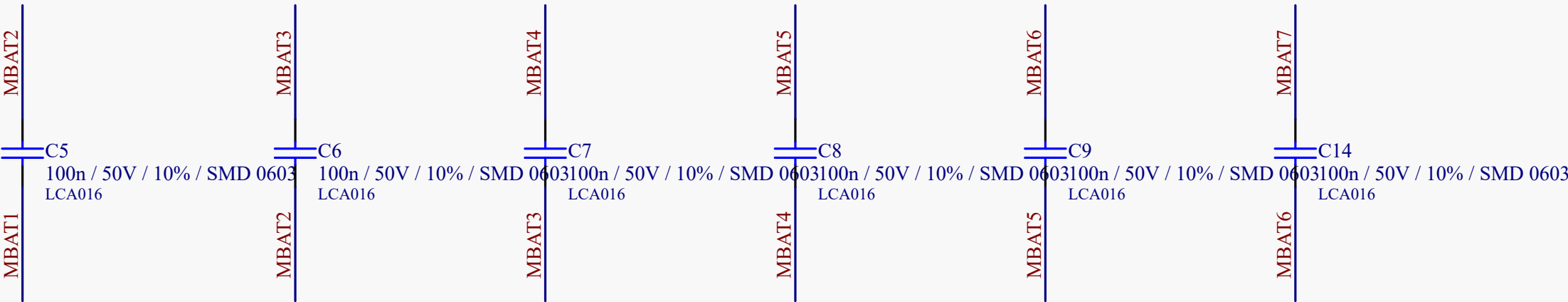
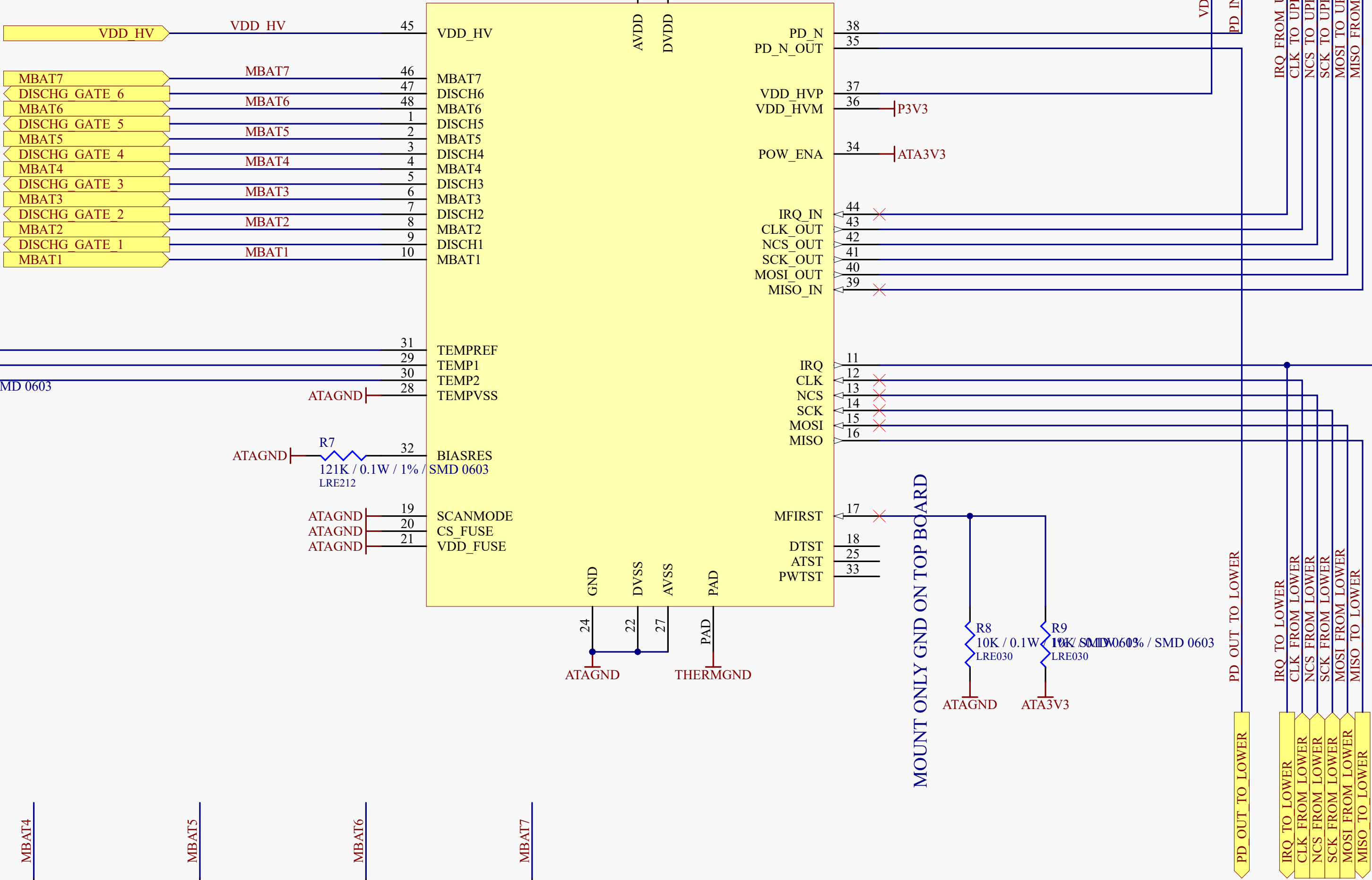
VDD HV R3 VDD FROM UPPER
0R / 0.1W / SMD 0603
LRE026

Internal Reg powered from VDD_VH on TOP BOARD ONLY!


INT VOLT REG

ATA3V3
26
23

IC3
ATA6870N-PLQW-1
LIC563



BYPASS CAPS

| | | | | |
|--|-----------------------------|-------------------|------------|----------------|
|  http://rloop.org | PCB COMPONENT DESCRIPTION | | LDL NUMBER | |
| | BMS Module | | LPCB225 | |
| | Assembly Details | | | |
| | Module Main Controller | | | |
| | Size | Drawing File Name | | Revision |
| A3 | LPCB225 - CONTROLLER.SchDoc | | 1 | |
| Scale | | | | Sheet Details |
| N.T.S | | | | Sheet: 3 Of: 6 |

6.9 to 30V MAX

CELL 7

CELL 6

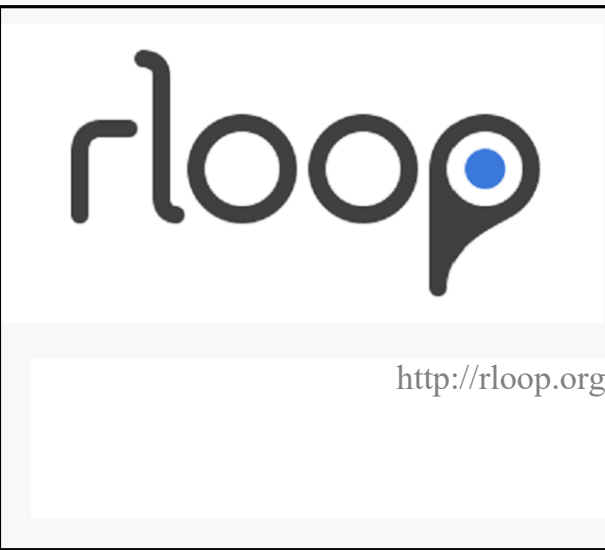
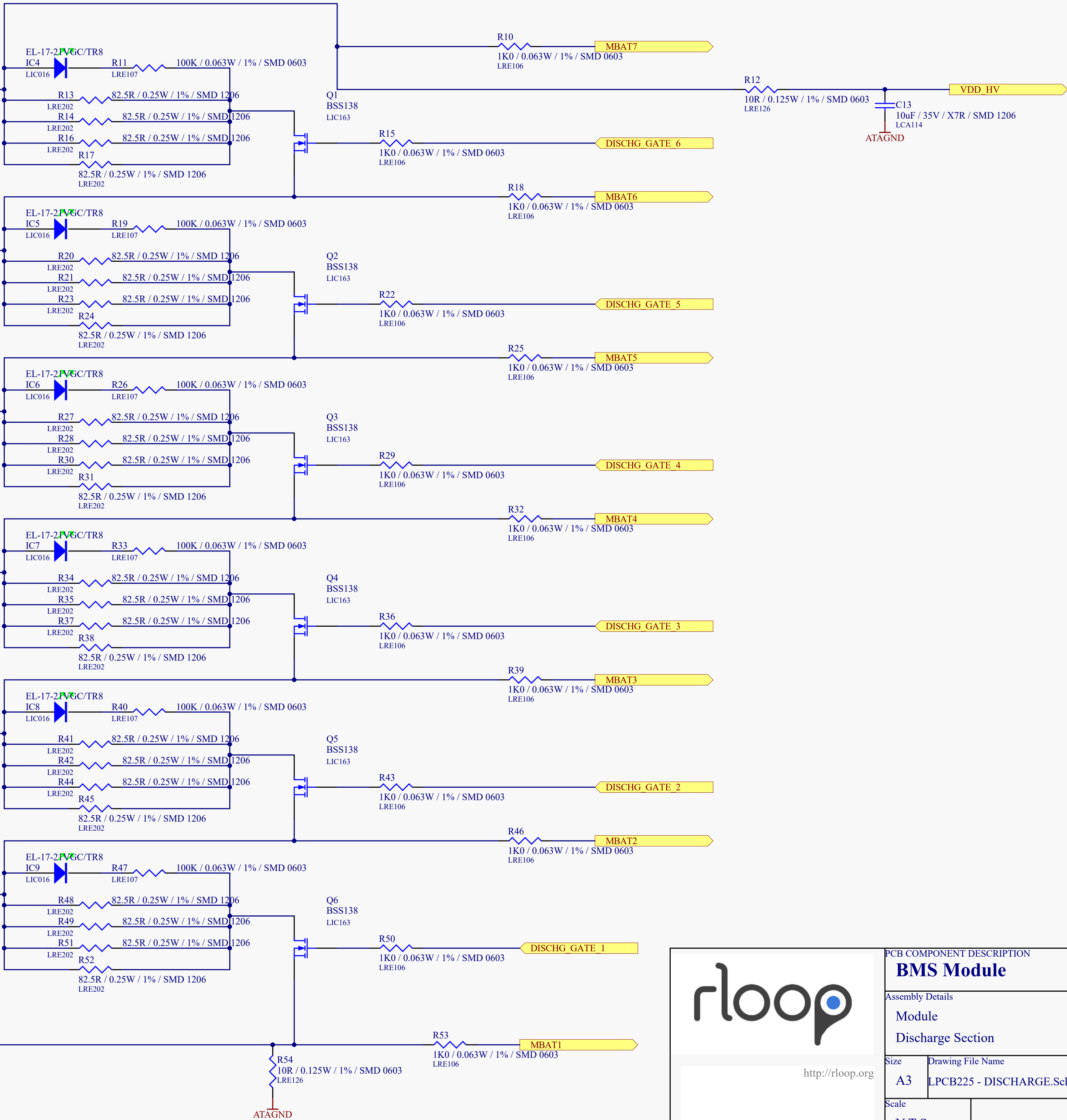
CELL 5

CELL 4

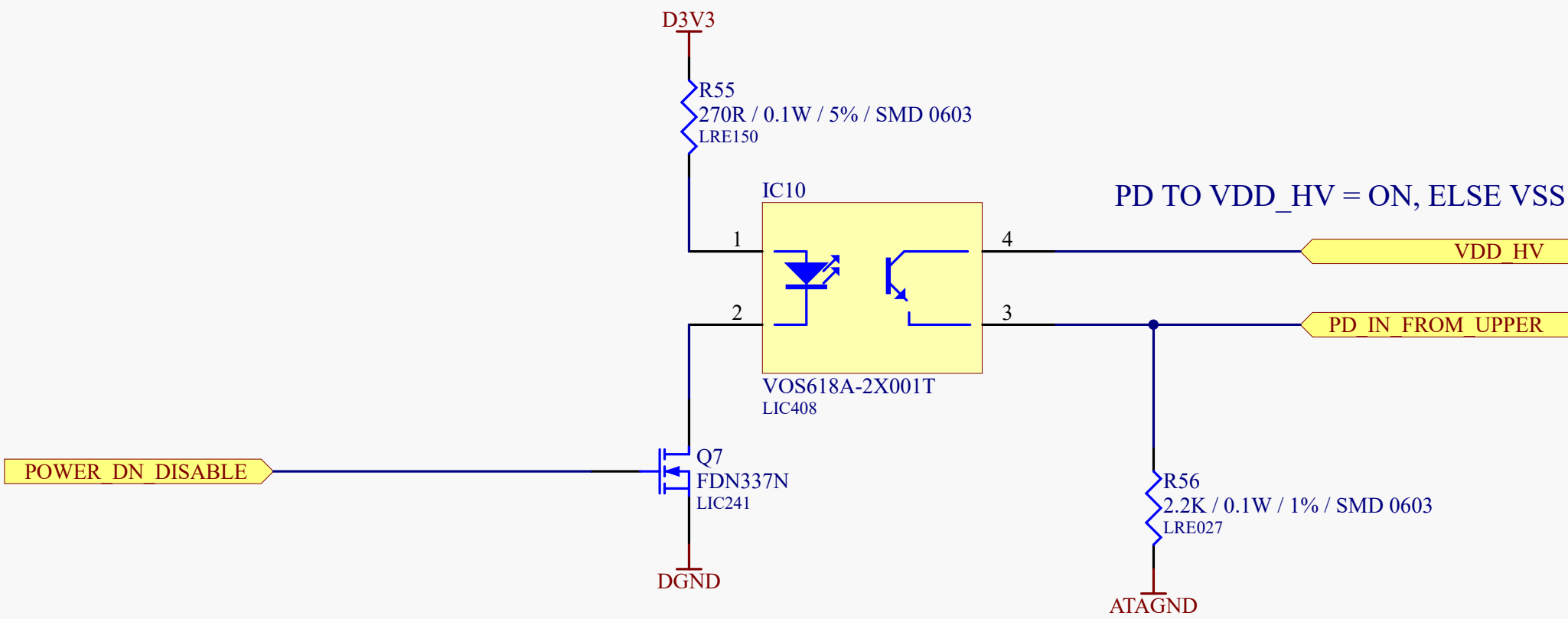
CELL 3

CELL 2


CELL 1



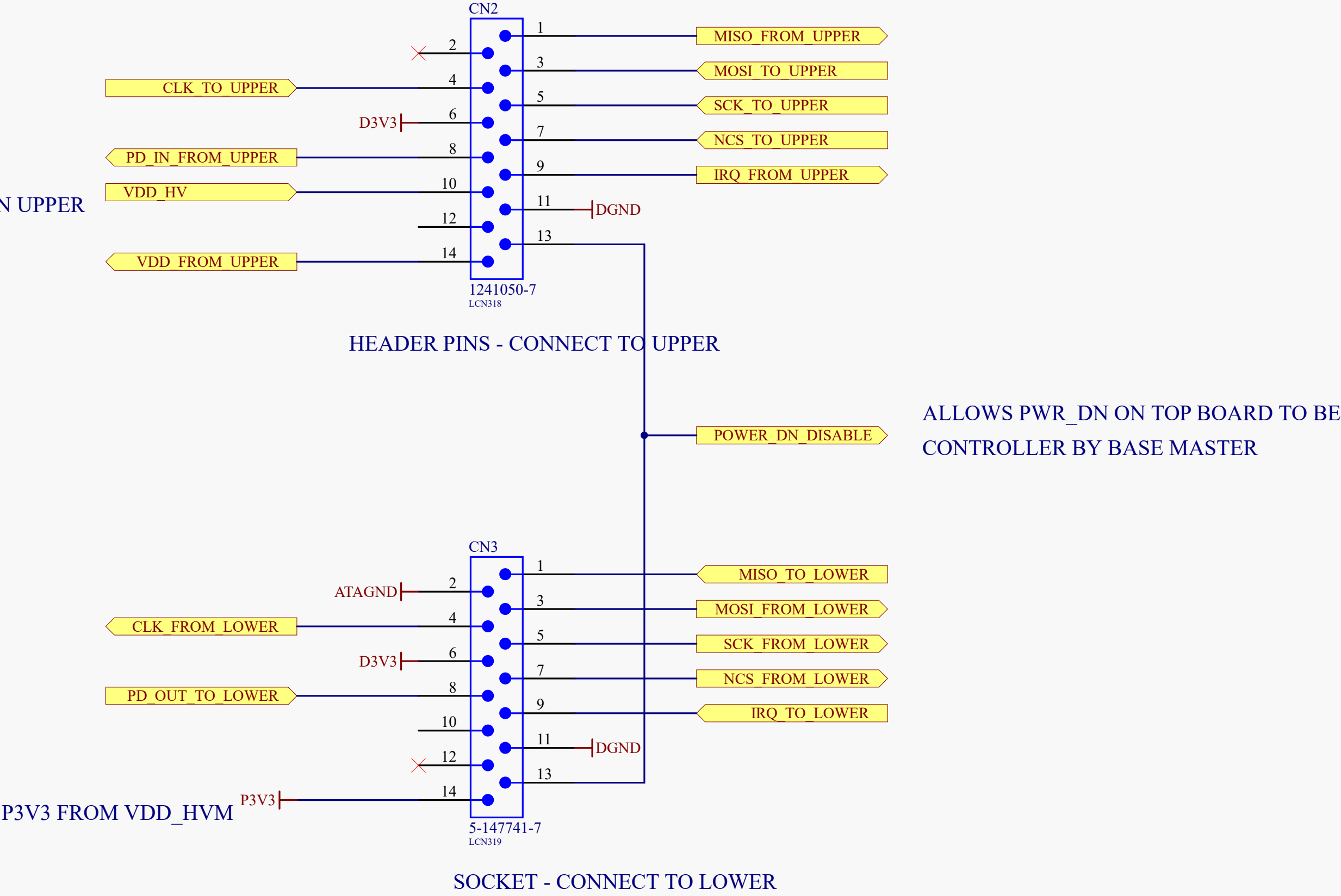
| PCB COMPONENT DESCRIPTION | | LDL NUMBER |
|---------------------------|----------------------------|------------|
| BMS Module | | LPCB225 |
| Assembly Details | | |
| Module | | |
| Discharge Section | | |
| Size | Drawing File Name | Revision |
| A3 | LPCB225 - DISCHARGE.SchDoc | 1 |
| Scale | Sheet Details | |
| N.T.S | Sheet: 4 Of: 6 | |




Power-down Mode
In power-down mode all blocks of the IC are switched off.
The circuit can be switched from Power-down to ON mode or back via the PD_N input. If the pin is connected to VDDHV via an external optocoupler, for example, the circuit is in ON mode. If several Atmel ATA6870N are stacked, the power-down signal must be only provided for the IC on the top level of the stack. The next lower IC receives this information from the PD_N_OUT output of its upper IC. The PD_N_OUT pin must be connected to either the PD_N pin of the next lower Atmel ATA6870N or to AVSS.

| | | | |
|---|--|----------------|------------|
| <div></div> <div>http://rloop.org</div> | PCB COMPONENT DESCRIPTION | | LDL NUMBER |
| | BMS Module | | LPCB225 |
| | Assembly Details | | |
| | Module | | |
| | Power Down Controller | | |
| Size | Drawing File Name | | Revision |
| A3 | LPCB225 - POWER DOWN CONTROLLER.SchDoc | | 1 |
| Scale | | Sheet Details | |
| N.T.S | | Sheet: 5 Of: 6 | |

VDD_HV FROM LOWER BECOMES ATAGND ON UPPER



| | | | |
|--|-----------------------------------|-------------------|------------|
|  http://rloop.org | PCB COMPONENT DESCRIPTION | | LDL NUMBER |
| | BMS Module | | LPCB225 |
| | Assembly Details | | |
| | Module | | |
| | Stackup Connectors | | |
| | Size | Drawing File Name | Revision |
| A3 | LPCB225 - STACK CONNECTORS.SchDoc | 1 | |
| Scale | | Sheet Details | |
| N.T.S | | Sheet: 6 Of: 6 | |