LOGOCOM LABS

# PCB Preproduction Checklist

| ID | Item | Check |
|---|---|---|
| **0.0** | **Schematic** | |
| 0.1 | Boot strapping note added to MCU sheet? Triple-check default states due to internal vs. external pull-up/pull-down resistors. | |
| 0.2 | Boot strapping pins accessible via TPs? | |
| 0.3 | Debug pins broken out to SMD header? | |
| 0.4 | Test points on all unused pins? | |
| 0.5 | Small ceramic bypass cap on enable/reset lines? | |
| 0.6 | Noise-sensitive analog systems have separate power rail from low-noise LDO? Inside a grounded RF shield? | |
| 0.7 | All peripherals have TVS diodes as gatekeeper? | |
| 0.8 | All (UART, SPI, etc.) signals have 0R series resistors to make placeholder for ferrite bead? | |
| 0.9 | Check default internal state of IO pins (pull-up vs. pull-down) and add external resistors where necessary. Option to add both and DNP where necessary. | |
| **1.0** | **Footprints** | |
| 1.1 | All components have 3D extrusion? | |
| 1.2 | Footprints double-checked? | |
| 1.3 | Footprints triple-checked? | |
| 1.4 | Detailed 3D CAD populated for all ICs, especially connectors? Check manufacturer website if not available through distributor. | |
| 1.4 | Connectors facing outwards? | |
| 1.5 | Pin 1 indicator present on silkscreen of all ICs? Polarity (e.g. diodes, LEDs, electrolytic caps) indicated? | |
| **2.0** | **Power Plane** | |
| 2.1 | Islands for separate rails? | |

| | | |
|---|---|---|
| 2.2 | Island bridges ~20 mil width (check with trace width calculator) | |
| **3.0** | **Ground Plane** | |
| 3.1 | Stitching vias? | |
| 3.2 | Direct connect polygons for GND vias? | |
| 3.3 | No net antennae on DRC? Add vias to planes that extend into stubs without enough stitching vias. | |
| **4.0** | **Vias** | |
| 4.1 | Tented on top and bottom (except for thermal relief GND vias underneath large ICs)? | |
| 4.2 | 10-20mil ratio? | |
| **5.0** | **Miscellaneous** | |
| 5.1 | Mounting holes in each corner, M3 (3mm dia) screws | |
| 5.2 | Board outline defined on Keep-Out or Mechanical 1 layer with curved edges | |
| 5.3 | Board outlines clearance set to 20-40mil | |
| 5.4 | Useful TP and connector labels on silkscreen? Specify polarity of power inputs, DC vs. AC, boot strapping TPs, status LEDs, power rails, and ground TPs. | |
| 5.5 | Light passives (e.g. 0402, 0603 or less) have even amount of copper pours on either side to ensure equal melt distribution? | |
| **6.0** | **Manufacturability** | |
| 6.1 | Min. 3 fiducials per side to ensure manufacturing alignment? | |
| 6.2 | No acid traps (acute angle traces?) | |
| 6.3 | Latest PCB design rules (.RUL) imported as per manufacturer's specifications? | |
| 6.4 | Board thickness/stack-up is 1.6mm / 63mil (for four-layer) PCB? | |
| **7.0** | **RF** | |
| 7.1 | Antenna trace length impedance matched? | |
| 7.2 | Ground vias around perimeter? | |
| 7.3 | External/shielding pins of connector (if applicable) grounded? | |
| **8.0** | **Power Supply** | |
| 8.1 | Bypass caps close to IC, in order of lowest capacitance to highest? | |
| 8.2 | High-frequency traces thick (min. pad thickness, if possible use a plane) | |

| | | |
|---|---|---|
| 8.3 | No traces underneath switching inductor? | |
| 8.4 | Via ampacity: 18-35mil in/out diameter via on power traces? Multiple for connecting large planes (use min. 3 vias or make larger). Check with trace width calculator, specifically for internal layers. | |
| **9.0** | **Bill of Materials (BOM)** | |
| 9.1 | Only CT (Cut Tape) PNs used? (Digi-Reel costs extra $8-10) | |
| 9.2 | Checked twice? | |
| 9.3 | Checked thrice? | |
| **10.0** | **Post Production** | |
| 10.1 | Export 3D STEP model of PCB for enclosure design team | |
| 10.2 | Zip release files and label with board house and order date | |
| 10.3 | Upload all project files to GitHub | |
| 10.4 | Order BOM. If sufficient amount of parts are cheaper through Mouser, Future, etc. and cart is large enough to get free shipping on all orders, then order through multiple distributors. Otherwise, order through DigiKey. | |

FINAL CHECK:

Is the PCB looking SEX? HELL YEAH NAH