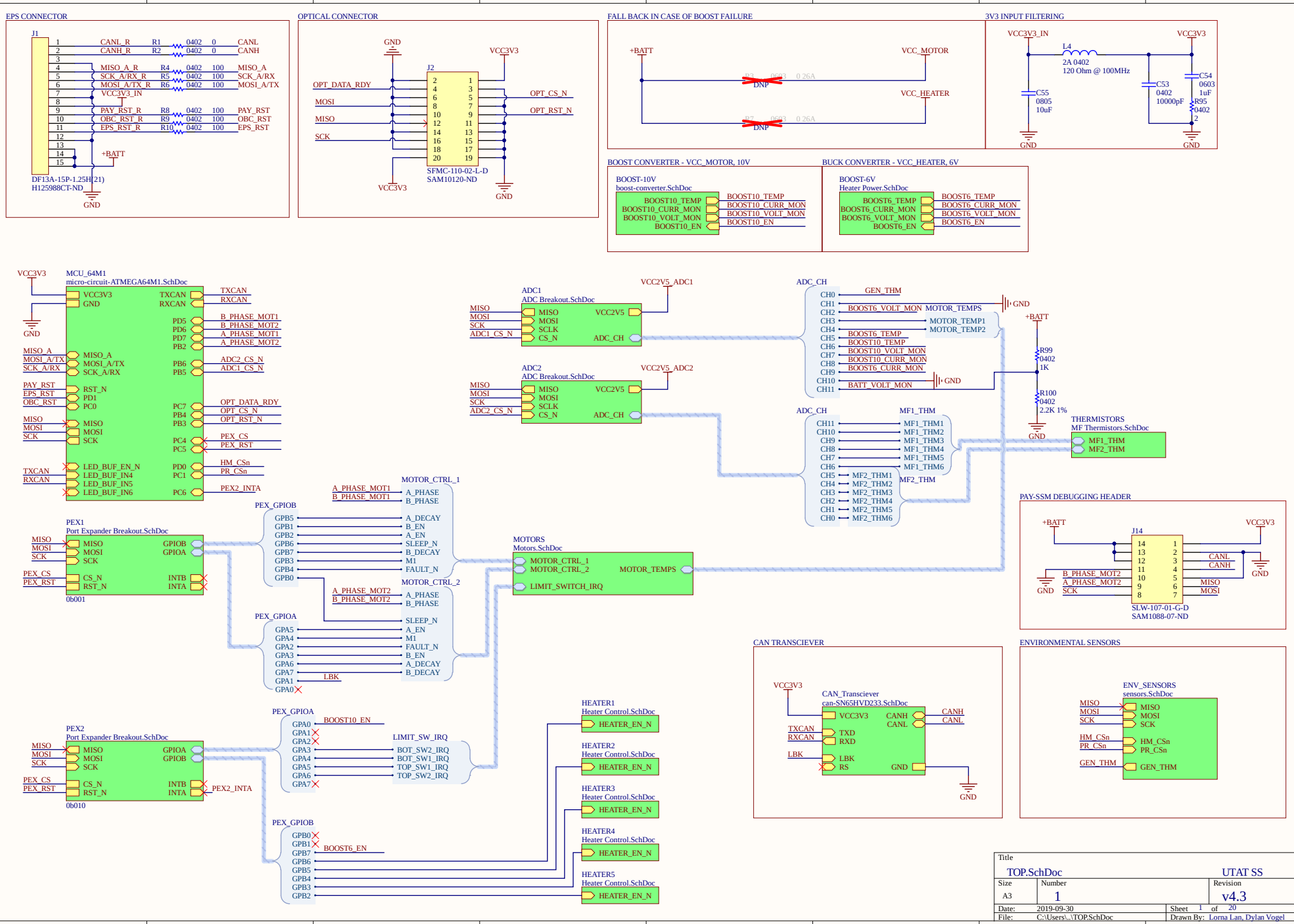
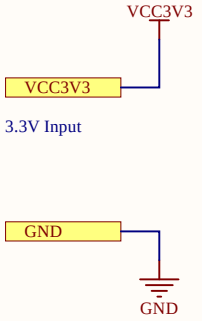
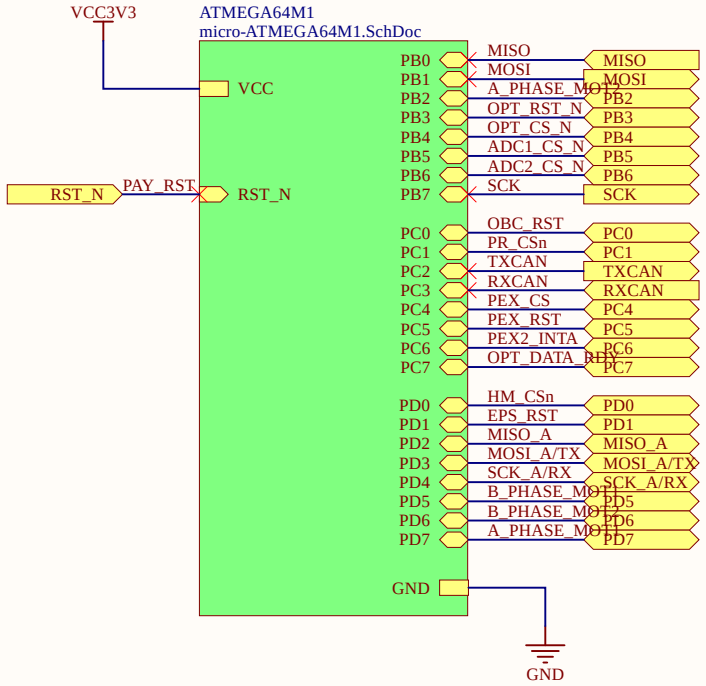

EPS CONNECTOR
J1
CANL_R
CANH_R
MISO_A_R
SCK_A/RX_R
MOSI_A/TX_R
VCC3V3_IN
PAY_RST_R
OBC_RST_R
EPS_RST_R
+BATT
DF13A-15P-1.25H(21)
H125988CT-ND
GND
OPTICAL CONNECTOR
J2
OPT_DATA_RDY
MOSI
MISO
SCK
OPT_CS_N
OPT_RST_N
SFMC-110-02-L-D
SAM10120-ND
FALL BACK IN CASE OF BOOST FAILURE
+BATT
VCC_MOTOR
VCC_HEATER
DNP
3V3 INPUT FILTERING
VCC3V3_IN
VCC3V3
L4
2A 0402
120 Ohm @ 100MHz
C55
0805
10uF
C53
0402
10000pF
C54
0603
1uF
R95
0402
2
BOOST CONVERTER - VCC_MOTOR, 10V
BOOST-10V
boost-converter.SchDoc
BOOST10_TEMP
BOOST10_CURR_MON
BOOST10_VOLT_MON
BOOST10_EN
BUCK CONVERTER - VCC_HEATER, 6V
BOOST-6V
Heater Power.SchDoc
BOOST6_TEMP
BOOST6_CURR_MON
BOOST6_VOLT_MON
BOOST6_EN
MCU_64M1
micro-circuit-ATMEGA64M1.SchDoc
TXCAN
RXCAN
B_PHASE_MOT1
B_PHASE_MOT2
A_PHASE_MOT1
A_PHASE_MOT2
ADC2_CS_N
ADC1_CS_N
OPT_DATA_RDY
OPT_CS_N
OPT_RST_N
PEX_CS
PEX_RST
HM_CSn
PR_CSn
PEX2_INTA
ADC1
ADC Breakout.SchDoc
VCC2V5_ADC1
ADC2
ADC Breakout.SchDoc
VCC2V5_ADC2
ADC_CH
GEN_THM
MOTOR_TEMPS
MOTOR_TEMP1
MOTOR_TEMP2
BATT_VOLT_MON
MF1_THM
MF2_THM
R99
0402
1K
R100
0402
2.2K 1%
THERMISTORS
MF Thermistors.SchDoc
PEX1
Port Expander Breakout.SchDoc
0b001
PEX_GPIOB
PEX_GPIOA
MOTOR_CTRL_1
MOTOR_CTRL_2
A_DECAY
B_DECAY
SLEEP_N
M1
FAULT_N
LBK
MOTORS
Motors.SchDoc
LIMIT_SWITCH_IRQ
PAY-SSM DEBUGGING HEADER
J14
SLW-107-01-G-D
SAM1088-07-ND
PEX2
Port Expander Breakout.SchDoc
0b010
BOOST10_EN
BOOST6_EN
LIMIT_SW_IRQ
BOT_SW2_IRQ
BOT_SW1_IRQ
TOP_SW1_IRQ
TOP_SW2_IRQ
HEATER1
Heater Control.SchDoc
HEATER2
Heater Control.SchDoc
HEATER3
Heater Control.SchDoc
HEATER4
Heater Control.SchDoc
HEATER5
Heater Control.SchDoc
HEATER_EN_N
CAN TRANSCIEVER
CAN_Transciever
can-SN65HVD233.SchDoc
ENVIRONMENTAL SENSORS
ENV_SENSORS
sensors.SchDoc
Title
TOP.SchDoc
UTAT SS
Size
A3
Number
1
Revision
v4.3
Date:
2019-09-30
Sheet 1 of 20
File:
C:\Users\..\TOP.SchDoc
Drawn By:
Lorna Lan, Dylan Vogel

POWER INPUTS

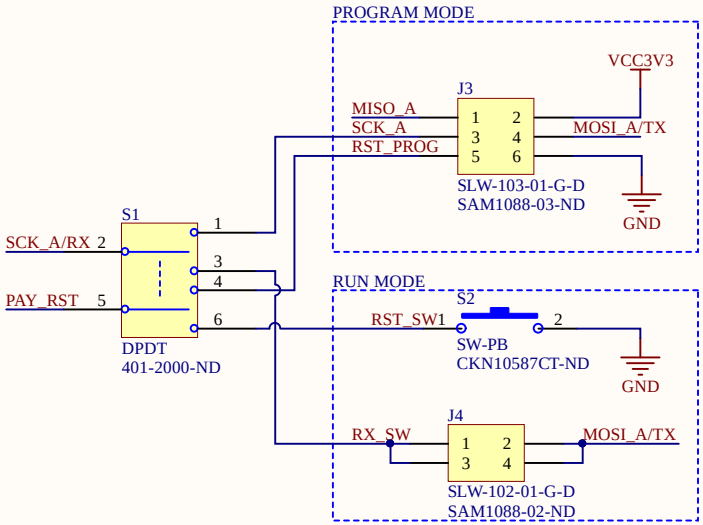


ATMEGA32M1

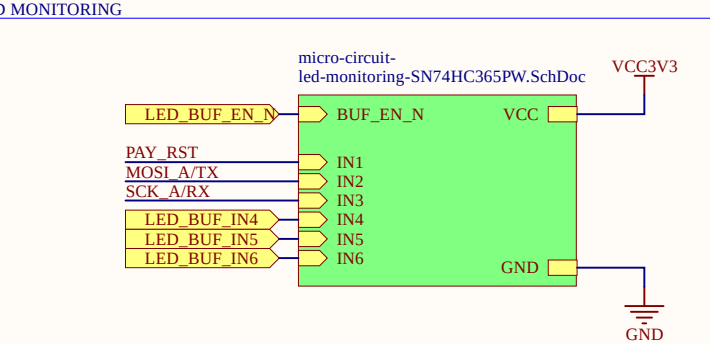


Specific No-ERCs placed for I/O Port and Bidirectional Sheet Entry

MODE SELECT CIRCUITRY



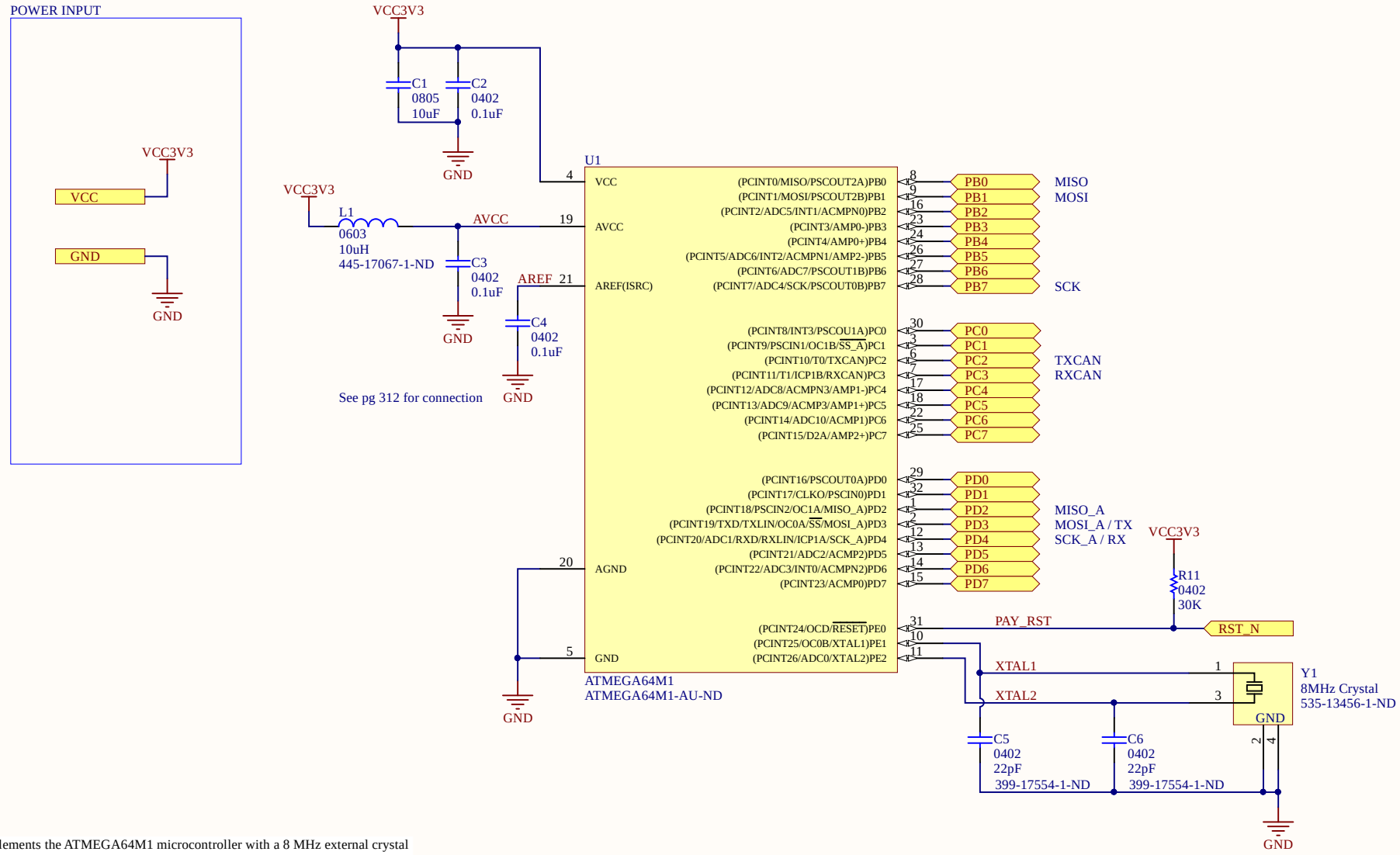
LED MONITORING



This schematic extends the functionality already included in the micro-ATMEGA32M1 schematc, adding a mode select switch, programming header, reset button and LED indication for TX, RX and RSTn.

- IN[4:6] of the LED buffer have been left unconnected, but are broken out on ports LED_BUF_IN[4:6]. They can be connected in the schematic which includes this sheet to monitor up to an additional 3 lines. Highly recommend more blinking lights.

Title	micro-circuit-ATMEGA64M1.SchDoc	UTAT SS
Size: A4	Number: PCBS-COMMON	Revision: 1.1
Date: 2019-09-30	Sheet 2 of 20	
File: C:\Users\..\micro-circuit-ATMEGA64M1.SchDoc	Drawn By: Dylan Vogel	

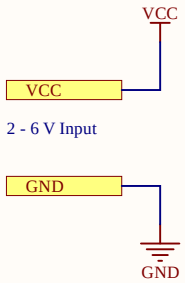


This schematic implements the ATMEGA64M1 microcontroller with a 8 MHz external crystal and necessary power connections.

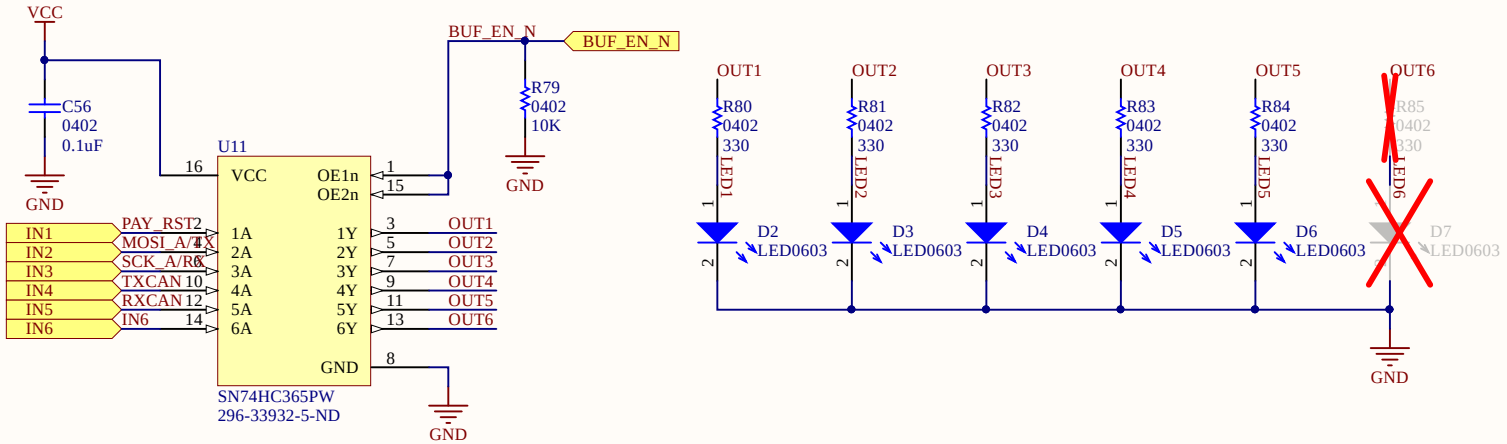
- Crystal is connected in a Pierce configuration, values of the capacitors were calculated based on the capacitance of the crystal and ESR.
- I would read through 18.5.2 and 18.6.2 of the complete 64M1 datasheet if you're interested in the motivation behind the ADC input connections. They recommend connecting AVCC through a RC lowpass network to minimize noise.
- If the ADC functionality of the device is used, either AVCC or the internal 2.56 V source can be seleted in software as the reference voltage.

Title	micro-ATMEGA64M1.SchDoc	UTAT SS
Size: A4	Number: PCBS-COMMON	Revision: 1.1
Date: 2019-09-30	Sheet 3 of 20	
File: C:\Users\..\micro-ATMEGA64M1.SchDoc	Drawn By: Dylan Vogel	

INPUT POWER



LED BUFFER

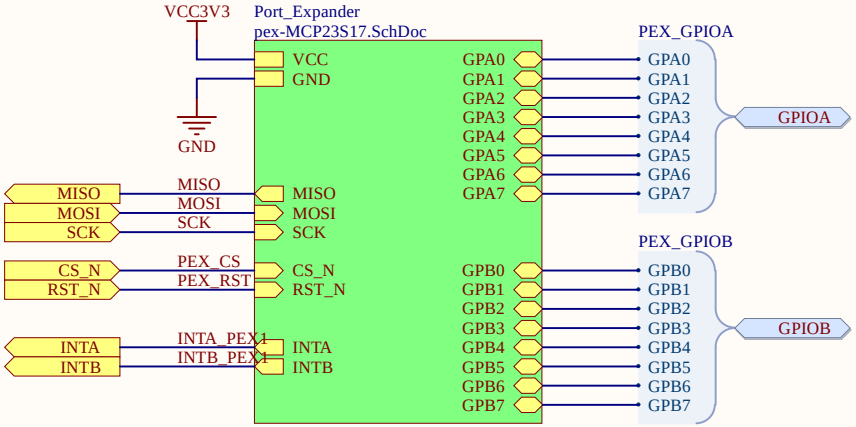


This schematic implements the SN74HC365PW non-inverting, tri-state hex buffer as an LED monitoring circuit. Connecting a signal to IN[1:6] will light up the corresponding LED on OUT[1:6].

- The BUF_EN_N input can be connected to a mircocontroller to control the buffer. An input HIGH will set the outputs to high-impedance and disable the LEDs.
- In the schematic symbol which references this schematic sheet, parameters LED[1:6] can be added to specify the colour of each LED. See the micro-circuit common sheet for an example of this.
- Unconnected inputs should be grounded if you don't want random flickering of the LEDs.

Title	led-monitoring-SN74HC365PW.SchDoc	UTAT SS
Size: A4	Number: PCBS-COMMON	Revision: 1.1
Date: 2019-09-30	Sheet 4 of 20	
File: C:\Users\..\led-monitoring-SN74HC365PW.SchDoc	Drawn By: Dylan Vogel	

PORT EXPANDER

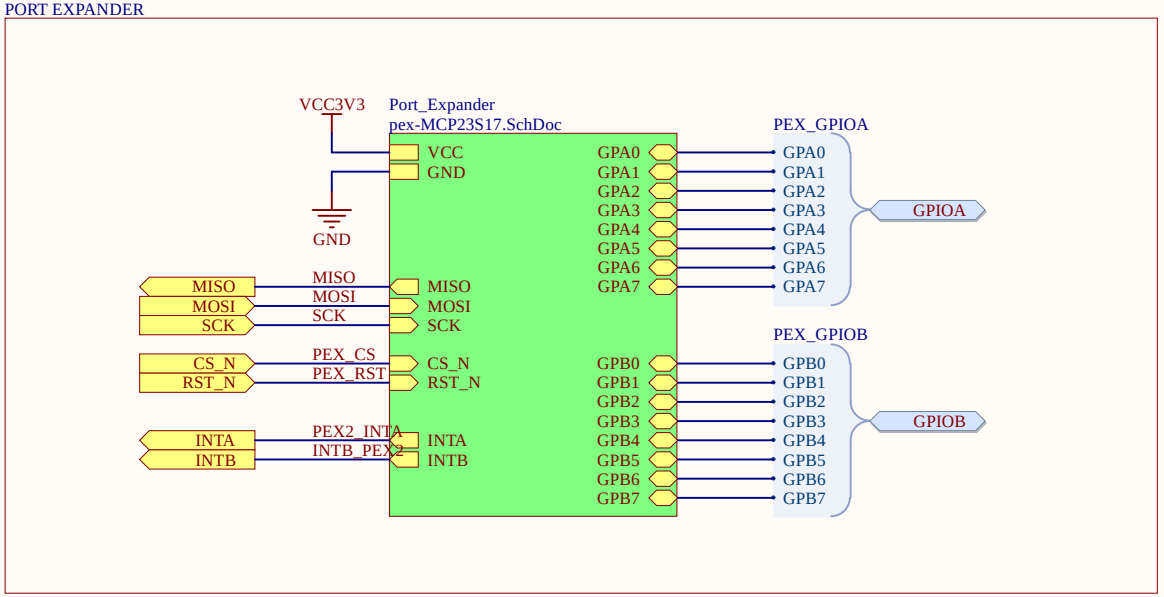


Breaks out the Port Expander GPIOs into harnesses

ADDRESS: 0b001

Title	Port Expander Breakout.SchDoc		UTAT SS
Size	Number		Revision
A4	5		v4.2
Date:	2019-09-30	Sheet 5	of 20
File:	C:\Users\..\Port Expander Breakout.SchDoc	Drawn By:	Dylan Vogel

PORT EXPANDER

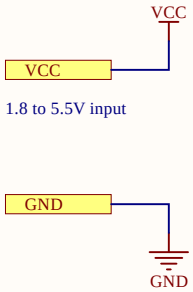


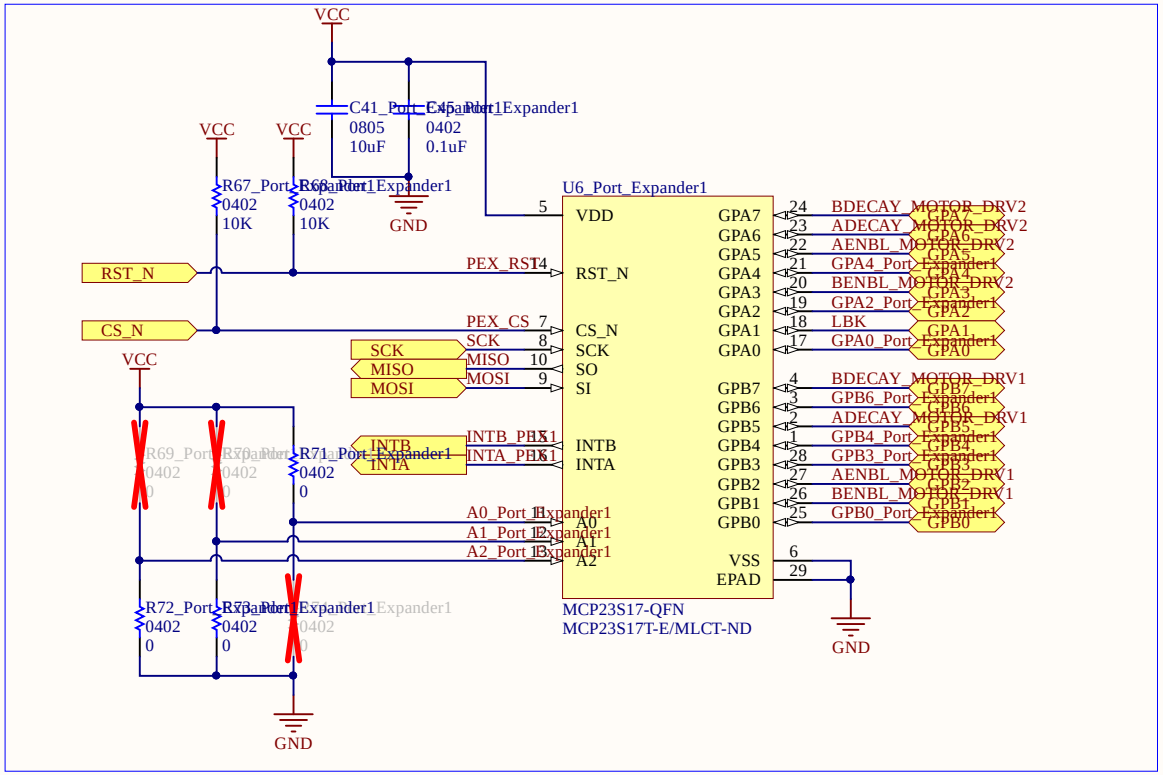
Breaks out the Port Expander GPIOs into harnesses

ADDRESS: 0b010

Title	Port Expander Breakout.SchDoc		UTAT SS
Size: A4	Number: 5		Revision: v4.2
Date: 2019-09-30		Sheet 5 of 20	
File: C:\Users\..\Port Expander Breakout.SchDoc		Drawn By: Dylan Vogel	

POWER INPUTS





ADDRESS: 0b001

CHANNEL SELECTION

ONLY SOLDER ONE 0 OHM FROM EACH PAIR
PEX ADDRESS = A2 A1 A0
VCC == 1 GND == 0

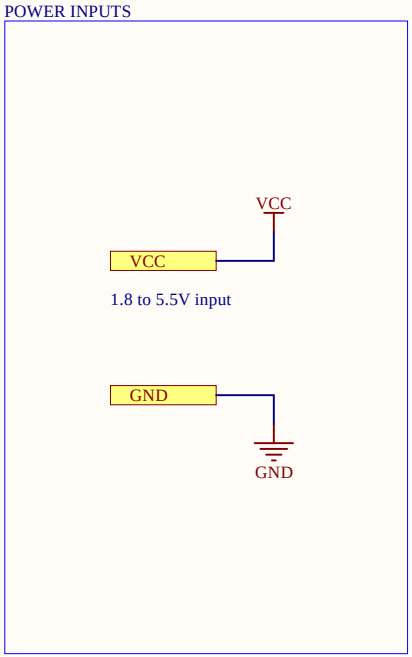
This schematic implements the MCP23S17 SPI port expander, and does some common-sense things like adding a bypass capacitor to the power supply and pull-up resistors to RST_N and CS_N.

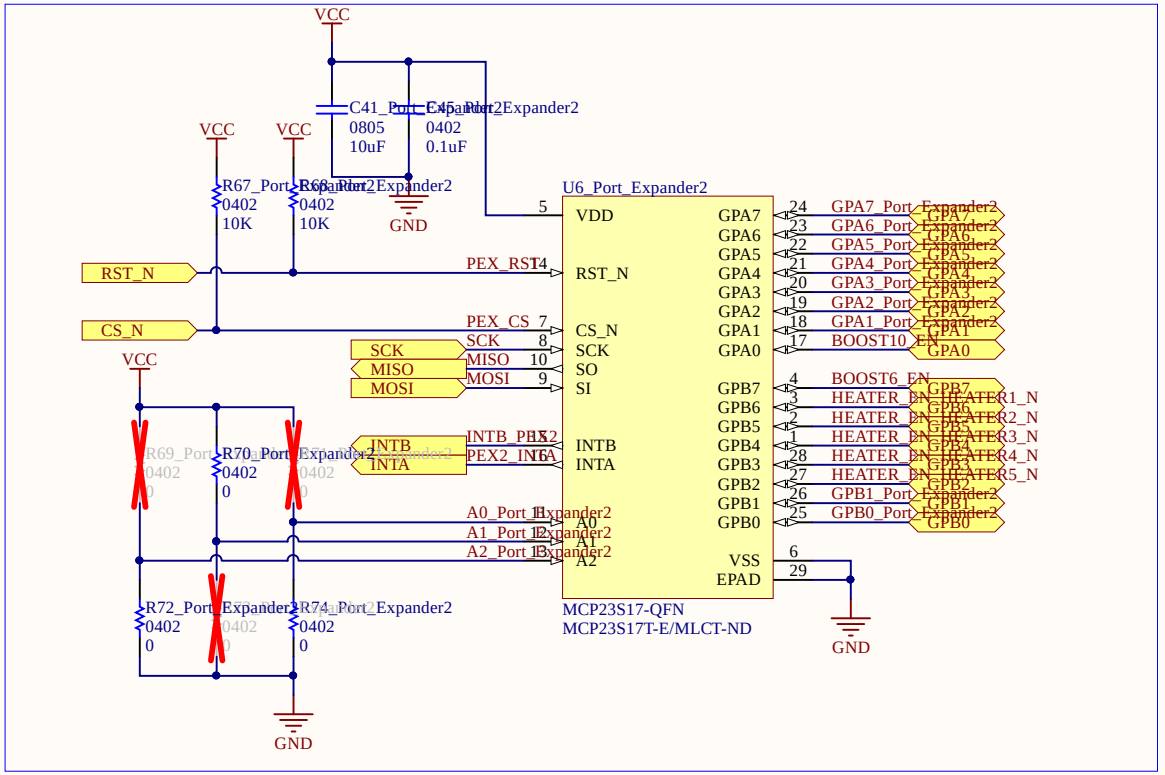
Multiple port expanders can be connected to the same CS_N line, and accessed via a device address that is used during software communication. This address is set in hardware via the A2, A1 and A0 pins. Soldering a 0 ohm resistor to VCC will set that bit to 1, and soldering to GND will set that bit to 0.

In the schematic which includes this file, you should make some note of the relevant hardware address that should be soldered during manufacturing.

Title	pex-MCP23S17.SchDoc	UTAT SS
Size: A4	Number: PCBS-COMMON	Revision: 1.1
Date: 2019-09-30	Sheet 6 of 20	
File: C:\Users\..\pex-MCP23S17.SchDoc	Drawn By: Dylan Vogel	

POWER INPUTS





ADDRESS: 0b010

CHANNEL SELECTION

ONLY SOLDER ONE 0 OHM FROM EACH PAIR
PEX ADDRESS = A2 A1 A0
VCC == 1 GND == 0

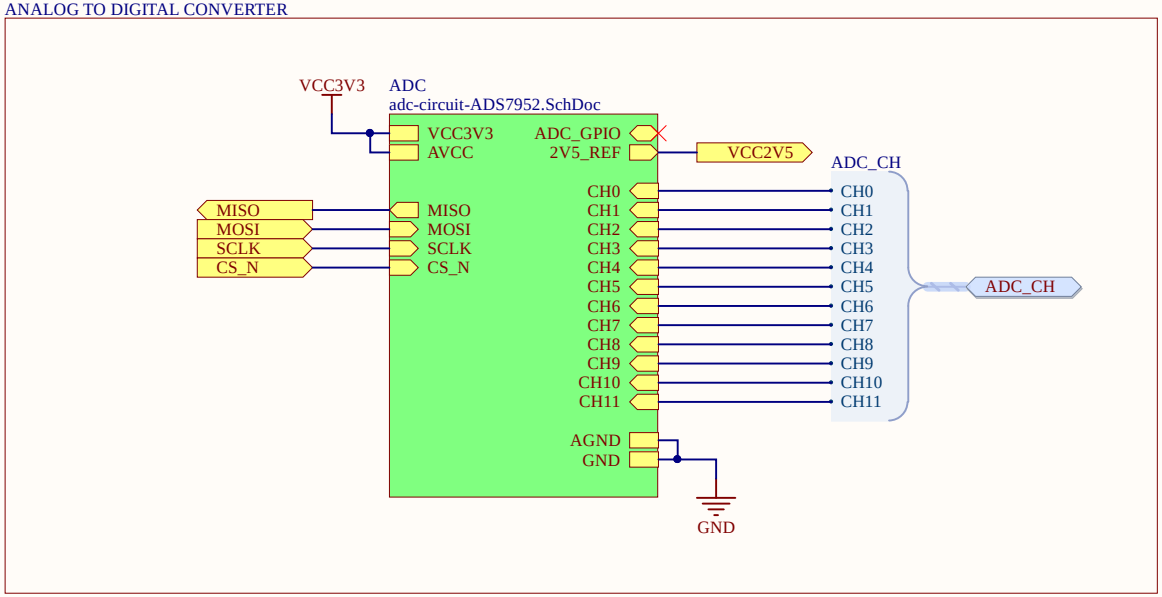
This schematic implements the MCP23S17 SPI port expander, and does some common-sense things like adding a bypass capacitor to the power supply and pull-up resistors to RST_N and CS_N.

Multiple port expanders can be connected to the same CS_N line, and accessed via a device address that is used during software communication. This address is set in hardware via the A2, A1 and A0 pins. Soldering a 0 ohm resistor to VCC will set that bit to 1, and soldering to GND will set that bit to 0.

In the schematic which includes this file, you should make some note of the relevant hardware address that should be soldered during manufacturing.

Title	pex-MCP23S17.SchDoc	UTAT SS
Size: A4	Number: PCBS-COMMON	Revision: 1.1
Date: 2019-09-30	Sheet 6 of 20	
File: C:\Users\..\pex-MCP23S17.SchDoc	Drawn By: Dylan Vogel	

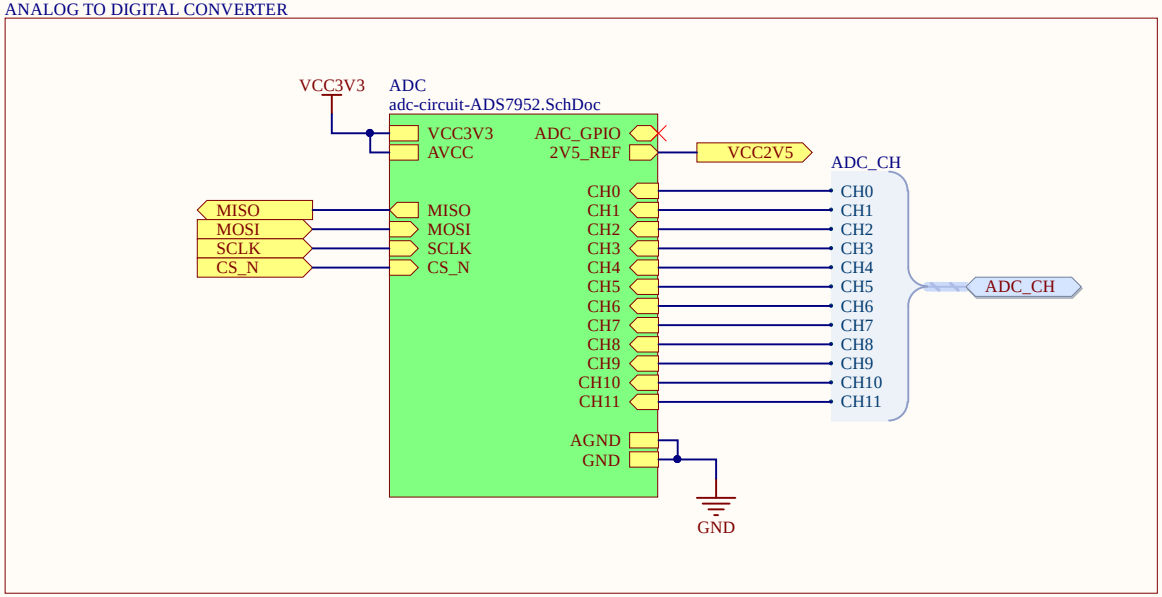
ANALOG TO DIGITAL CONVERTER



Breaks out the ADC channels into harnesses

Title	ADC Breakout.SchDoc	UTAT SS
Size: A4	Number: 7	Revision: v4.2
Date: 2019-09-30		Sheet 7 of 20
File: C:\Users\..\ADC Breakout.SchDoc		Drawn By: Lorna Lan, Dylan Vogel

ANALOG TO DIGITAL CONVERTER

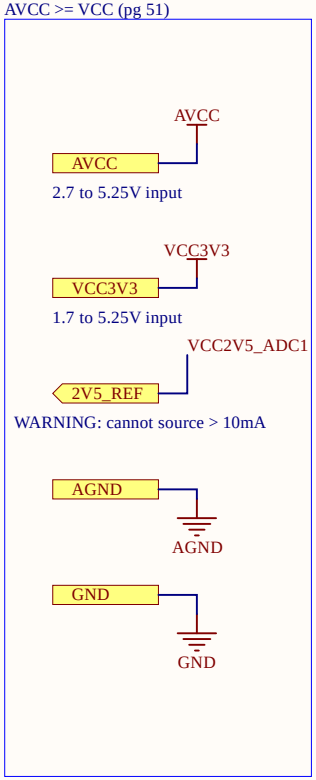


Breaks out the ADC channels into harnesses

Title	ADC Breakout.SchDoc	UTAT SS
Size: A4	Number: 7	Revision: v4.2
Date: 2019-09-30		Sheet 7 of 20
File: C:\Users\..\ADC Breakout.SchDoc		Drawn By: Lorna Lan, Dylan Vogel

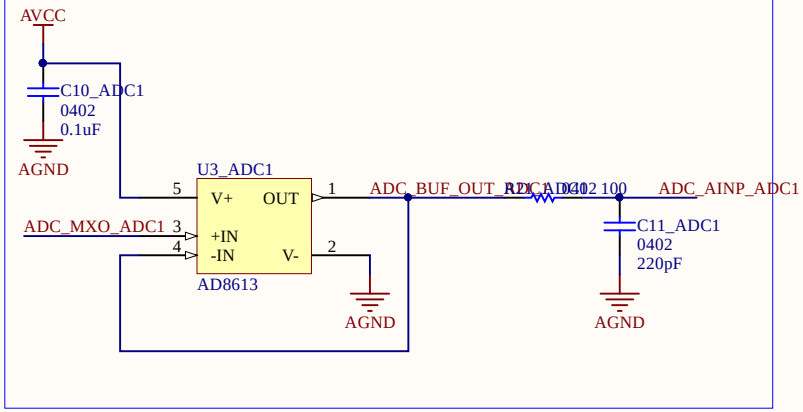
POWER PORTS

AVCC >= VCC (pg 51)



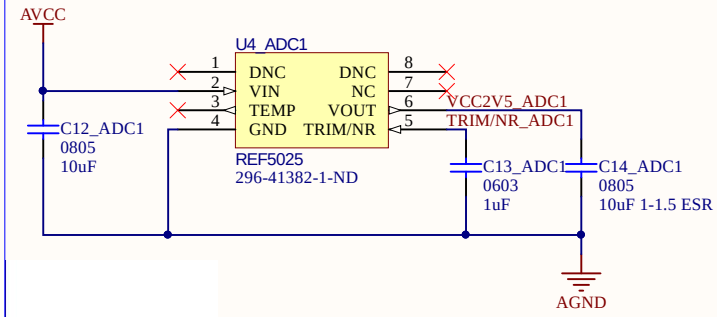
ADC INPUT BUFFER

See pg. 50 for discussion of unity buffer design procedure

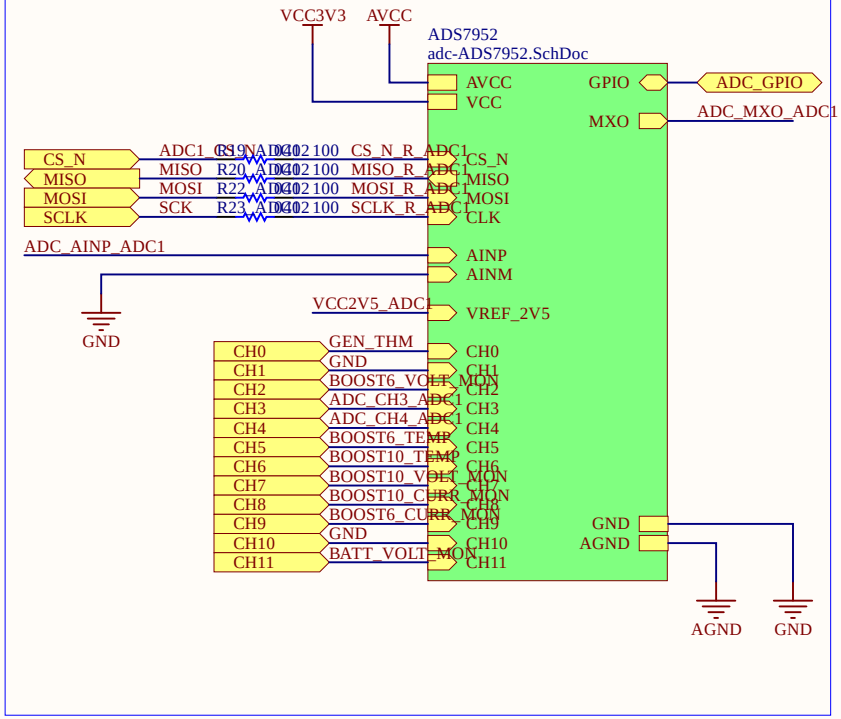


2V5 REFERENCE

Output cap should have ESR from 1 - 1.5 ohm (see pg. 21)



ADC



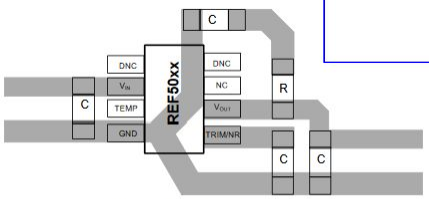


Figure 44. Layout Example

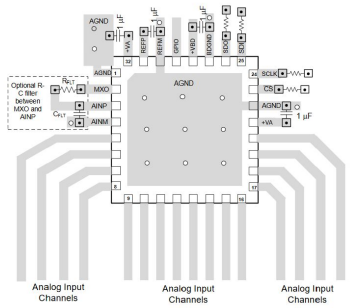


Figure 70. Recommended Layout for the VQFN Packaged Device

This schematic implements the ADS7952 analog-to-digital converter with a 2.5V reference and a unity-gain buffer on the output of the internal multiplexer.
- Recommended input impedance should be < 1K. Higher source impedances possible with slower sampling.
- Breaks out 2V5 for use as reference outside the circuit
- All necessary bypassing and pull-ups implemented in the ADS7952 schematic
- In most low-performance applications, AVCC and VCC can be tied together
- In the layout, the pins tied to AGND should be put on a local GND pour and then tied to the global ground plane with low-impedance.
- 100 ohm resistors on the SPI input help to isolate the ADC from digital noise

Title: adc-circuit-ADS7952.SchDoc		UTAT SS
Size: A4	Number: PCBS-COMMON	Revision: 1.1
Date: 2019-09-30	Sheet 8 of 20	
File: C:\Users\..\adc-circuit-ADS7952.SchDoc	Drawn By: Dylan Vogel	

POWER PORTS

AVCC >= VCC (pg 51)

AVCC

2.7 to 5.25V input

VCC3V3

1.7 to 5.25V input

MF_THM1_IN6

2V5_REF

WARNING: cannot source > 10mA

AGND

GND

ADC INPUT BUFFER

See pg. 50 for discussion of unity buffer design procedure

C10_ADC2
0402
0.1uF

U3_ADC2

V+ OUT

+IN

-IN V-

AD8613

ADC_MXO_ADC2

ADC_BUF_OUT_R21_ADC2 100

ADC_AINP_ADC2

C11_ADC2
0402
220pF

2V5 REFERENCE

Output cap should have ESR from 1 - 1.5 ohm (see pg. 21)

U4_ADC2

DNC DNC

VIN NC

TEMP VOUT

GND TRIM/NR

REF5025
296-41382-1-ND

MF_THM1_IN6

TRIM/NR_ADC2

C12_ADC2
0805
10uF

C13_ADC2
0603
1uF

C14_ADC2
0805
10uF 1-1.5 ESR

ADC

ADS7952
adc-ADS7952.SchDoc

AVCC GPIO ADC_GPIO

VCC

MXO ADC_MXO_ADC2

CS_N MISO MOSI SCLK

ADC_AINP_ADC2

MF_THM1_IN6

CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7 CH8 CH9 CH10 CH11

MF2_THM6 MF2_THM5 MF2_THM4 MF2_THM3 MF2_THM2 MF2_THM1 MF1_THM6 MF1_THM5 MF1_THM4 MF1_THM3 MF1_THM2 MF1_THM1

GND AGND

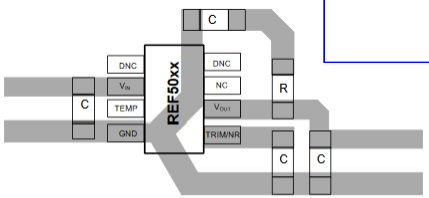


Figure 44. Layout Example

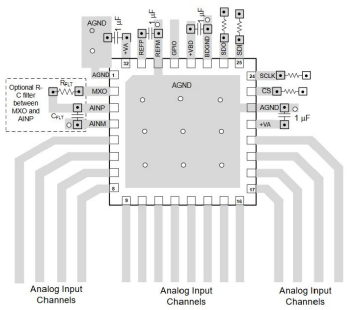


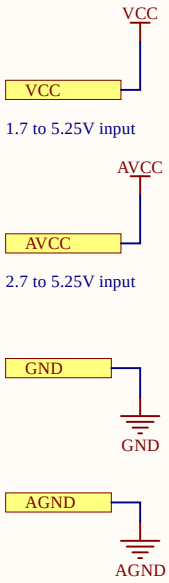
Figure 70. Recommended Layout for the VQFN Packaged Device

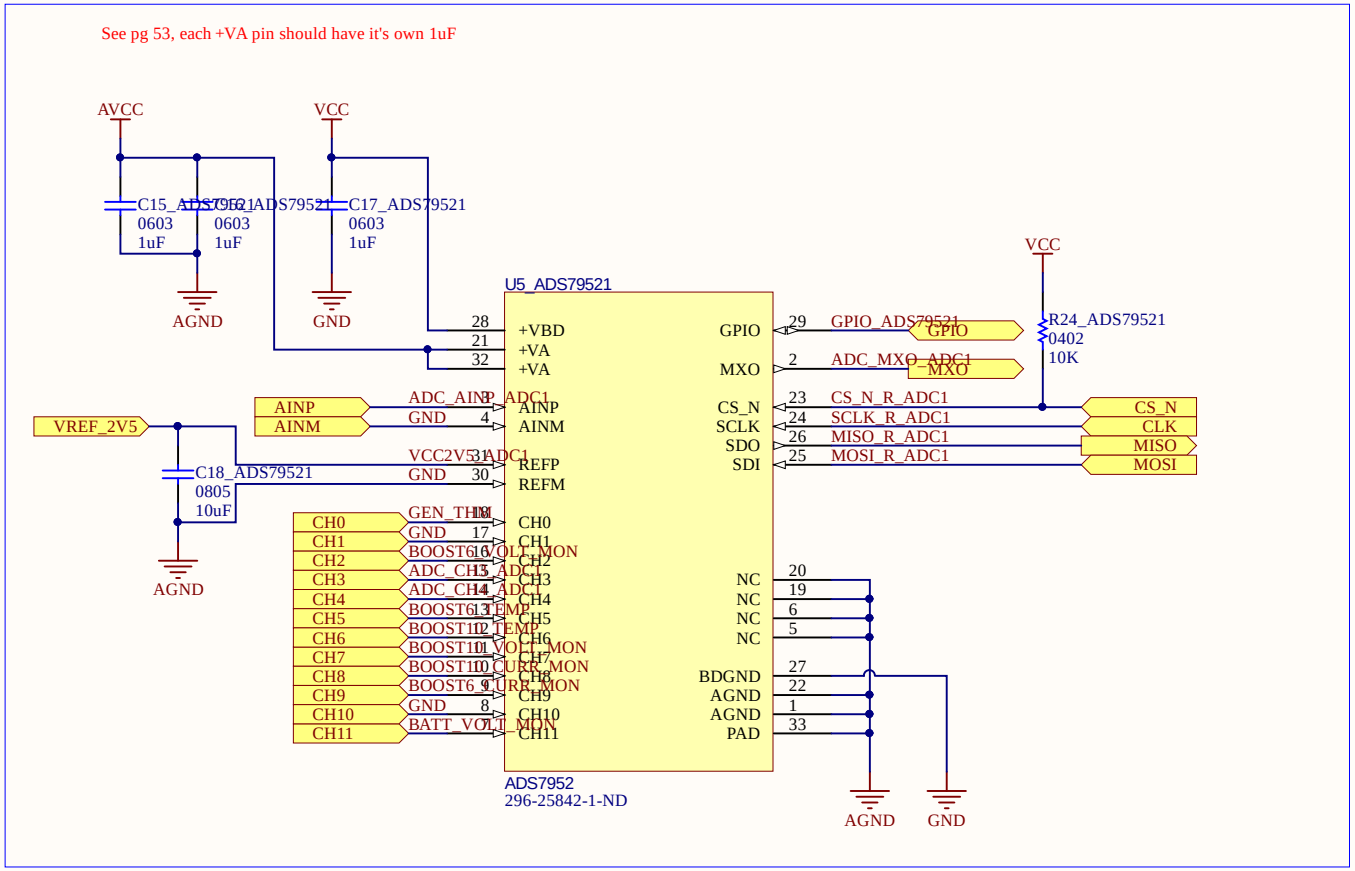
This schematic implements the ADS7952 analog-to-digital converter with a 2.5V reference and a unity-gain buffer on the output of the internal multiplexer.
- Recommended input impedance should be < 1K. Higher source impedances possible with slower sampling.
- Breaks out 2V5 for use as reference outside the circuit
- All necessary bypassing and pull-ups implemented in the ADS7952 schematic
- In most low-performance applications, AVCC and VCC can be tied together
- In the layout, the pins tied to AGND should be put on a local GND pour and then tied to the global ground plane with low-impedance.
- 100 ohm resistors on the SPI input help to isolate the ADC from digital noise

Title	adc-circuit-ADS7952.SchDoc	UTAT SS
Size: A4	Number: PCBS-COMMON	Revision: 1.1
Date: 2019-09-30	Sheet 8 of 20	
File: C:\Users\..\adc-circuit-ADS7952.SchDoc	Drawn By: Dylan Vogel	

POWER INPUTS

AVCC >= VCC (pg 51)

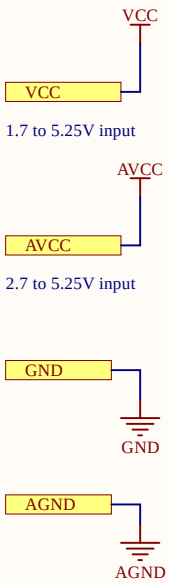




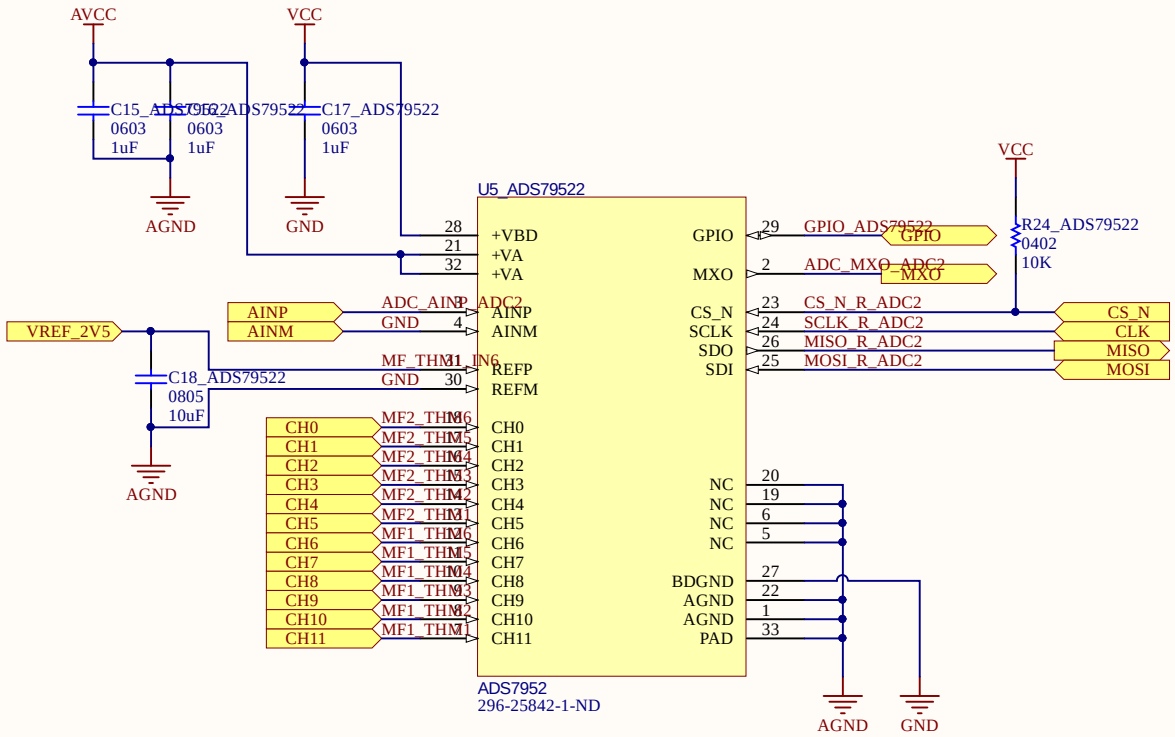
12 CHANNEL ADC

Title	adc-ADS7952.SchDoc	UTAT SS
Size: A4	Number: PCBS-COMMON	Revision: 1.1
Date: 2019-09-30	Sheet 9 of 20	
File: C:\Users\..\adc-ADS7952.SchDoc	Drawn By: Dylan Vogel	

POWER INPUTS
AVCC >= VCC (pg 51)

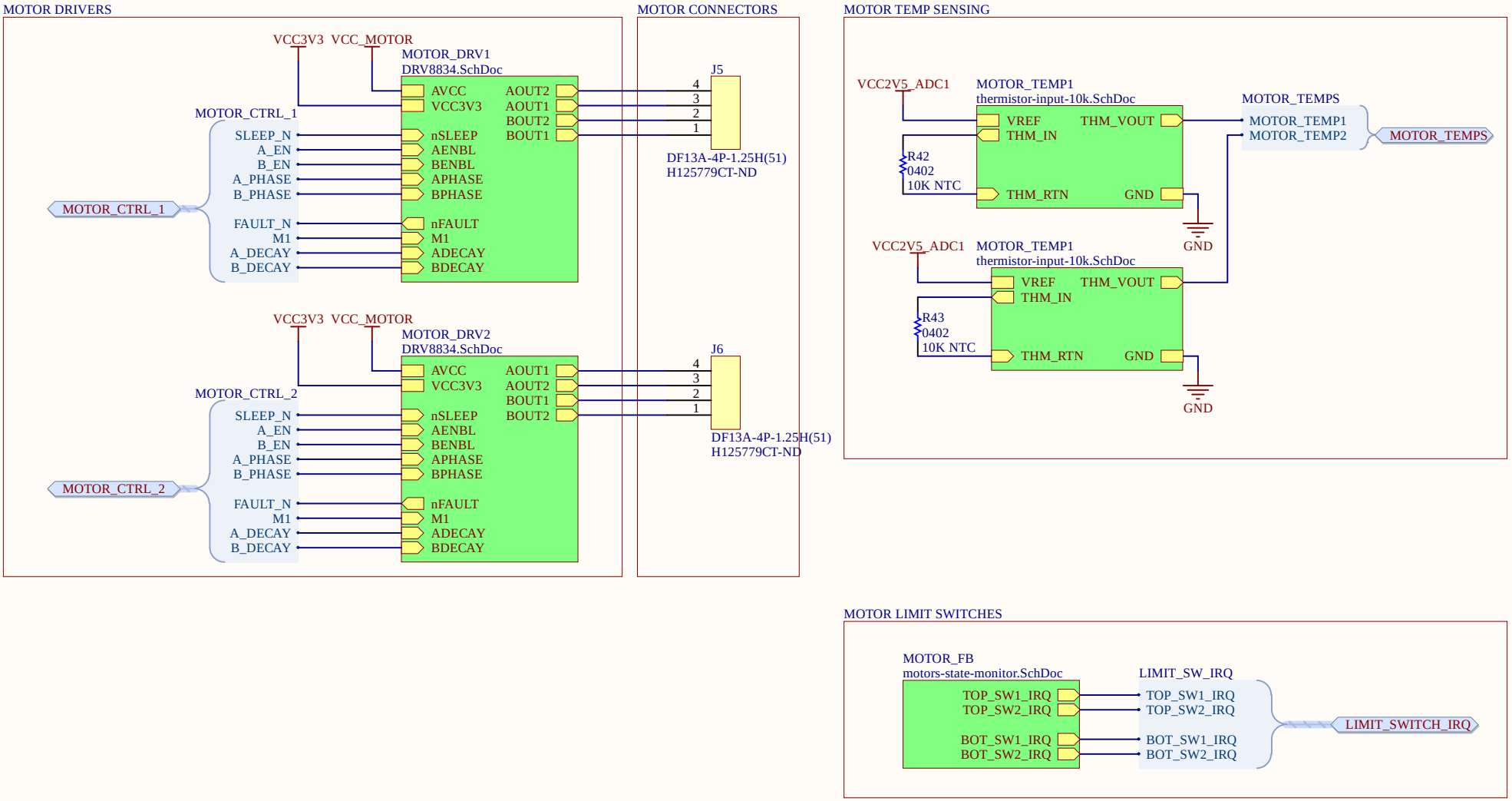


See pg 53, each +VA pin should have it's own 1uF



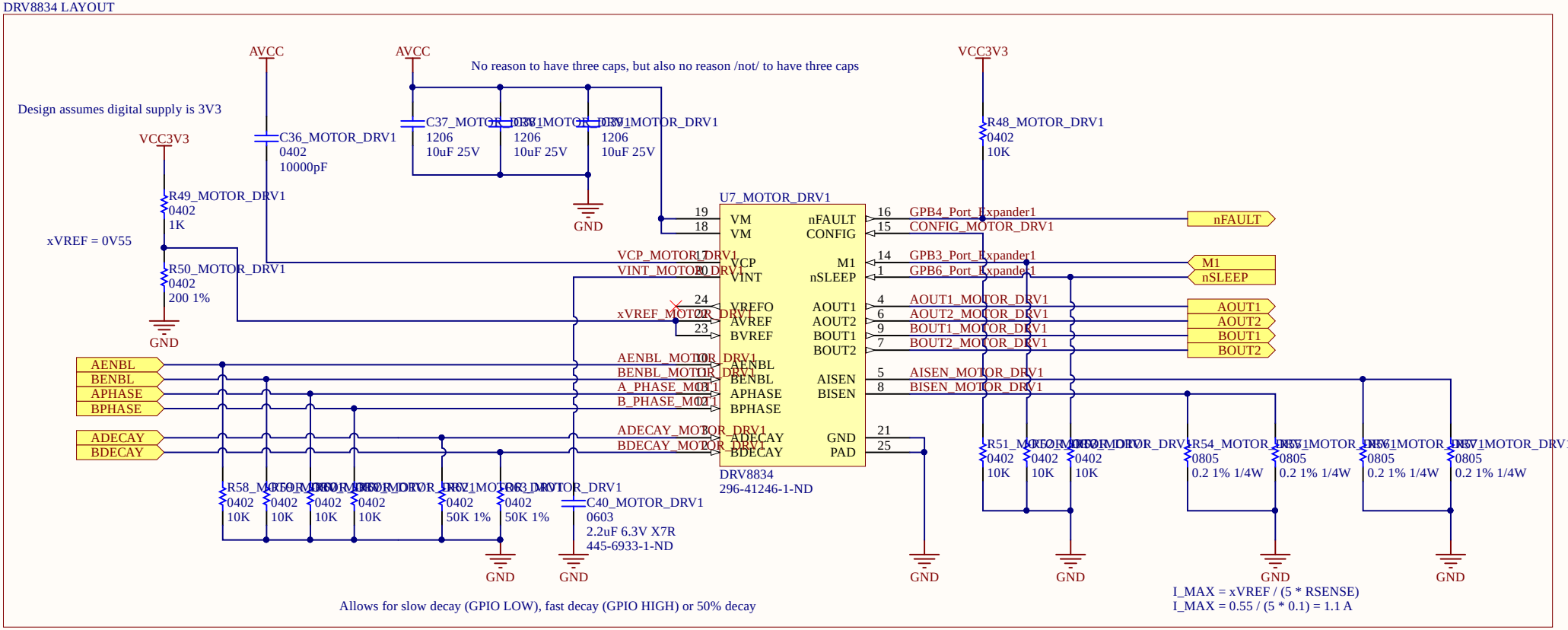
12 CHANNEL ADC

Title	adc-ADS7952.SchDoc	UTAT SS
Size: A4	Number: PCBS-COMMON	Revision: 1.1
Date: 2019-09-30	Sheet 9 of 20	
File: C:\Users\..\adc-ADS7952.SchDoc	Drawn By: Dylan Vogel	



Title	Motors.SchDoc	UTAT SS
Size	Number	Revision
A4	11	v4.2
Date: 2019-09-30		Sheet 11 of 20
File: C:\Users\..\Motors.SchDoc		Drawn By: Lorna Lan, Dylan Vogel

DRV8834 LAYOUT



DRV8834 Motor Driver Notes

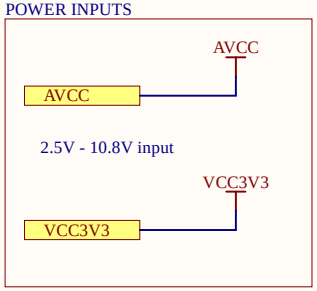
Datasheet: http://www.ti.com/lit/ds/symlink/drv8834.pdf

Indexer mode of this motor driver was tested to be not functioning, so everything is set in hardware to implement only the PHASE/ENABLE mode.

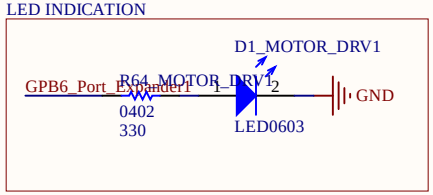
Implemented a voltage divider to set-up the xVREF voltage if want to modify xISEN and the resistor later. VREFO is left unconnected.

About decay settings: decay mode is selected by the voltage presented at the xDECAY pins in PHASE/ENABLE mode. It is also recommended with a pull-down to ground and a GPIO for setting.

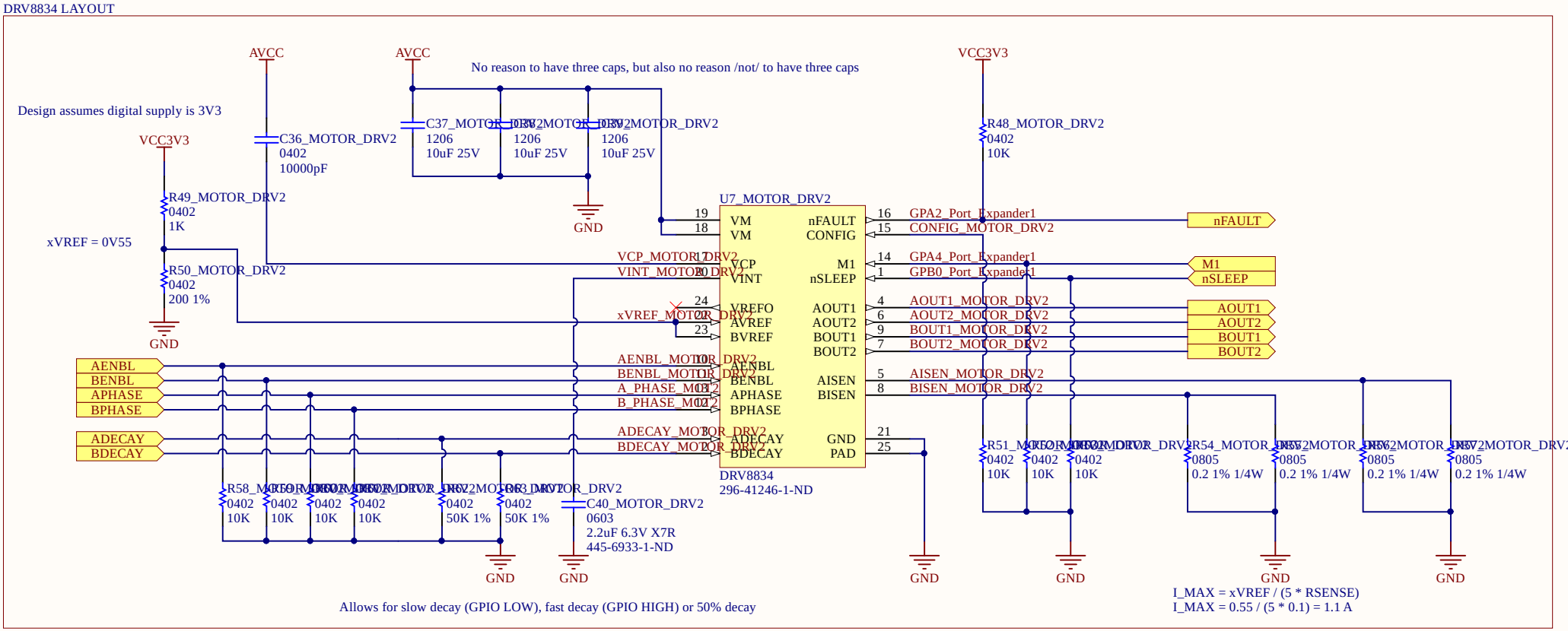
POWER INPUTS



LED INDICATION



Title	DRV8834.SchDoc	UTAT SS
Size: A4	Number: 12	Revision: v4.2
Date: 2019-09-30	Sheet 12 of 20	
File: C:\Users\..\DRV8834.SchDoc	Drawn By: Lorna Lan, Dylan Vogel	



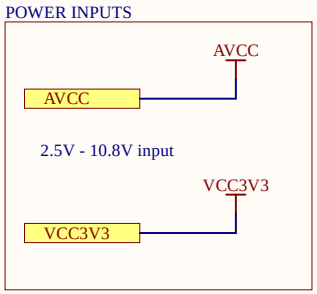
DRV8834 Motor Driver Notes

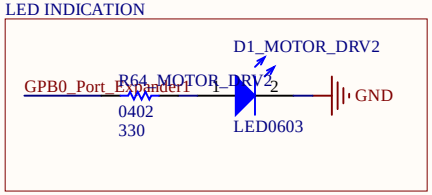
Datasheet: http://www.ti.com/lit/ds/symlink/drv8834.pdf

Indexer mode of this motor driver was tested to be not functioning, so everything is set in hardware to implement only the PHASE/ENABLE mode.

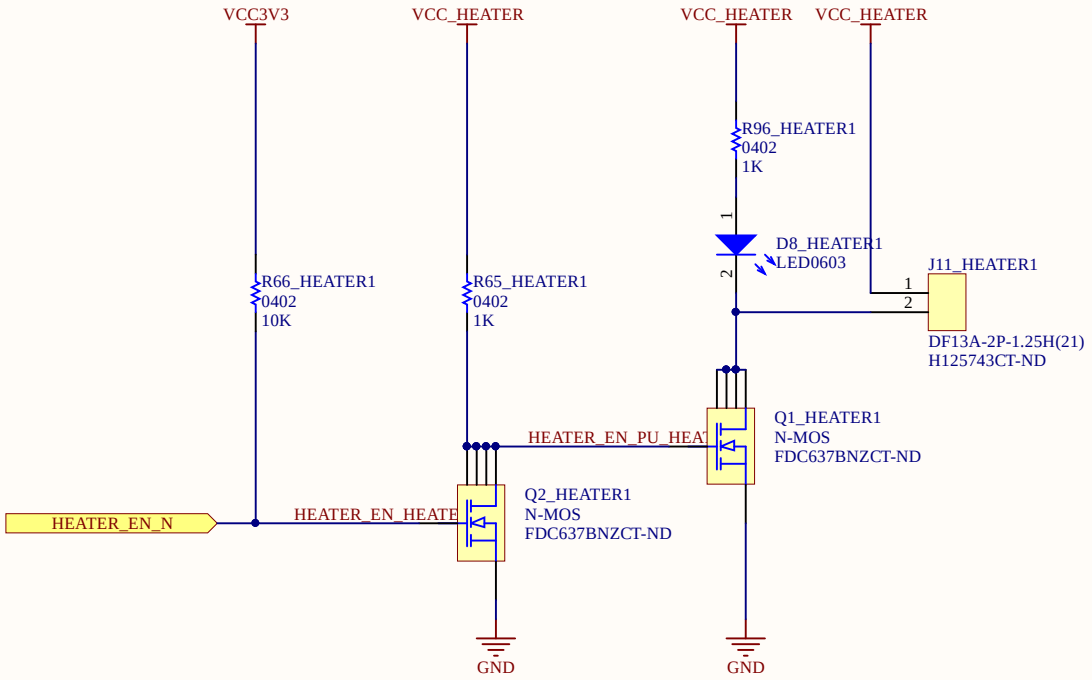
Implemented a voltage divider to set-up the xVREF voltage if want to modify xISEN and the resistor later. VREFO is left unconnected.

About decay settings: decay mode is selected by the voltage presented at the xDECAY pins in PHASE/ENABLE mode. It is also recommended with a pull-down to ground and a GPIO for setting.

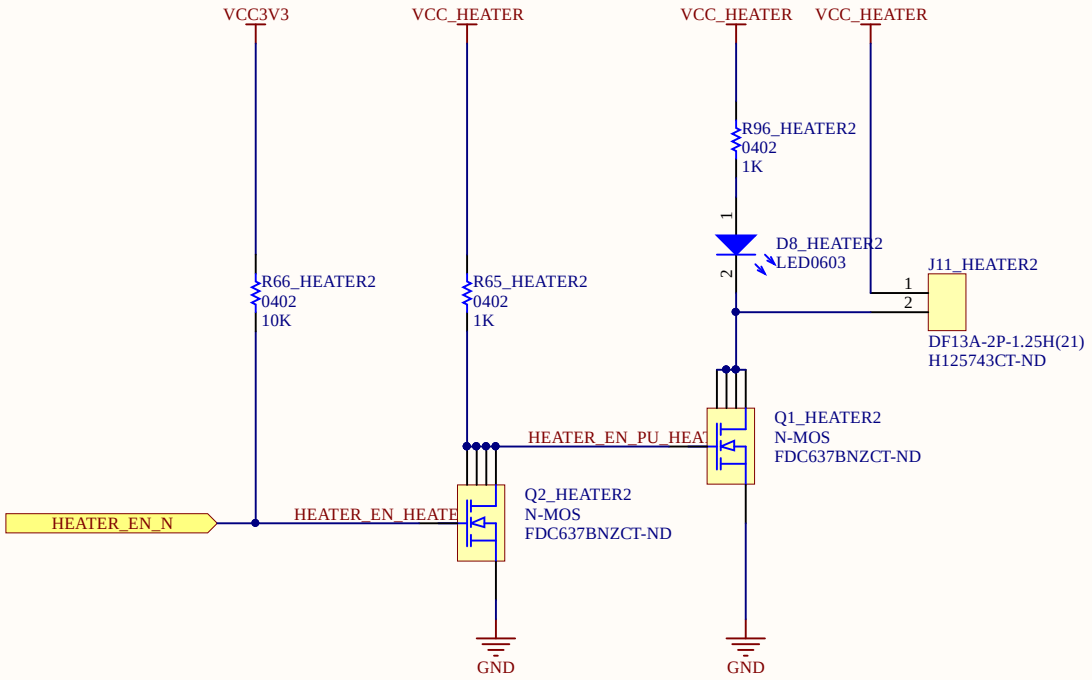




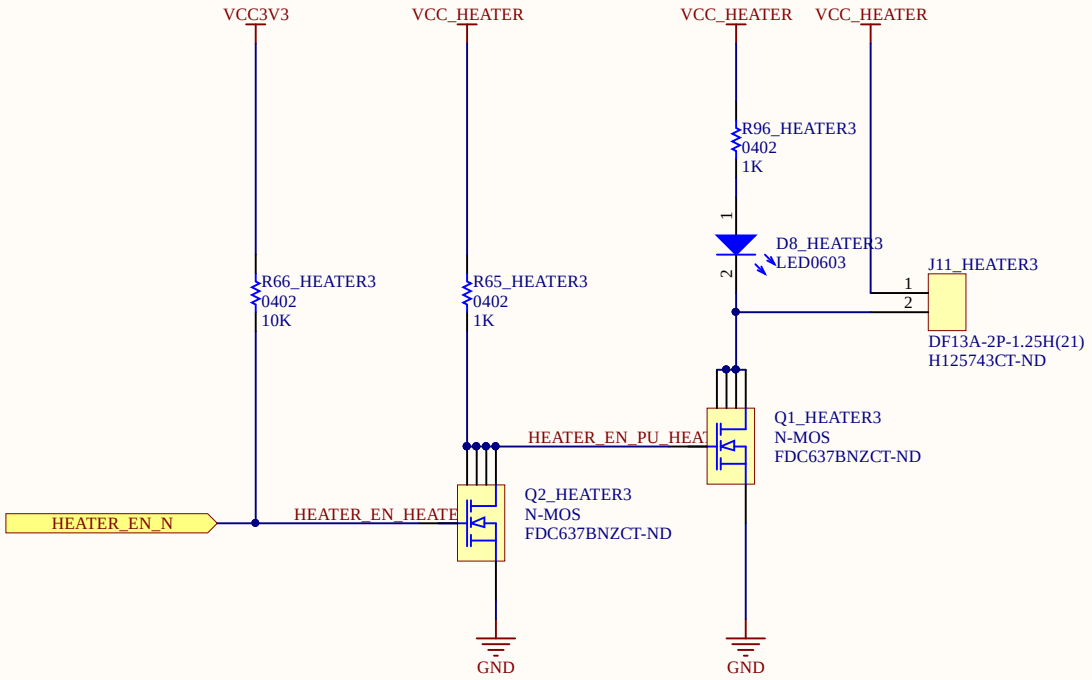
Title	DRV8834.SchDoc	UTAT SS
Size: A4	Number: 12	Revision: v4.2
Date: 2019-09-30	Sheet 12 of 20	
File: C:\Users\..\DRV8834.SchDoc	Drawn By: Lorna Lan, Dylan Vogel	



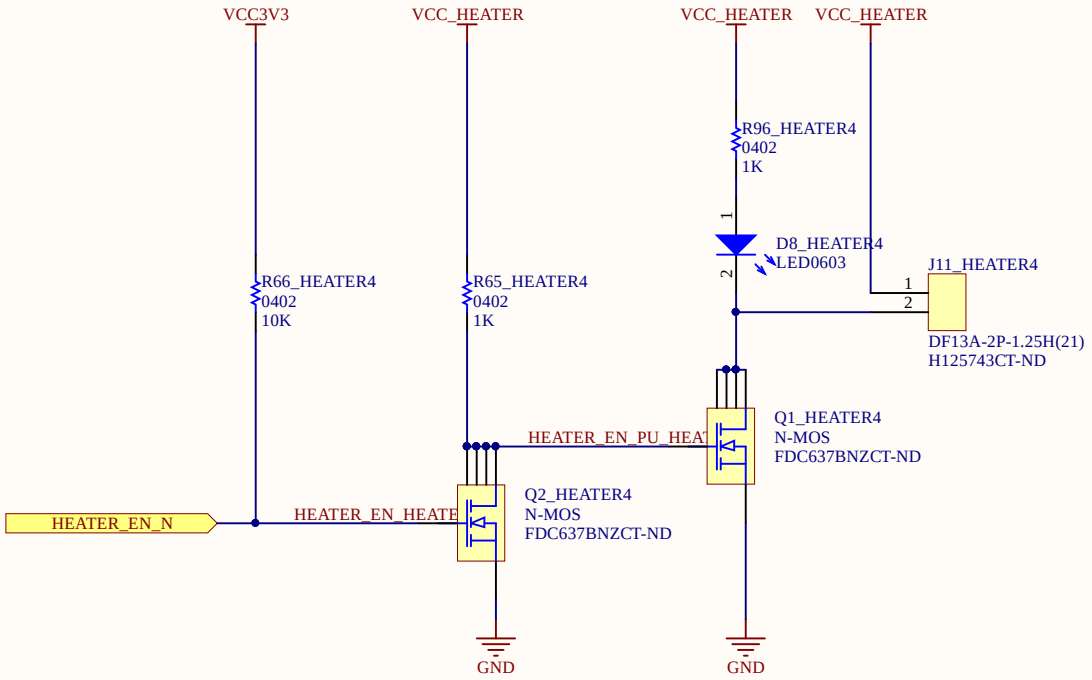
Title	Heater Control.SchDoc		UTAT SS
Size	Number		Revision
A4	15		v4.2
Date:	2019-09-30	Sheet 15	of 20
File:	C:\Users\..\Heater Control.SchDoc	Drawn By:	Lorna Lan



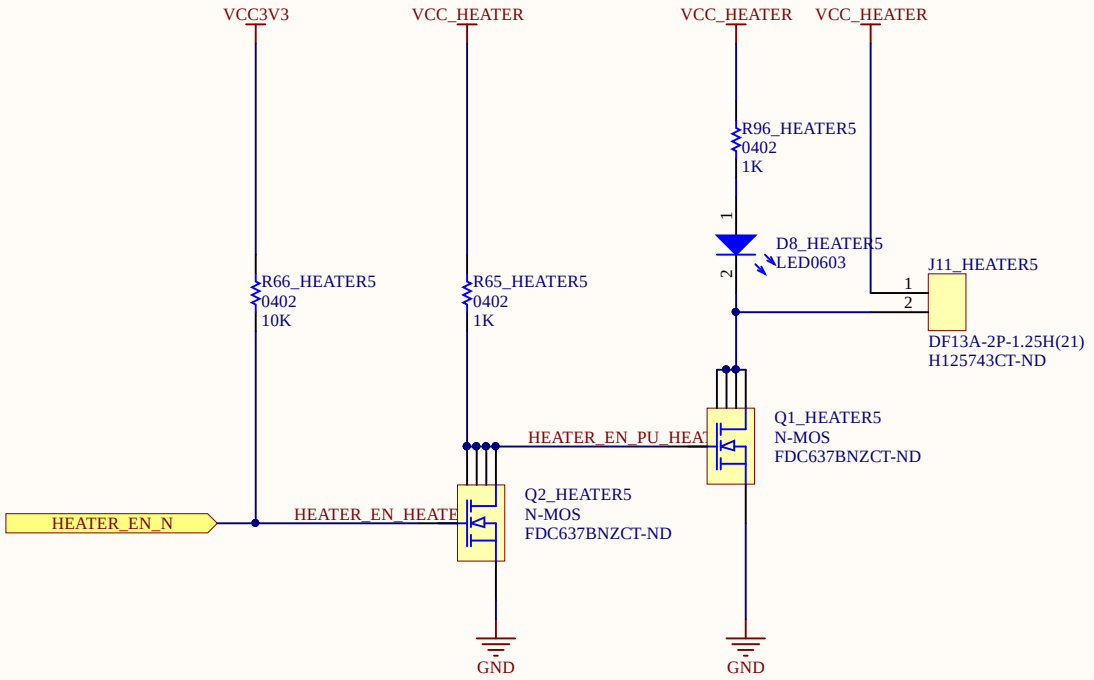
Title	Heater Control.SchDoc		UTAT SS
Size	Number		Revision
A4	15		v4.2
Date:	2019-09-30	Sheet 15	of 20
File:	C:\Users\..\Heater Control.SchDoc	Drawn By:	Lorna Lan



Title	Heater Control.SchDoc		UTAT SS
Size	Number		Revision
A4	15		v4.2
Date:	2019-09-30	Sheet 15	of 20
File:	C:\Users\..\Heater Control.SchDoc	Drawn By:	Lorna Lan

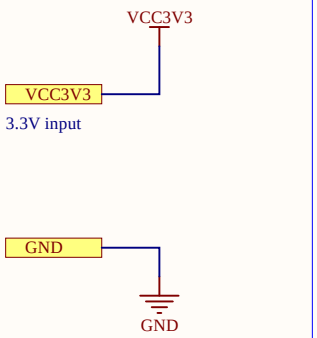


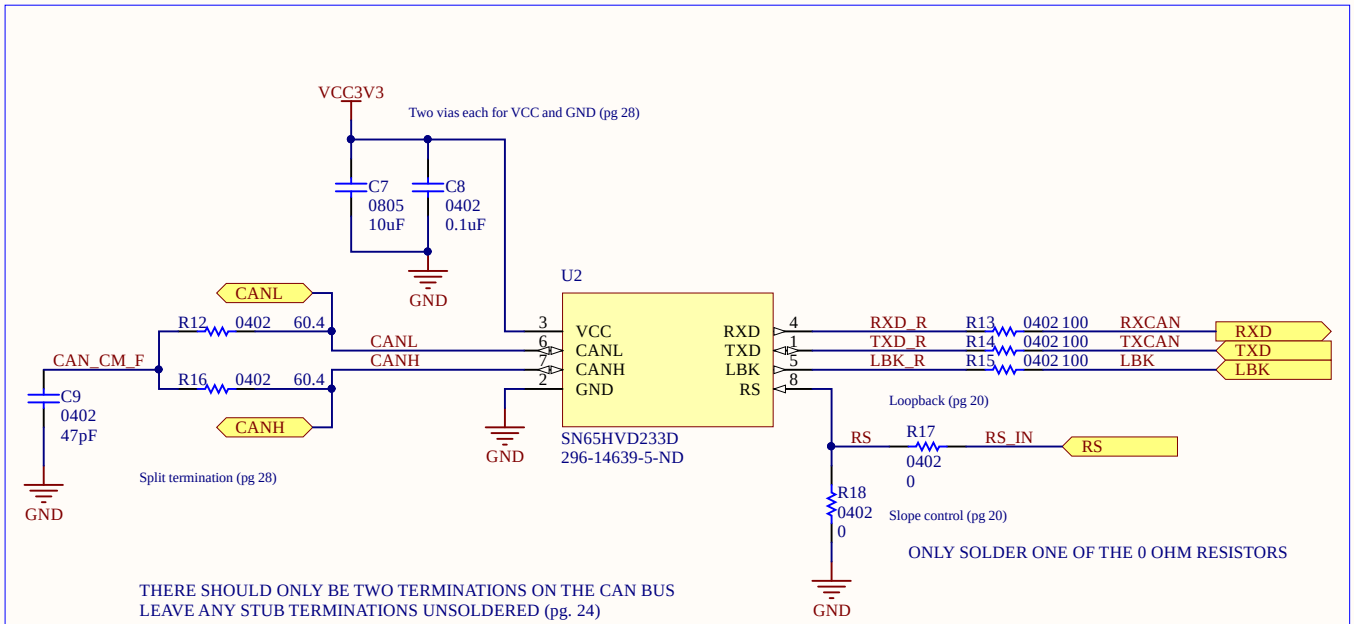
Title	Heater Control.SchDoc		UTAT SS
Size	A4	Number	15
			Revision v4.2
Date:	2019-09-30	Sheet 15	of 20
File:	C:\Users\..\Heater Control.SchDoc	Drawn By:	Lorna Lan



Title	Heater Control.SchDoc	UTAT SS
Size: A4	Number: 15	Revision: v4.2
Date: 2019-09-30	Sheet 15 of 20	
File: C:\Users\..\Heater Control.SchDoc	Drawn By: Lorna Lan	

POWER INPUT





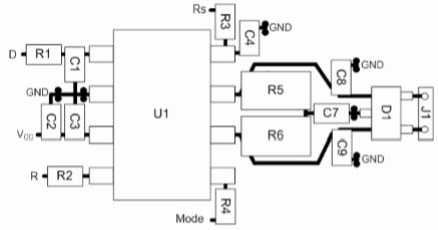


Figure 41. Layout Example Schematic

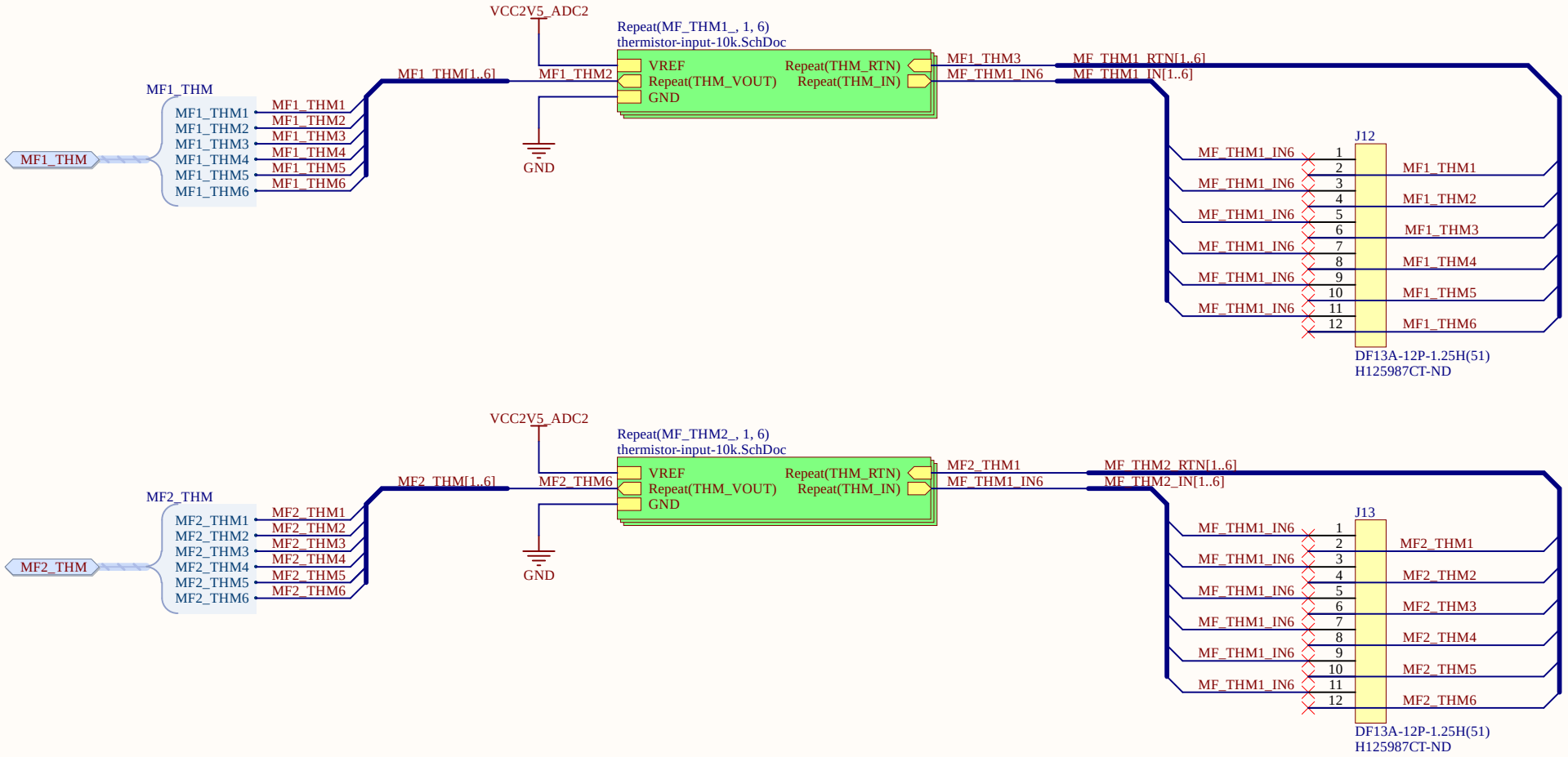
See pg. 28 of the datasheet for layout guidelines

This schematic implements the SN65HVD233 CAN transciever with loopback control and two options for slope control.

A 0 Ohm resistor can be soldered to GND to permanently put the device in high speed mode (20 V / us slew), or a 0 Ohm resistor can be soldered to the RS port to control the device via an external microcontroller. Connecting the RS pin to a microcontroller allows the device to be put into low-power mode by setting the RS pin high.

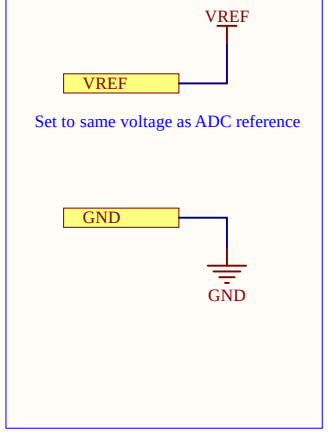
- Device is meant to be used in a 3.3 V system
- 100 Ohm current limiting resistors placed on the digital lines to minimize digital noise to the device
- Only two CAN transcievers on the bus should have 120 ohm terminations. Other devices should be placed on 'stub' networks where the terminations are left unsoldered

Title	can-SN65HVD233.SchDoc	UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-30	Sheet 16 of 20
File:	C:\Users\..\can-SN65HVD233.SchDoc	Drawn By: Dylan Vogel

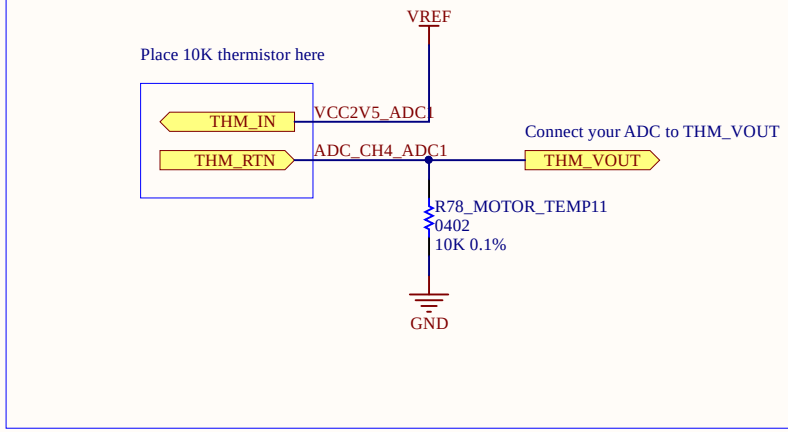


Title	MF Thermistors.SchDoc	UTAT SS
Size: A4	Number: 17	Revision: v4.1
Date: 2019-09-30		Sheet 17 of 20
File: C:\Users\..\MF Thermistors.SchDoc		Drawn By: Lorna Lan, Dylan Vogel

POWER INPUTS

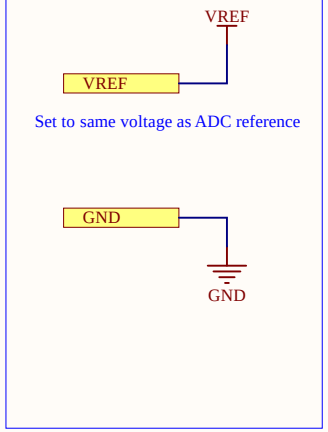


THERMISTOR

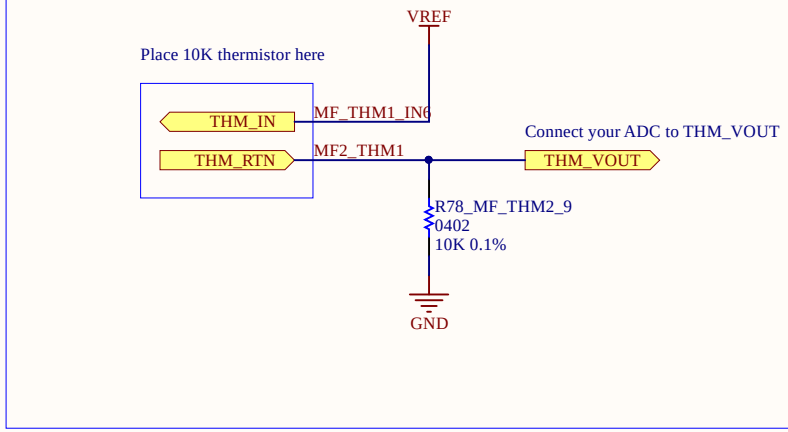


Title	thermistor-input-10k.SchDoc		UTAT SS
Size	Number		Revision
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS

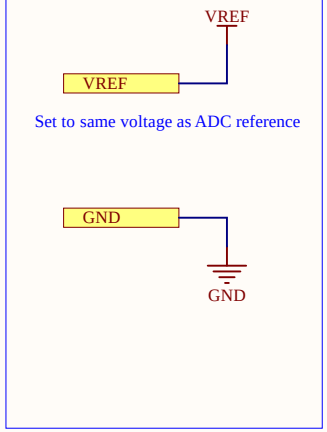


THERMISTOR



Title	thermistor-input-10k.SchDoc		UTAT SS
Size	Number		Revision
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS



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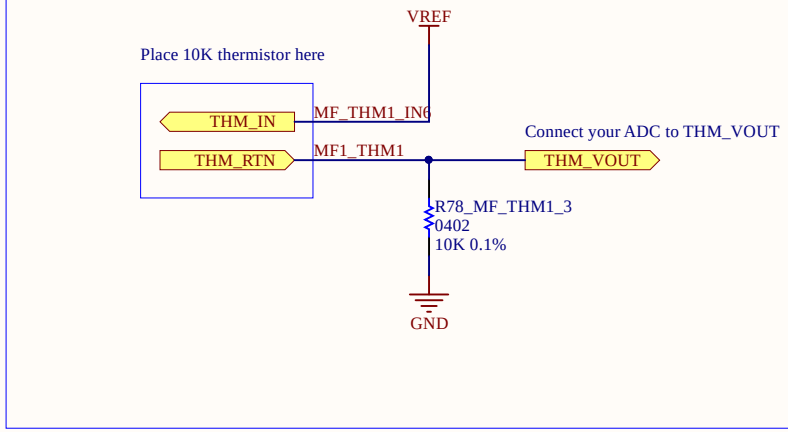
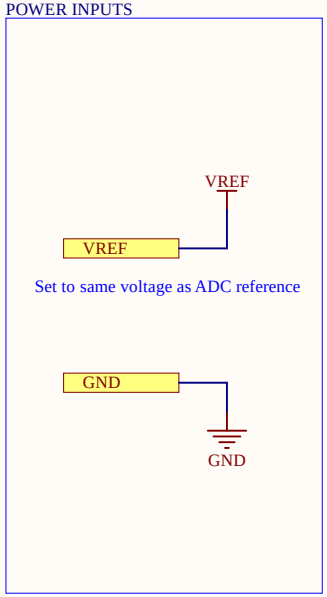


Title	thermistor-input-10k.SchDoc		UTAT SS
Size	Number		Revision
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS



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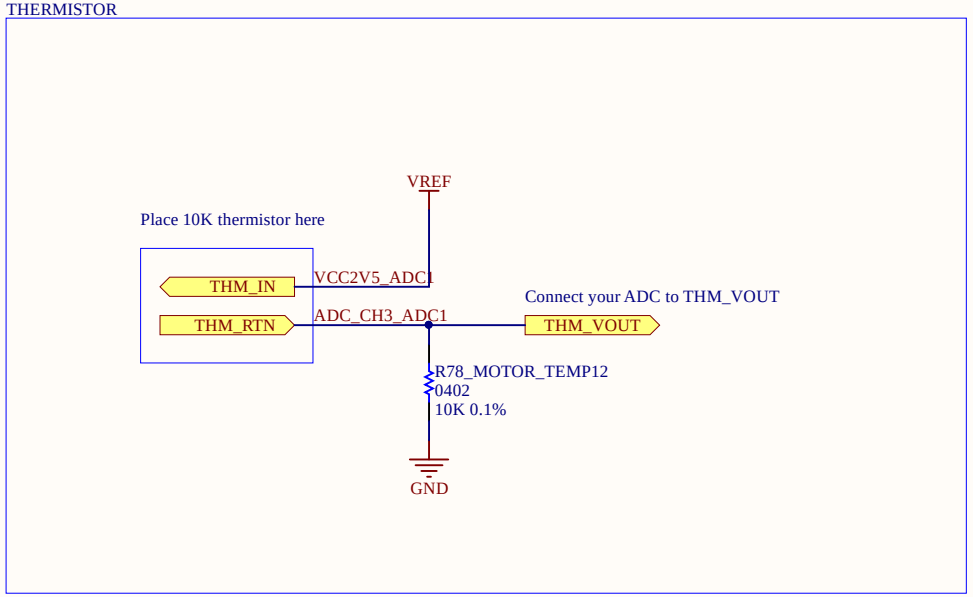
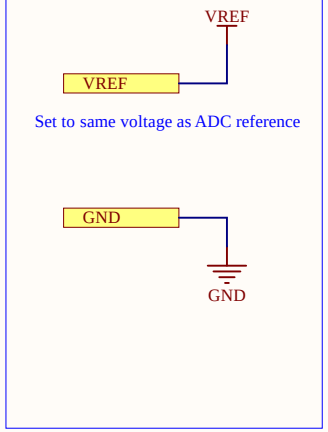


Title	thermistor-input-10k.SchDoc		UTAT SS
Size	Number		Revision
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS



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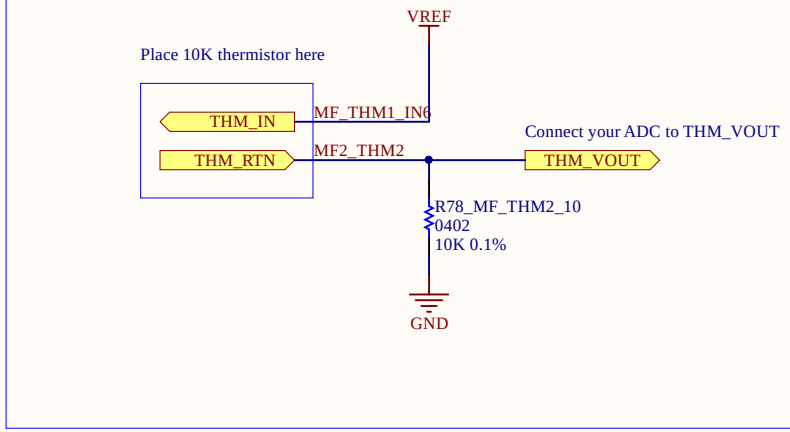
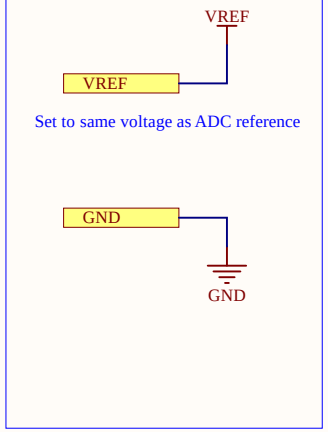
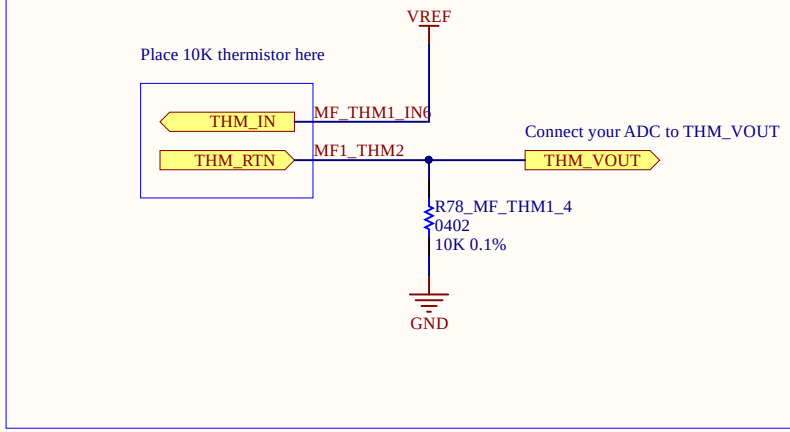


Title	thermistor-input-10k.SchDoc		UTAT SS
Size	Number		Revision
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS

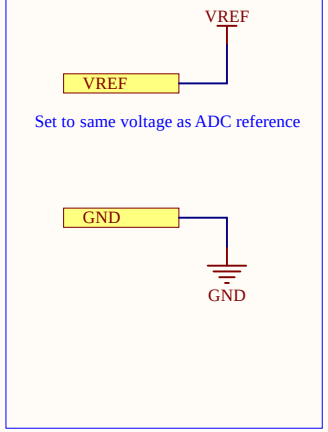


THERMISTOR

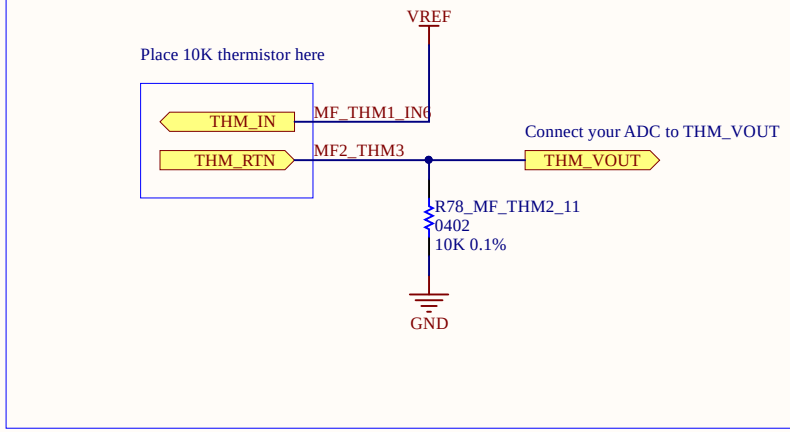


Title	thermistor-input-10k.SchDoc		UTAT SS
Size	Number		Revision
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS

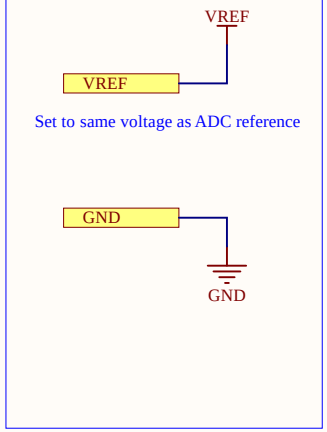


THERMISTOR



Title	thermistor-input-10k.SchDoc		UTAT SS
Size	Number		Revision
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS



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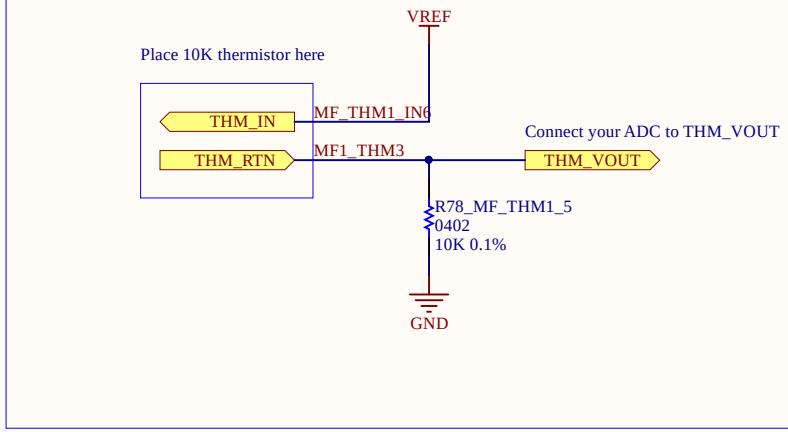
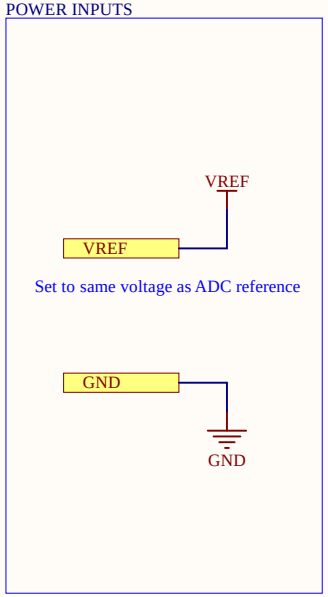


Title	thermistor-input-10k.SchDoc		UTAT SS
Size	Number		Revision
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS



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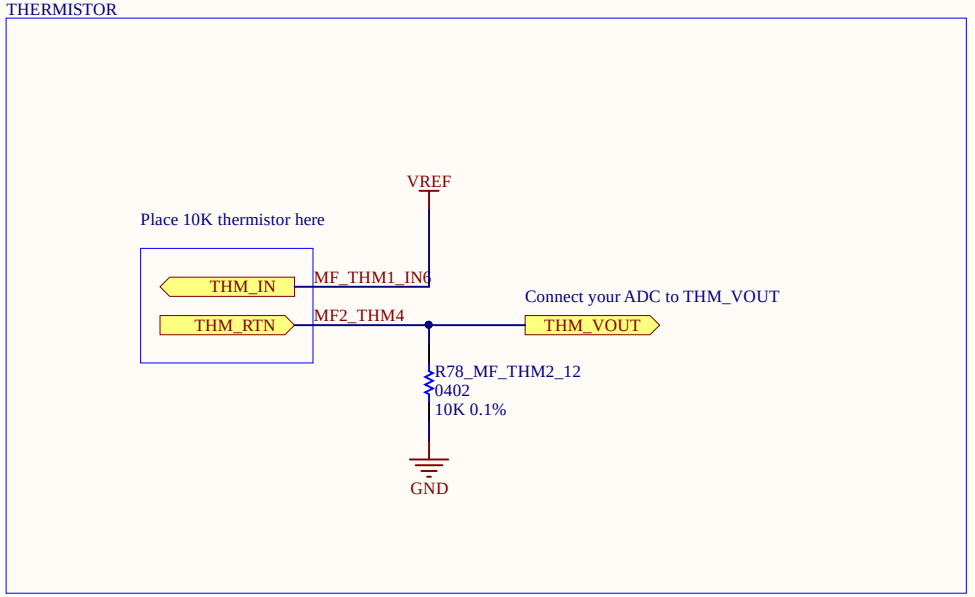
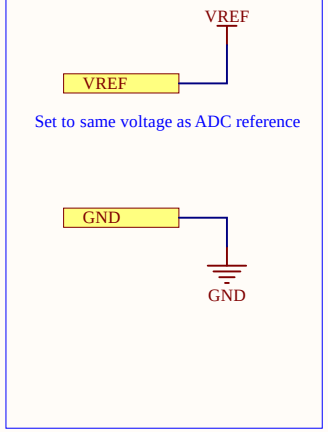


Title	thermistor-input-10k.SchDoc		UTAT SS
Size	Number		Revision
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS



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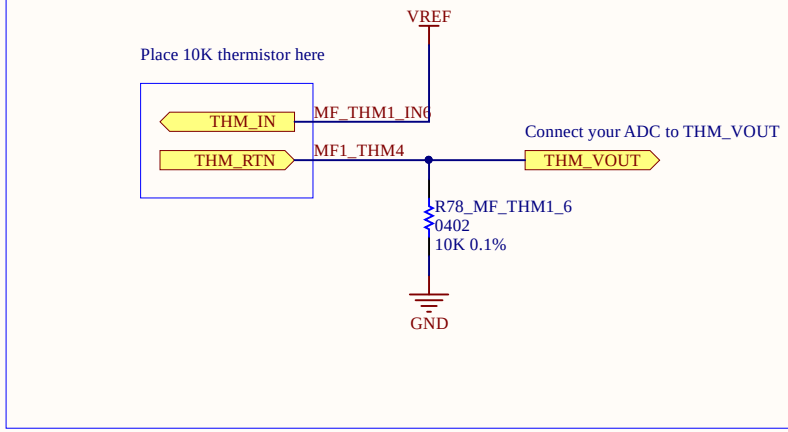
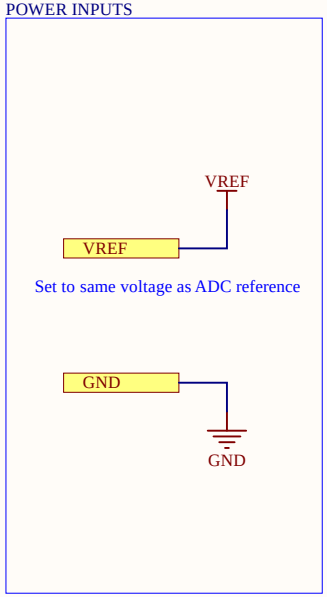


Title	thermistor-input-10k.SchDoc		UTAT SS
Size	Number		Revision
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS



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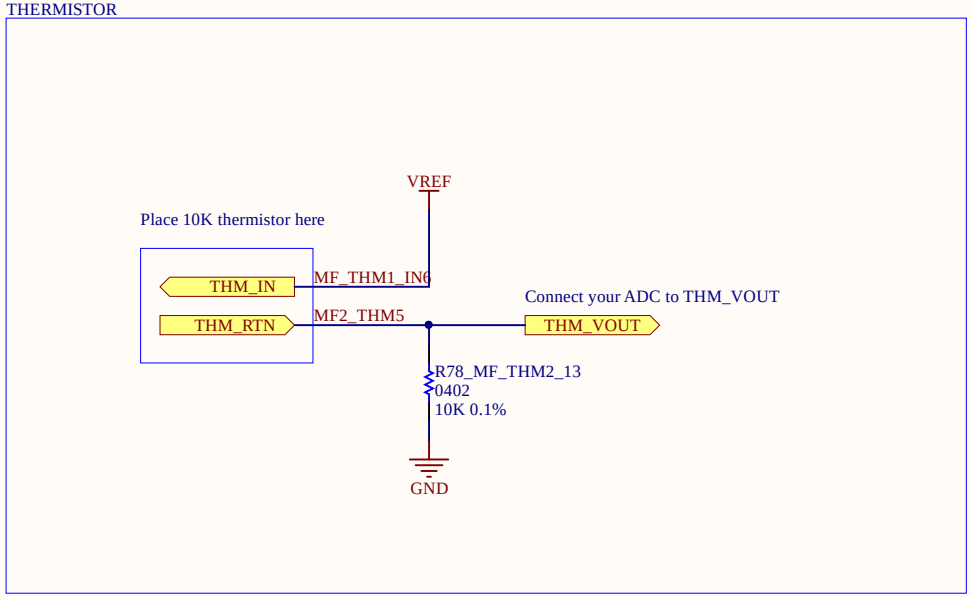

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Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

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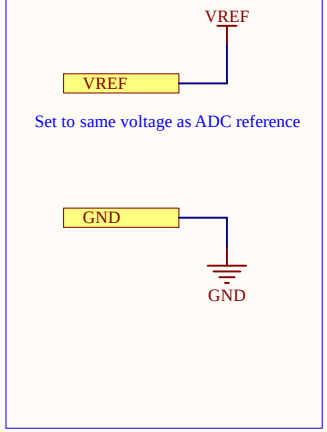

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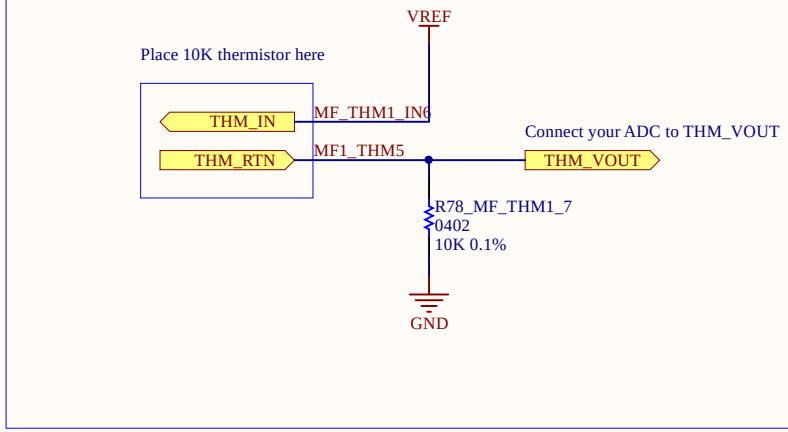

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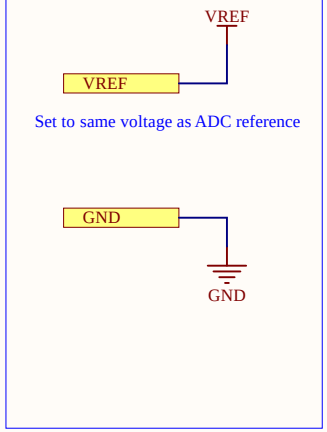
A4	PCBS-COMMON		1.2
Date:	2019-09-30	Sheet 18	of 20
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS



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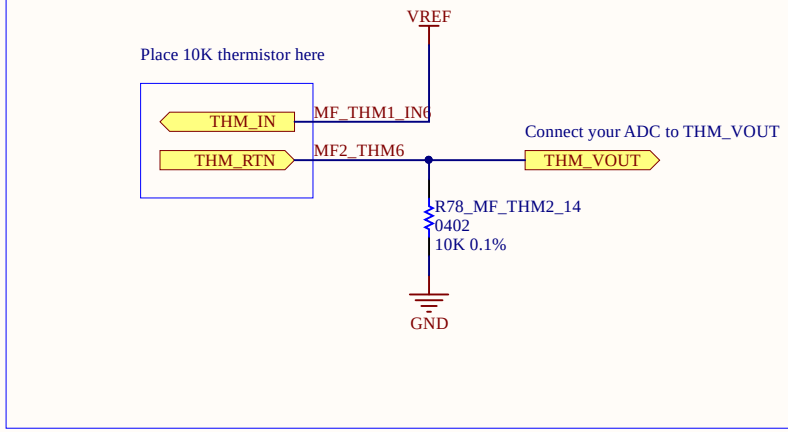

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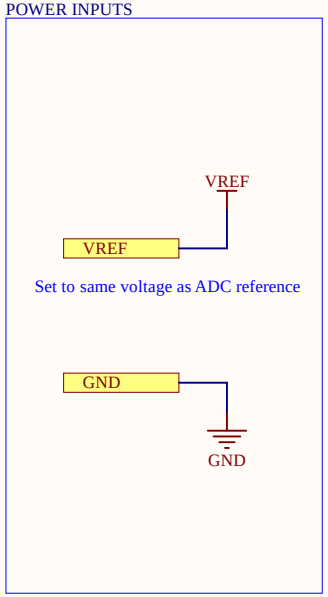
File:	C:\Users\..\thermistor-input-10k.SchDoc	Drawn By:	B. Almeida, D. Vogel

POWER INPUTS



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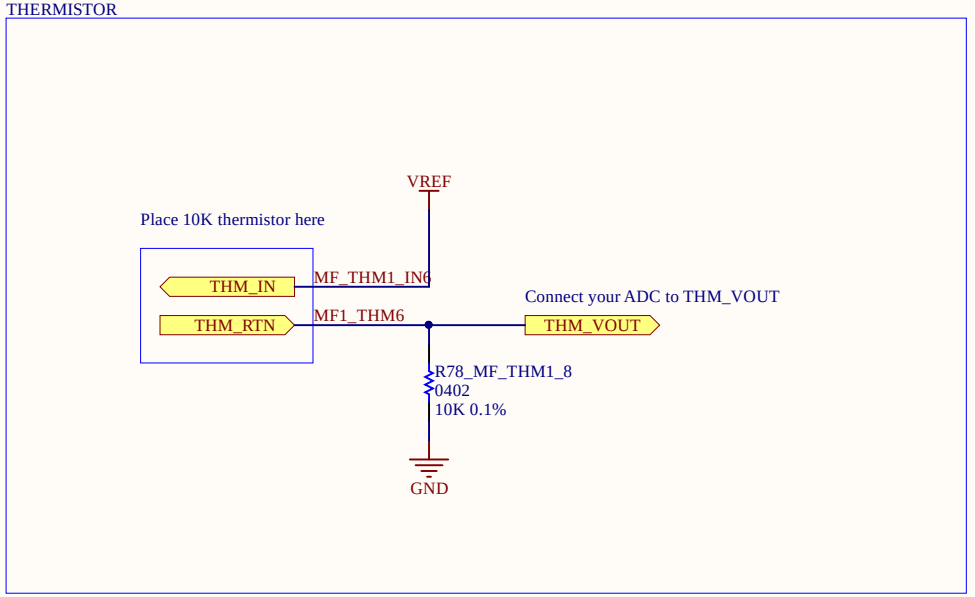

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