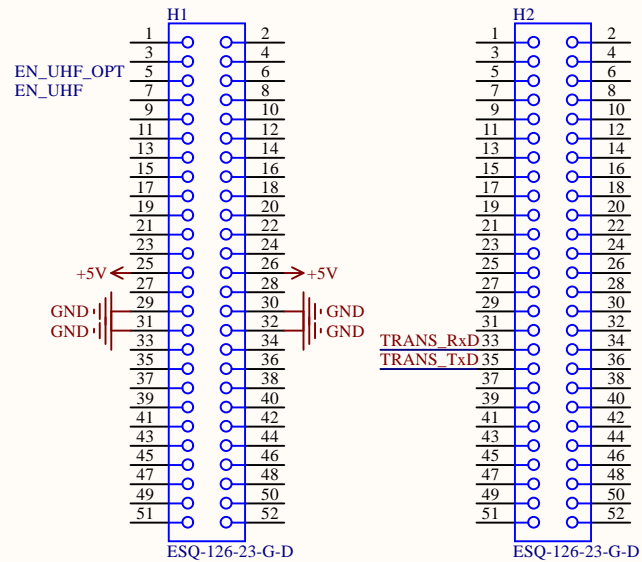
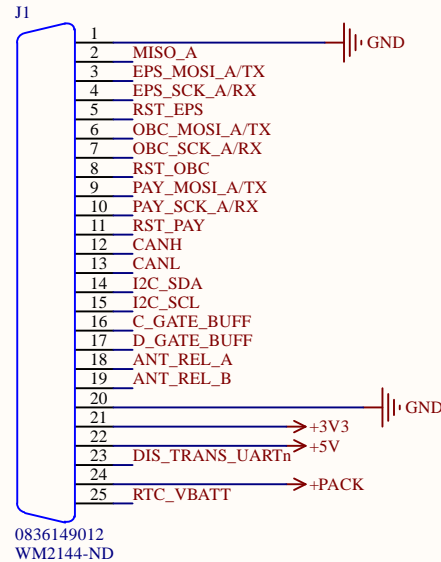


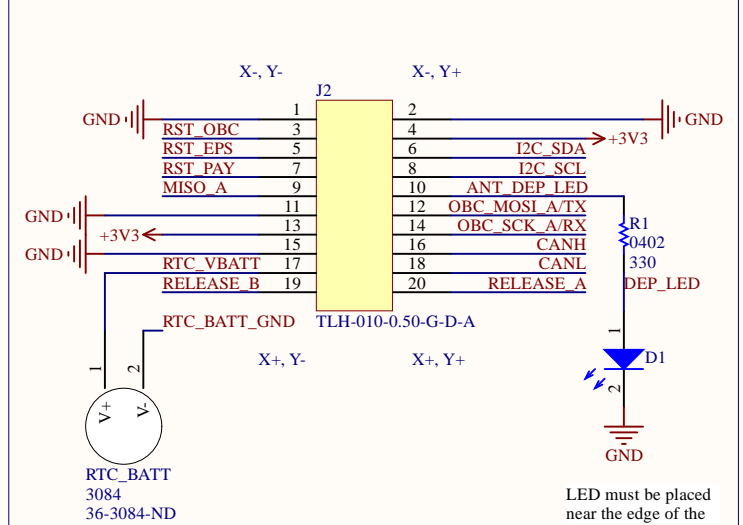
Transceiver PC104 Connectors



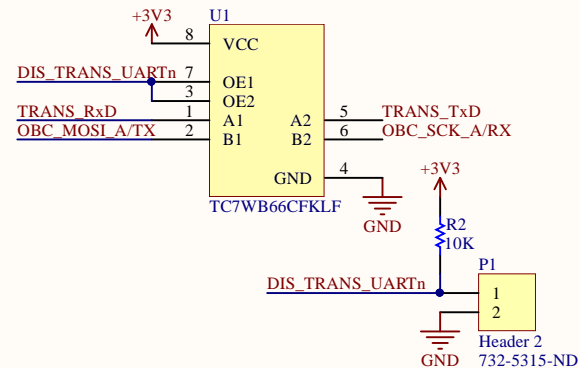
Systems PCB DSUB Connector



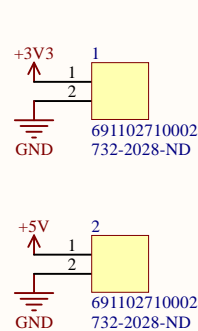
OBC Butterfly Connector



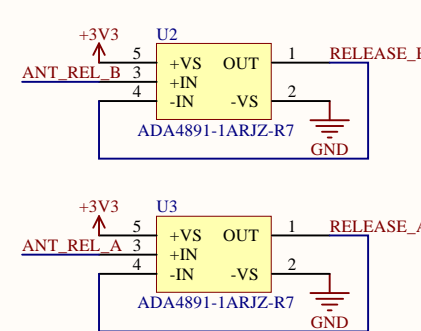
TRANSCEIVER/UART PROG



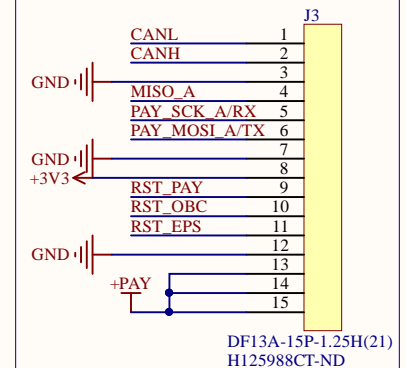
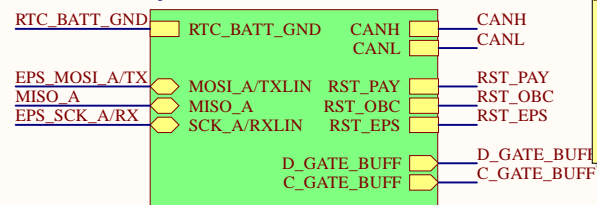
Converter Output Screw Terminals



Release Pin Buffers

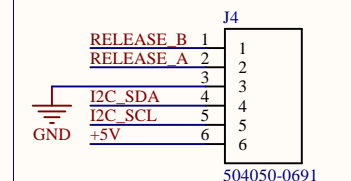


Payload Connector

MAIN  
eps.SchDoc

Questions:  
- should we choose a smaller RTC battery to allow for more clearance from the OBC mounting connections?

Antenna Connector



Title		UTAT SS	
Top Level		Revision	
Size	Number	1.0	
A4	1		
Date:	2019-07-27	Sheet	1 of 17
File:	C:\Users\...\main.SchDoc	Drawn By:	J. Reimer T. Yeung M. Au

A

A

B

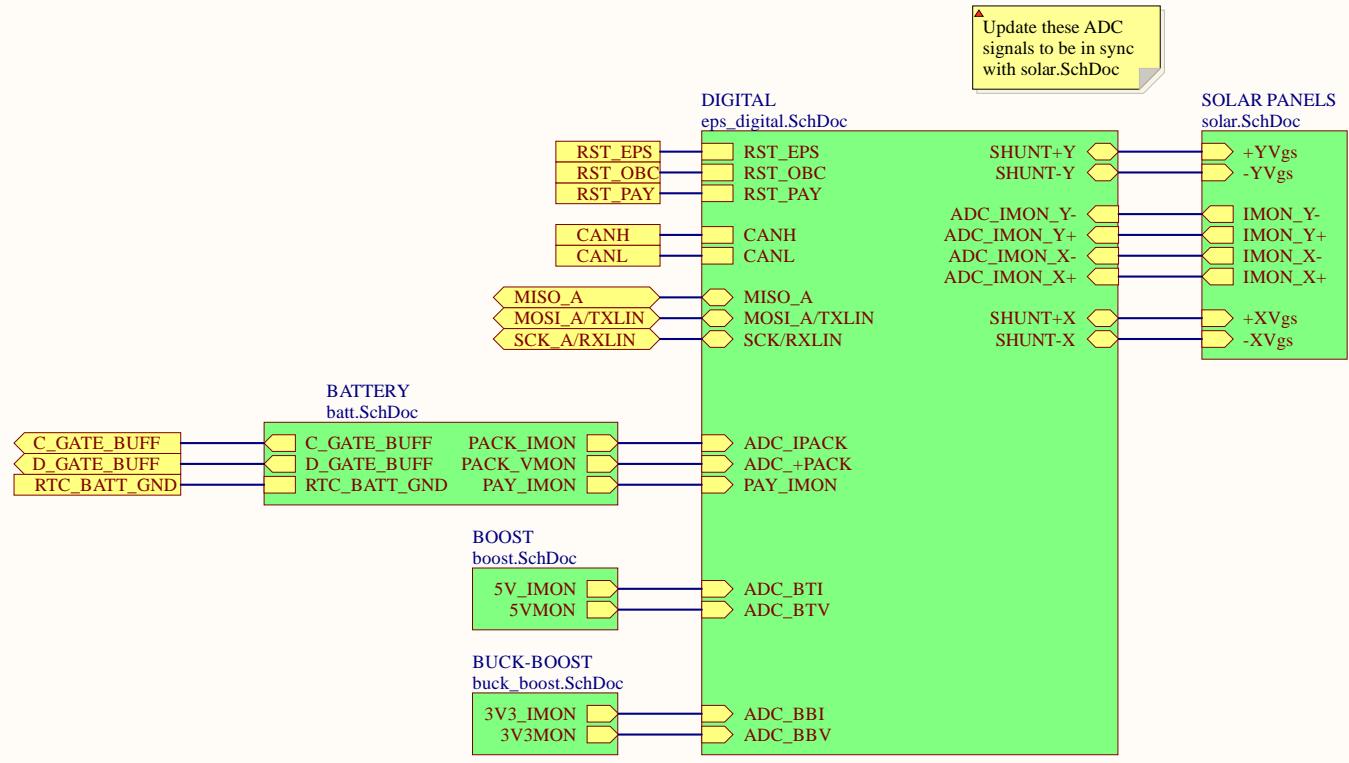
B

C

C

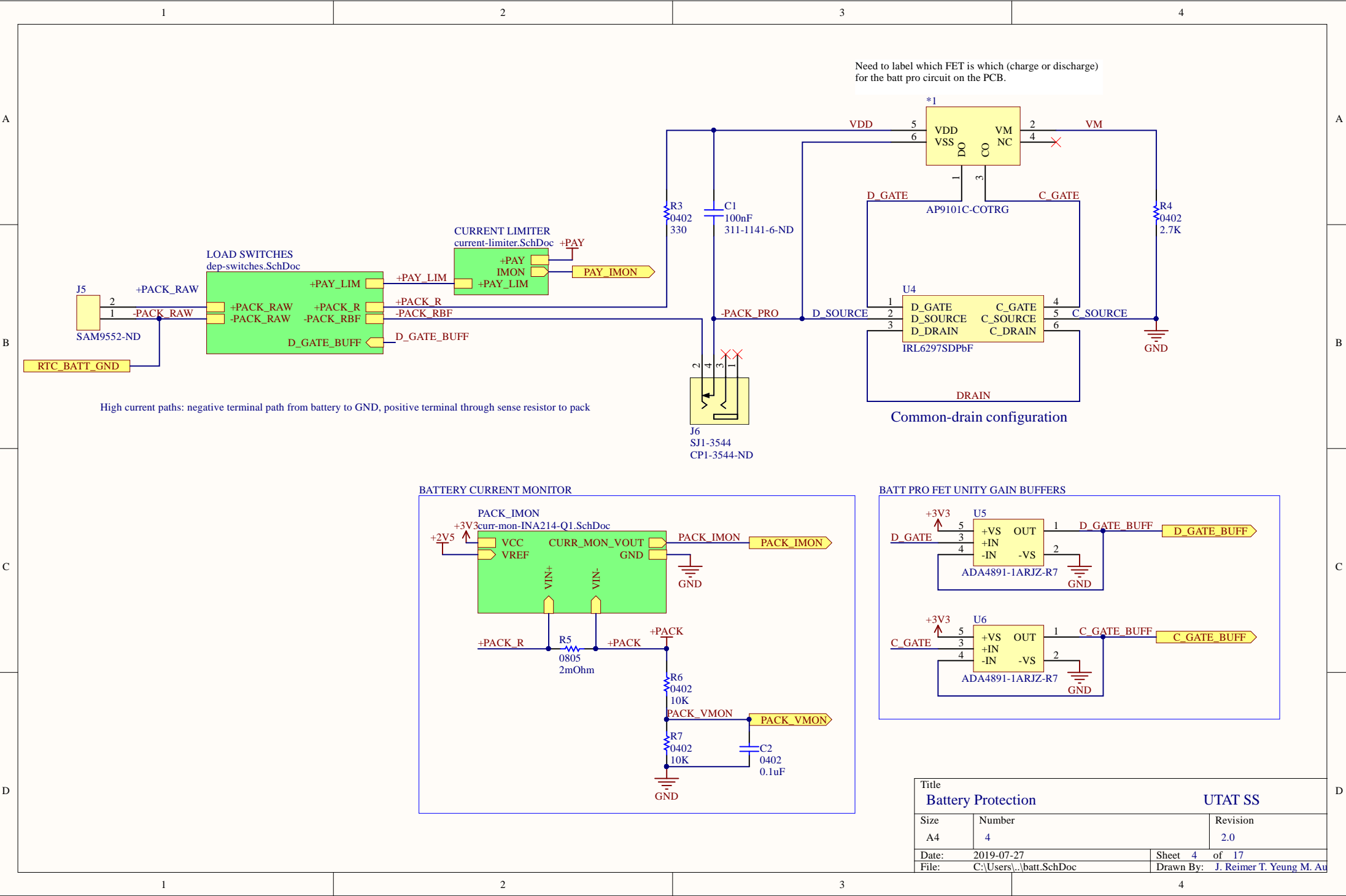
D

D

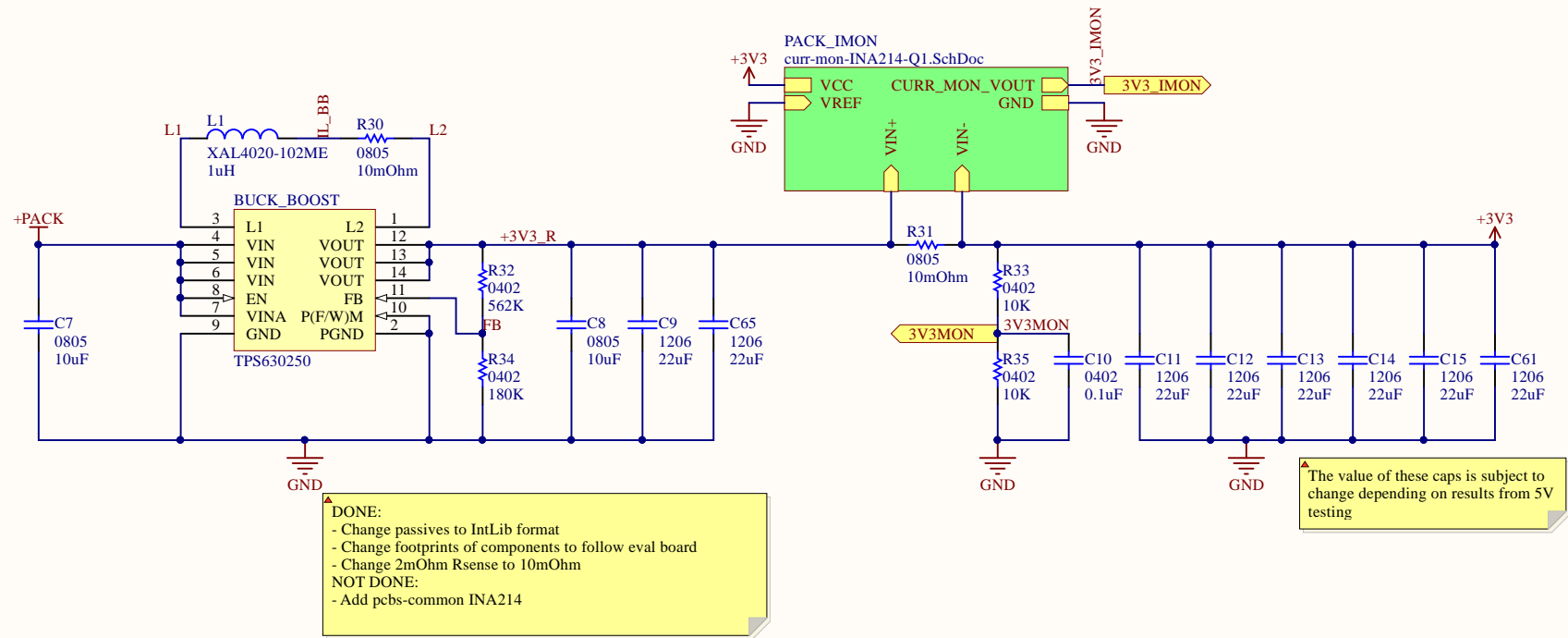


Title		UTAT SS	
Power Top Level			
Size	Number	Revision	
A	2	1.0	
Date:	2019-07-27	Sheet	2 of 17
File:	C:\Users\...\eps.SchDoc	Drawn By:	J. Reimer T. Yeung M. Au

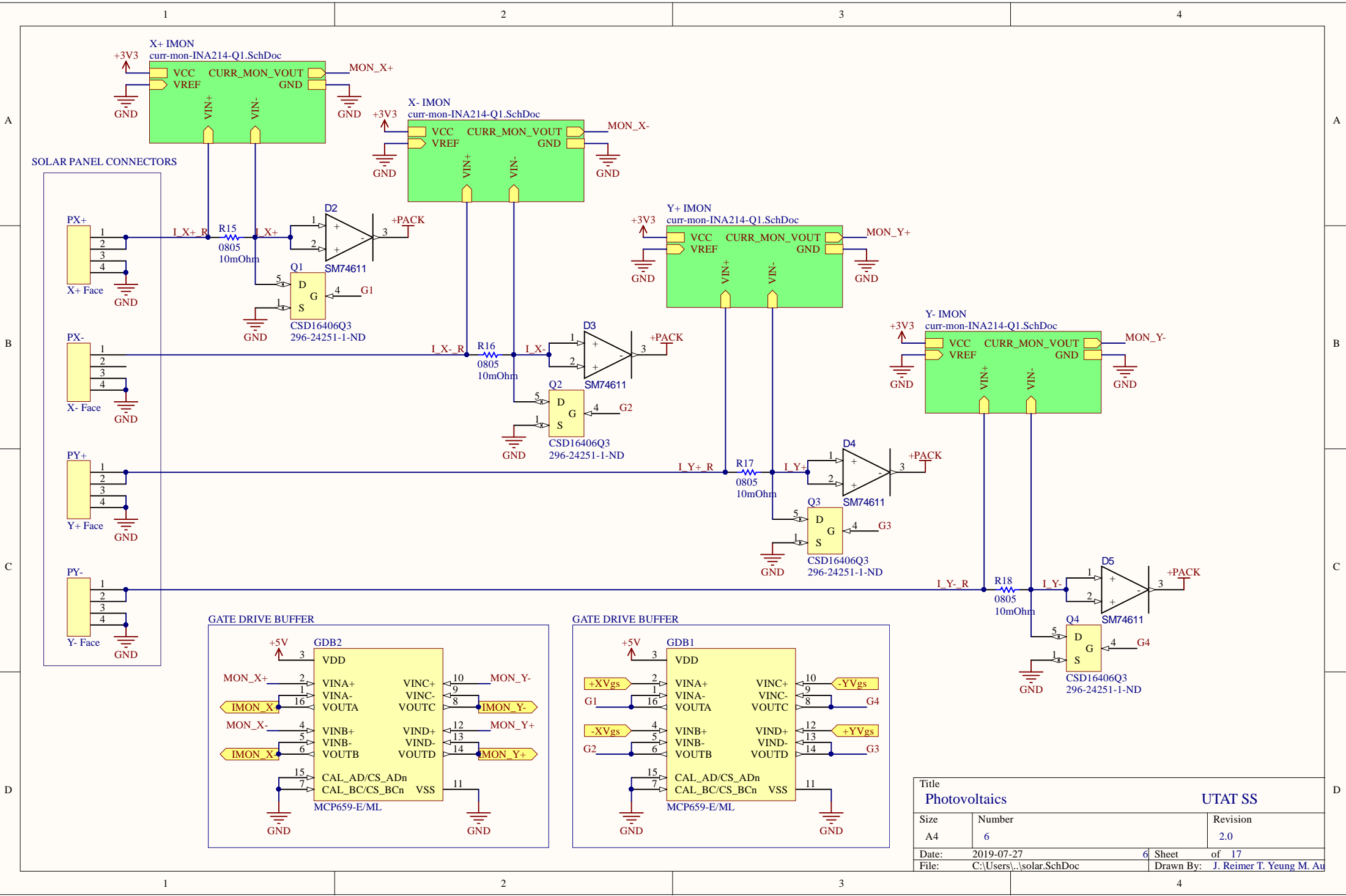




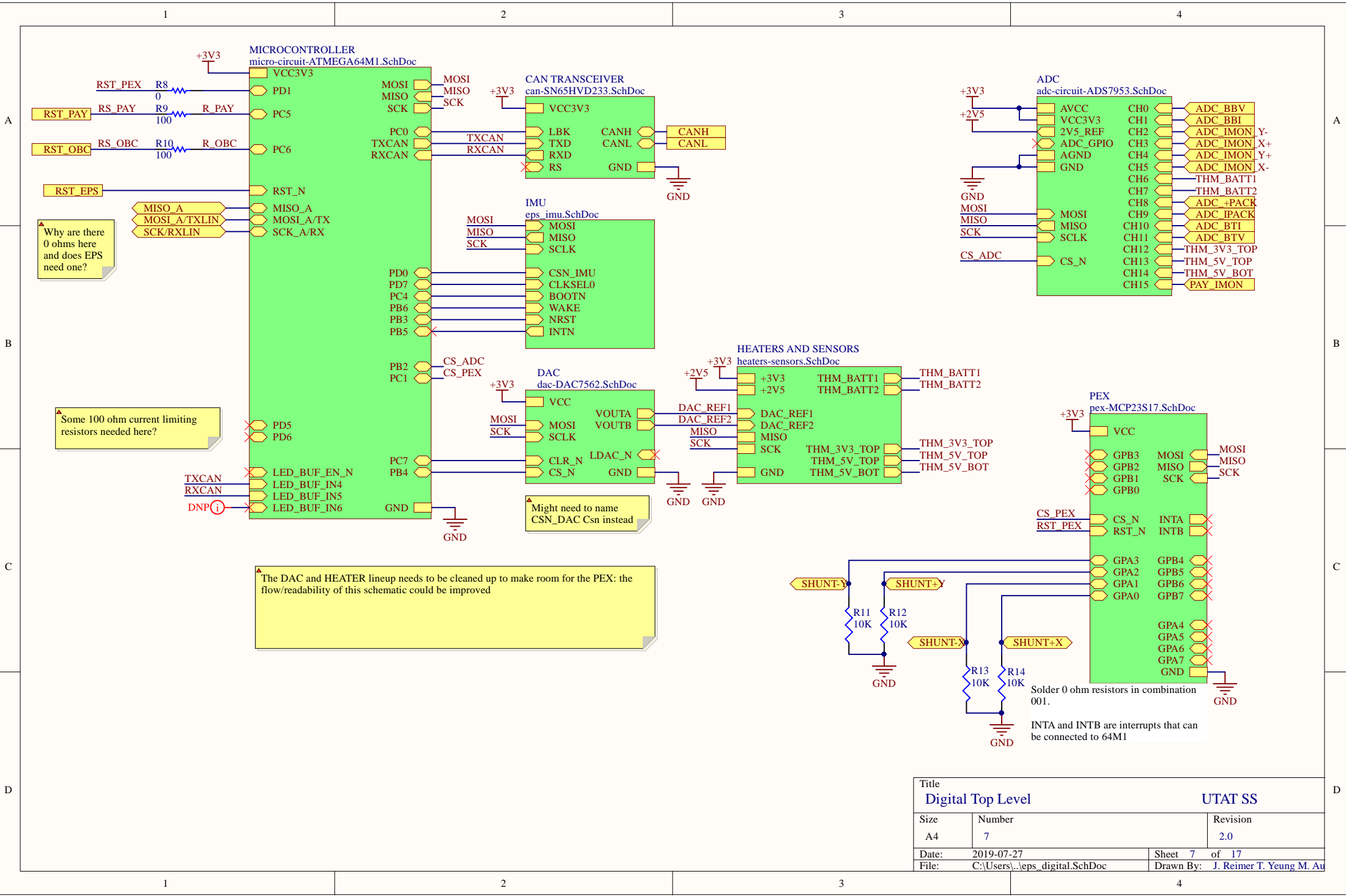
Questions:  
- 2mOhm resistors for current sensing and for inductor current measuring; would we possibly need a larger resistor for the inductor current sensing (to be able to probe the voltage across it)?  
- input filtering using capacitors: is the 10uF enough?



Title			UTAT SS
Buck-Boost			
Size	Number	Revision	
A4	5	2.0	
Date:	2019-07-27		Sheet 5 of 17
File:	C:\Users\...\buck_boost.SchDoc		Drawn By: J. Reimer T. Yeung M. Au



Title		UTAT SS	
Photovoltaics			
Size	Number	Revision	
A4	6	2.0	
Date:	2019-07-27	6	Sheet of 17
File:	C:\Users\...\solar.SchDoc	Drawn By:	J. Reimer T. Yeung M. Au

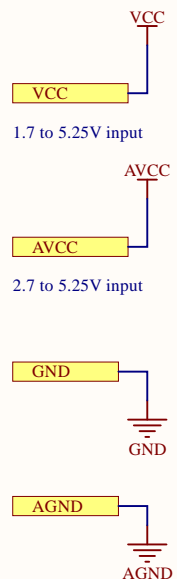


Title		UTAT SS	
Digital Top Level			
Size	Number	Revision	
A4	7	2.0	
Date:	2019-07-27	Sheet 7	of 17
File:	C:\Users\...\eps_digital.SchDoc	Drawn By:	J. Reimer T. Yeung M. Au

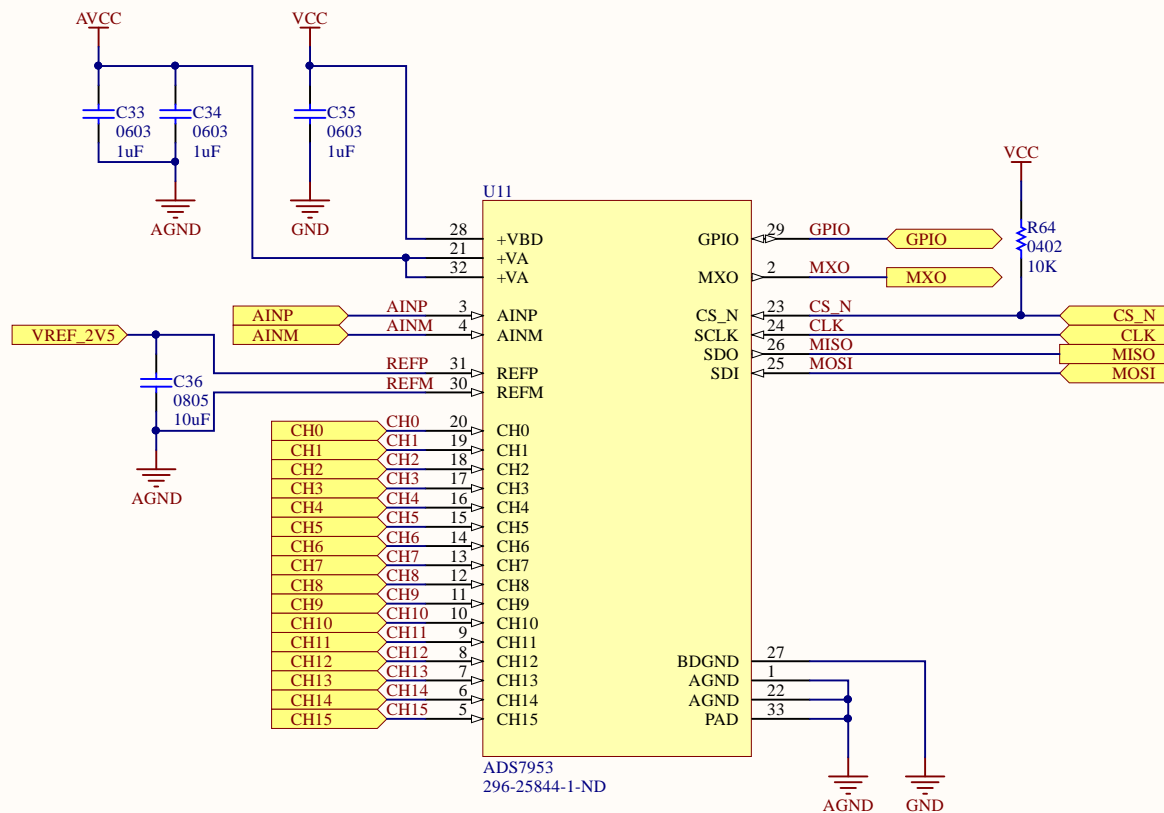




POWER INPUTS  
AVCC >= VCC (pg 51)



See pg 53, each +VA pin should have it's own 1uF

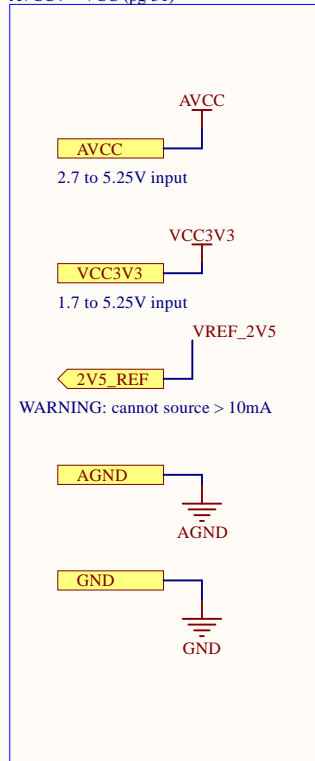


16 CHANNEL ADC

Title adc-ADS7953.SchDoc			
Size A4	Number PCBS-COMMON	Revision 1.1	
Date: 2019-07-27	Sheet * of *		
File: C:\Users\...\adc-ADS7953.SchDoc	Drawn By: Dylan Vogel		

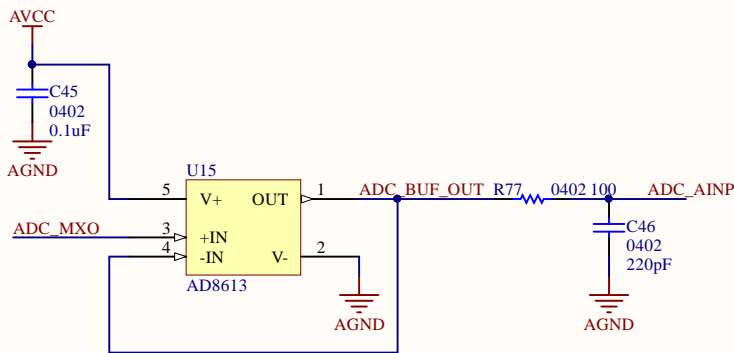
# POWER PORTS

## AVCC >= VCC (pg 51)



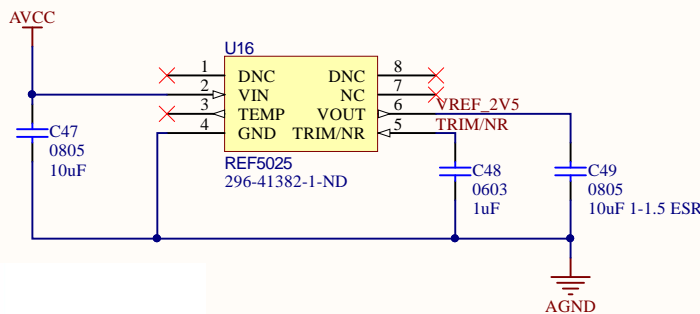
# ADC INPUT BUFFER

See pg. 50 for discussion of unity buffer design procedure

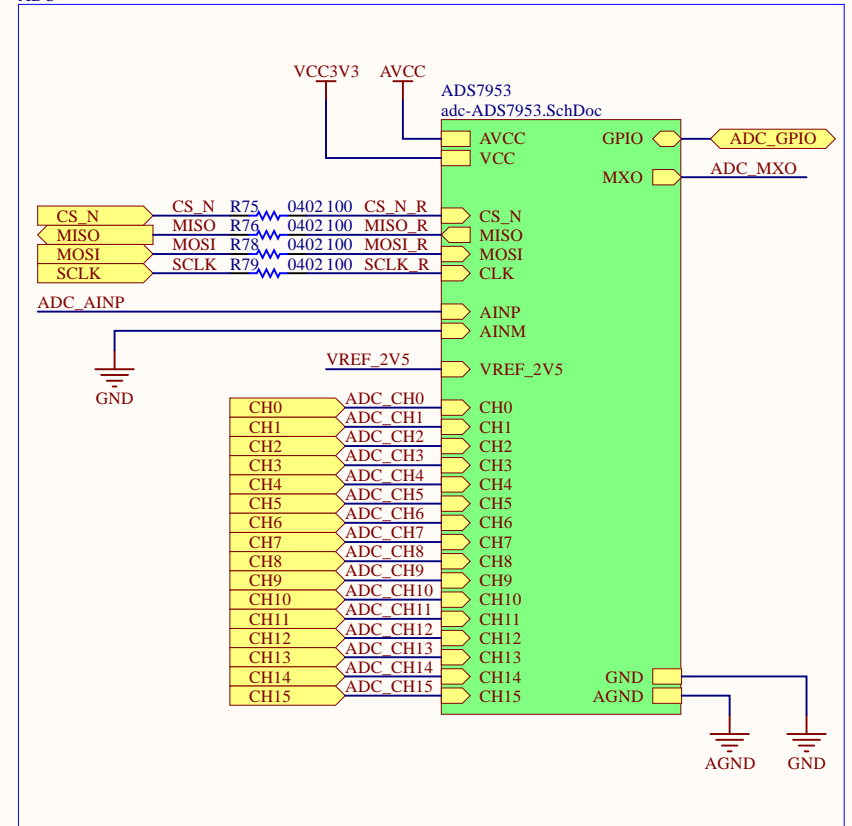


# 2V5 REFERENCE

Output cap should have ESR from 1 - 1.5 ohm (see pg. 21)



# ADC



This schematic implements the ADS7953 analog-to-digital converter with a 2.5V reference and a unity-gain buffer on the output of the internal multiplexer.

- Recommended input impedance should be < 1K. Higher source impedances possible with slower sampling.
- Breaks out 2V5 for use as reference outside the circuit
- All necessary bypassing and pull-ups implemented in the ADS7953 schematic
- In most low-performance applications, AVCC and VCC can be tied together
- In the layout, the pins tied to AGND should be put on a local GND pour and then tied to the global ground plane with low-impedance.
- 100 ohm resistors on the SPI input help to isolate the ADC from digital noise

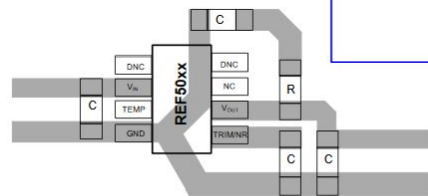


Figure 44. Layout Example

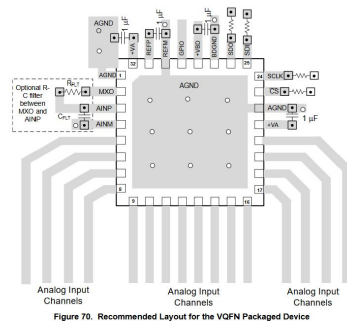


Figure 70. Recommended Layout for the VQFN Packaged Device

Title			
adc-circuit-ADS7953.SchDoc			
Size	Number	Revision	
A4	PCBS-COMMON	1.1	
Date:	2019-07-27	Sheet *	of *
File:	C:\Users\...\adc-circuit-ADS7953.SchDoc Drawn By: Dylan Vogel		

# POWER INPUT

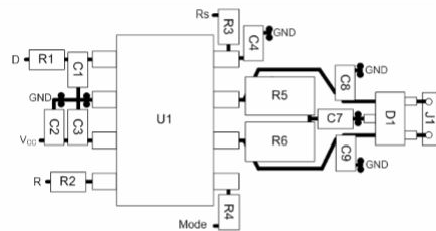
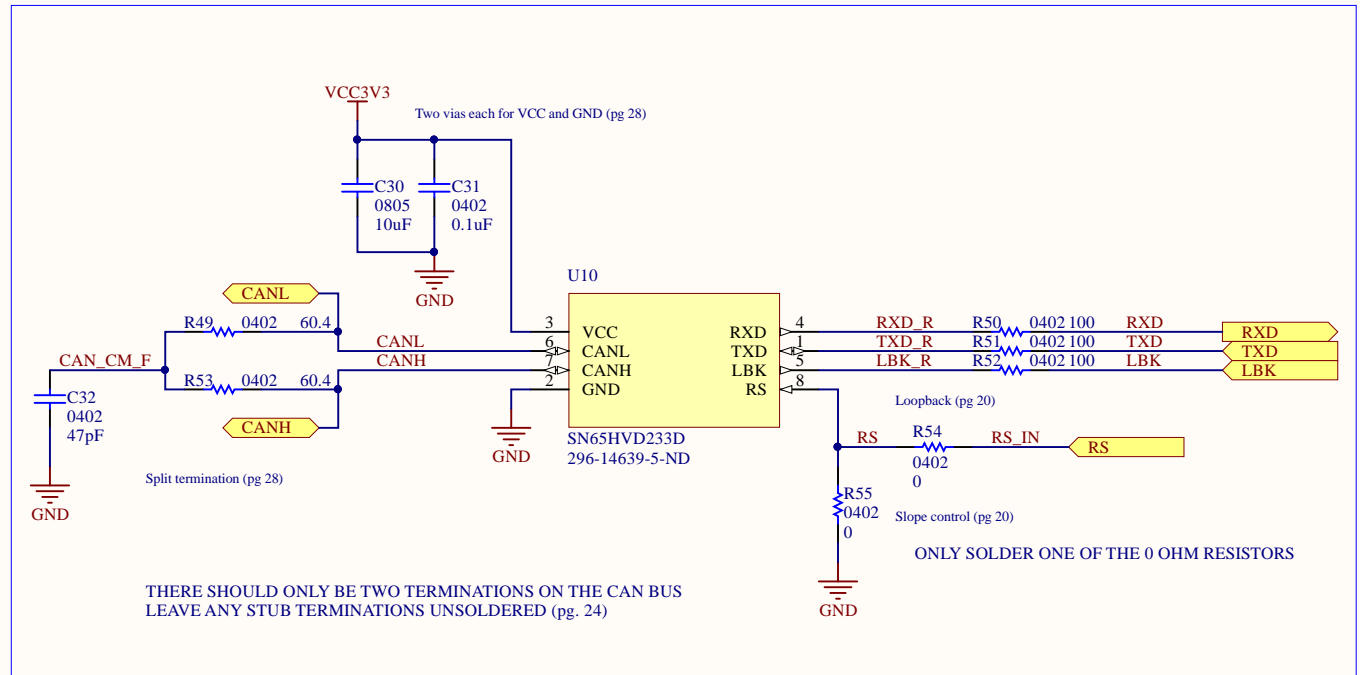
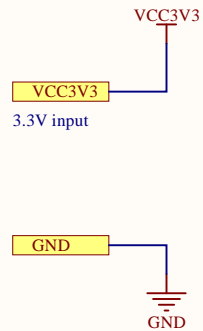


Figure 41. Layout Example Schematic

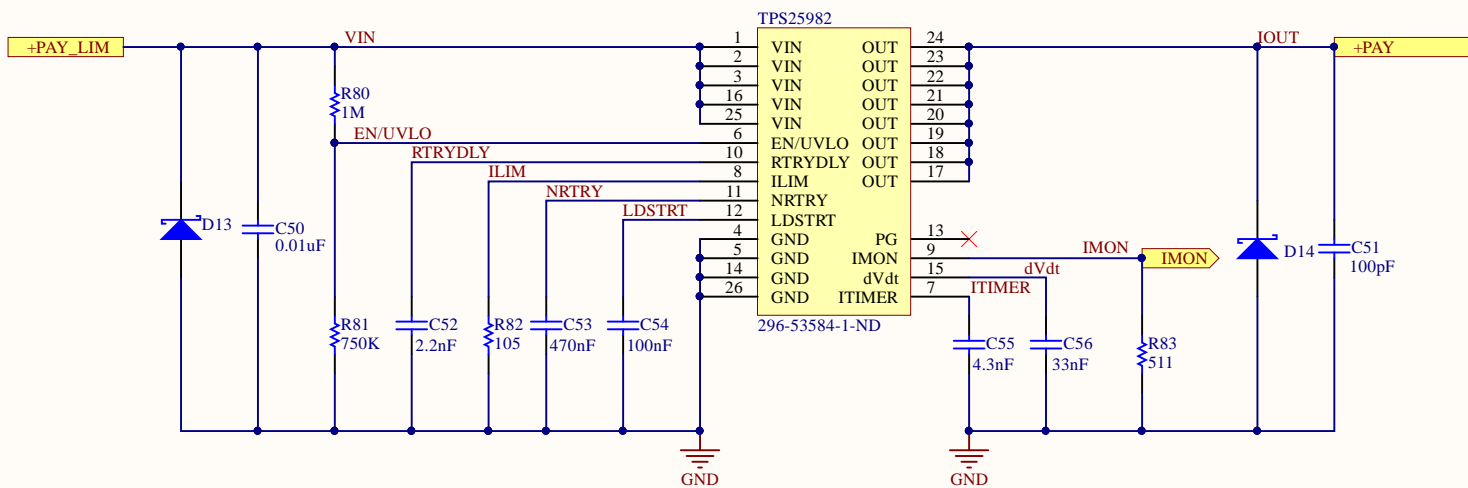
See pg. 28 of the datasheet for layout guidelines

This schematic implements the SN65HVD233 CAN transceiver with loopback control and two options for slope control.

A 0 Ohm resistor can be soldered to GND to permanently put the device in high speed mode (20 V / us slew), or a 0 Ohm resistor can be soldered to the RS port to control the device via an external microcontroller. Connecting the RS pin to a microcontroller allows the device to be put into low-power mode by setting the RS pin high.

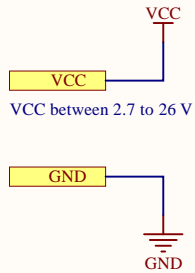
- Device is meant to be used in a 3.3 V system
- 100 Ohm current limiting resistors placed on the digital lines to minimize digital noise to the device
- Only two CAN transceivers on the bus should have 120 ohm terminations. Other devices should be placed on 'stub' networks where the terminations are left unsoldered

Title			
can-SN65HVD233.SchDoc			
Size	Number	Revision	
A4	PCBS-COMMON	1.2	
Date:	2019-07-27	Sheet *	of *
File:	C:\Users\...\can-SN65HVD233.SchDoc	Drawn By:	Dylan Vogel

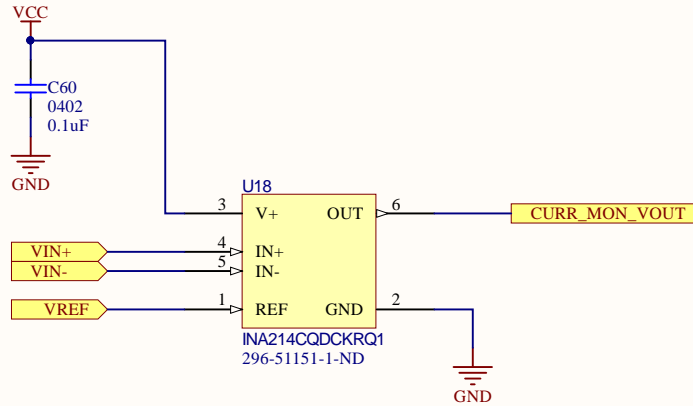


Title		UTAT-SS	
e-Fuse			
Size	Number	Revision	
A4		Text	
Date:	2019-07-27	Sheet	of
File:	C:\Users\...\current-limiter.SchDoc	Drawn By:	J. Riemer, T. Yeung, M. Hirole

POWER INPUTS



CURRENT MONITOR

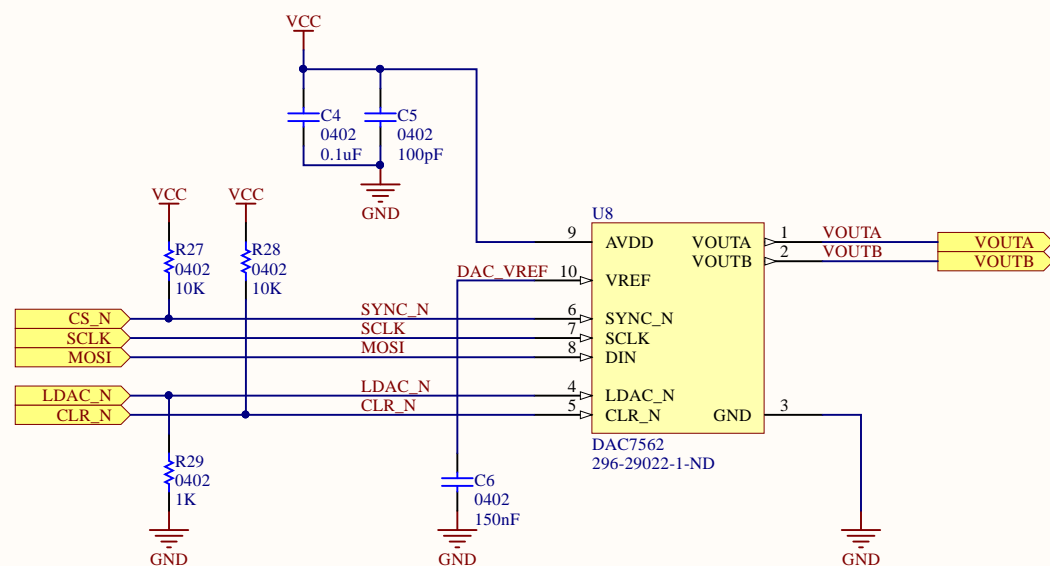
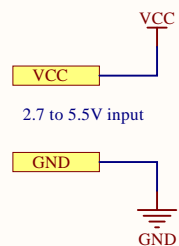


This schematic implements the INA214-Q1 automotive grade, voltage output, high- or low-side, bidirectional, zero-drift current shunt monitor

Application Information:

- This amplifier has an internal gain of 100x
- Place a small value current sense resistor (1 -> 10 mOhm) in series with the current you're trying to monitor. Connect VIN+ of the current monitor to the positive terminal of the resistor, and VIN- to the negative terminal.
- Assume the worst-case input voltage offset is 100uV. This allows you to calculate your expected measurement error. No strict guideline on what this should be, but if your full-scale current generates a voltage of 10mV across your sen resistor, that's 1% error. Typical error will be lower than this.
- For unidirectional operation (current in one direction) connect VREF to GND
- For bidirectional operation, UTAT recommends connecting VREF to the stable 2.5V reference you probably already use for your ADC. Pop a 0.1uF on your VREF connection in that case.
- To calculate your current range for bidirectional, understand that forward current will cause VOUT to rise from 2.5 V up to VCC - 0.2 V. Reverse current will cause VOUT to drop from 2.5V to GND. Divide this voltage swing in each direction by  $(100 * R_{sense})$  to figure out your max current

Title			
curr-mon-INA214-Q1.SchDoc			
Size	Number		Revision
A4	PCBS-COMMON		1.0
Date:	2019-07-27	Sheet *	of *
File:	C:\Users\...\curr-mon-INA214-Q1.SchDoc Drawn By: J. Reimer, D. Vogel		



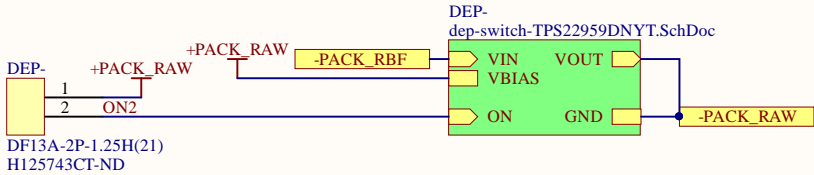
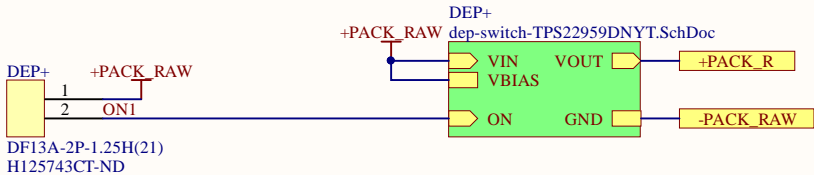
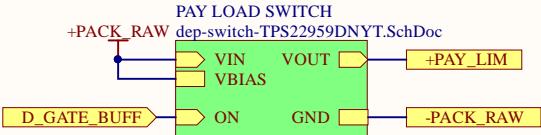
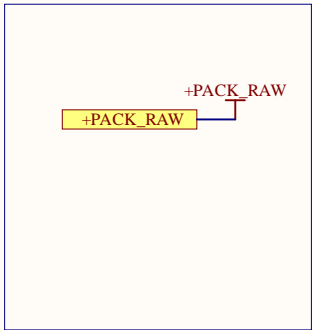
This schematic implements the DAC7562 16-bit digital-to-analog converter. The device has two configurable outputs, VOUTA and VOUTB, which can be digitally written through the 3-wire SPI interface. This particular device is set to zero scale (0V) both outputs upon power-on/reset. Toggling CLRN to LOW via an external GPIO will also zero both outputs.

The device is connected in synchronous mode, where LDAC\_N is connected to GND through a strong pull-down. This means that output VOUTA/VOUTB will be updated at the end of the SPI communication frame. The alternative would be to connect LDAC\_N to a microcontroller GPIO and toggle it low manually to set all outputs at the same time. This is referred to as asynchronous mode in the datasheet.

Title		
dac-DAC7562.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-07-27	Sheet * of *
File:	C:\Users\...\dac-DAC7562.SchDoc	Drawn By: Dylan Vogel

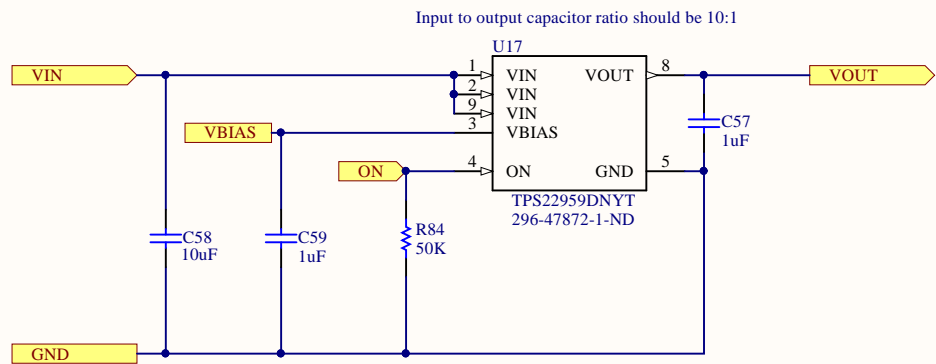
▲ Questions:

- I think these deployment switches are bidirectional: in the current setup, VIN and VOUT are configured in the direction of battery discharge. Is there a reason either of these should be switched around?
- Is there an optimal value for the pull-downs? I put them at 50K because they will have BATT voltage driving the load switches high for the entire satellite lifetime so increased it, but still pretty arbitrary at 50K



▲ TITLE BLOCK

Title		
Size	Number	Revision
A4		
Date:	2019-07-27	Sheet of
File:	C:\Users\...\dep-switches.SchDoc	Drawn By:

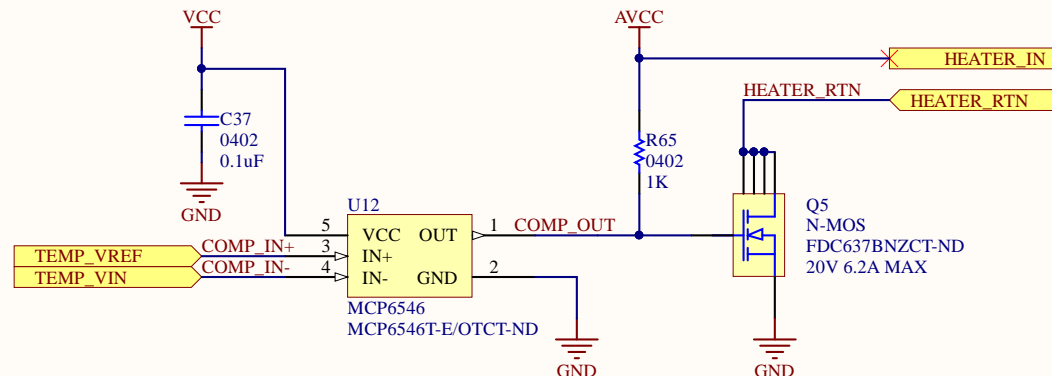
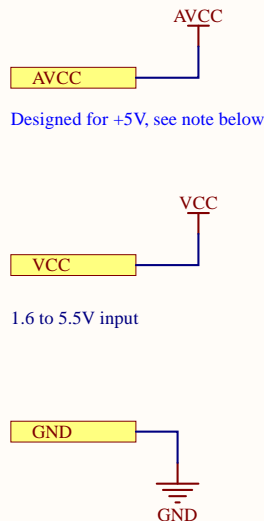


TITLE BLOCK

Title		UTAT-SS	
Deployment Load Switch		Revision	
Size		3.0	
A4		Number	
Date:		Sheet of	
2019-07-27		C:\Users\...\dep-switch-TPS22959DNYT.SchDoc	
File:		By: J. Riemer, T. Yeung, M. Hirole	

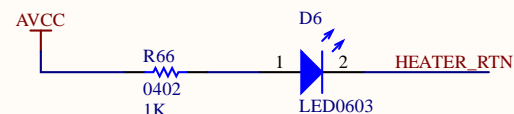


## POWER INPUTS



Non-Inverting Open Drain Comparator  
 IF  $IN+ > IN-$ ,  $OUT = Z$ , HEATER ON  
 IF  $IN+ < IN-$ ,  $OUT = LOW$ , HEATER OFF

## LED HEATER STATUS INDICATION



Might need to be changed based on your AVCC level. Designed for 5V

This schematic implements a single heater control circuit, relying on an open-drain comparator and NMOS switch for completely analog operation.

The temperature setpoint is set via the voltage on the TEMP\_VREF pin, which is compared against the voltage on the TEMP\_VIN pin. If the voltage on TEMP\_VREF is higher, the output of the comparator will go high-impedance and drive the gate of the NMOS to 5V through the 1K pull-up resistor. This should be enough to switch the MOSFET in triode with a relatively low VDS at our target current (128mA).

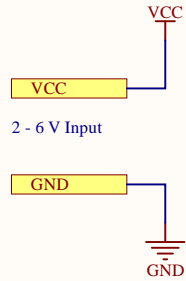
Conversely, when TEMP\_VIN is above TEMP\_VREF, the output is switched to GND and the MOSFET turns off. How you decide to set TEMP\_VREF and TEMP\_VIN is entirely up to you.

The circuit is designed to work at 5V. To operate at different voltages, just be sure to check the relevant ratings on the different components.

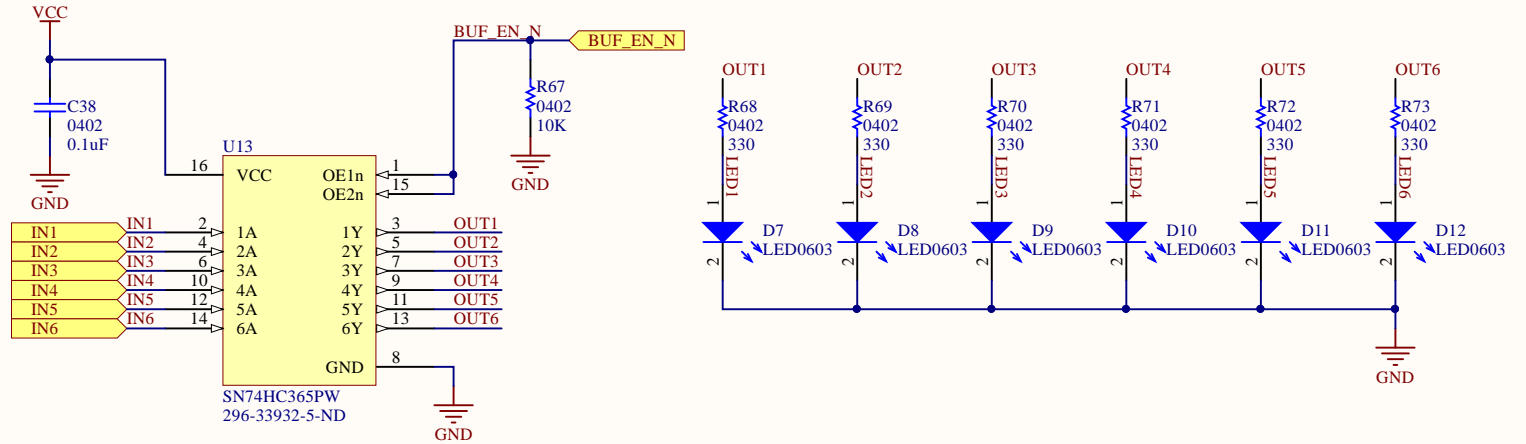
Title			
heater-control-comparator.SchDoc			
Size	Number	Revision	
A	PCBS-COMMON	1.0	
Date:	2019-07-27	Sheet *	of *
File:	C:\Users\...\heater-control-comparator.SchDoc	Drawn By:	B. Almeida, D. Vogel



# INPUT POWER



# LED BUFFER

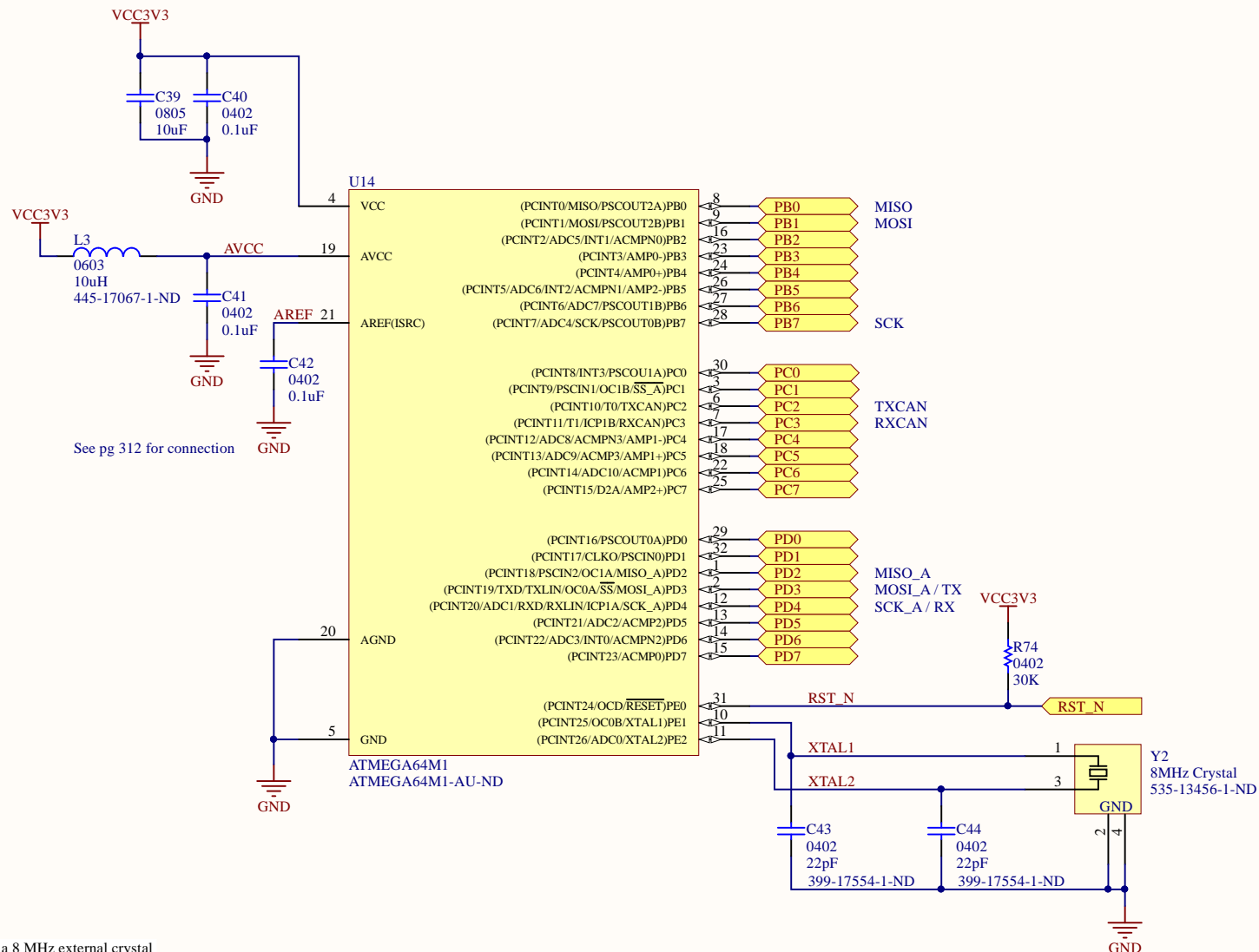
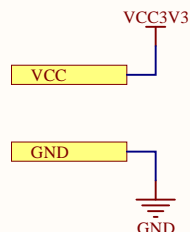


This schematic implements the SN74HC365PW non-inverting, tri-state hex buffer as an LED monitoring circuit. Connecting a signal to IN[1:6] will light up the corresponding LED on OUT[1:6].

- The BUF\_EN\_N input can be connected to a microcontroller to control the buffer. An input HIGH will set the outputs to high-impedance and disable the LEDs.
- In the schematic symbol which references this schematic sheet, parameters LED[1:6] can be added to specify the colour of each LED. See the micro-circuit common sheet for an example of this.
- Unconnected inputs should be grounded if you don't want random flickering of the LEDs.

Title			
led-monitoring-SN74HC365PW.SchDoc			
Size	Number	Revision	
A4	PCBS-COMMON	1.1	
Date:	2019-07-27	Sheet *	of *
File:	C:\Users\...led-monitoring-SN74HC365PW.SchDoc	Dylan Vogel	

# POWER INPUT

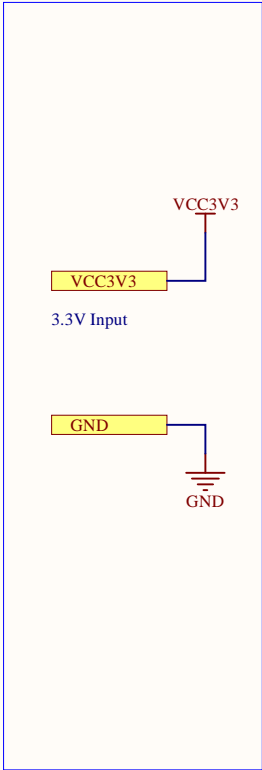


This schematic implements the ATMEGA64M1 microcontroller with a 8 MHz external crystal and necessary power connections.

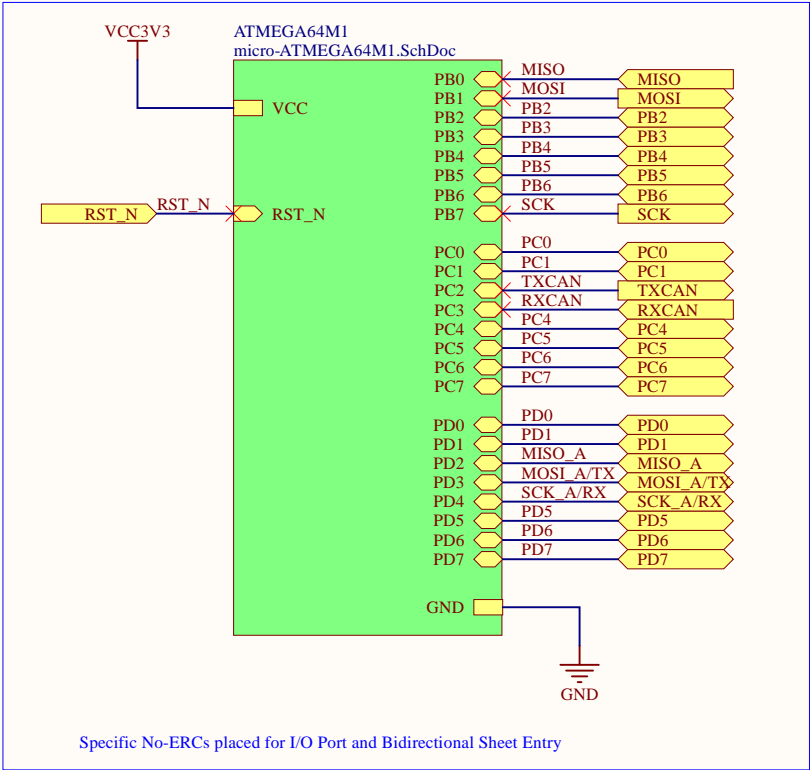
- Crystal is connected in a Pierce configuration, values of the capacitors were calculated based on the capacitance of the crystal and ESR.
- I would read through 18.5.2 and 18.6.2 of the complete 64M1 datasheet if you're interested in the motivation behind the ADC input connections. They recommend connecting AVCC through a RC lowpass network to minimize noise.
- If the ADC functionality of the device is used, either AVCC or the internal 2.56 V source can be selected in software as the reference voltage.

Title			
micro-ATMEGA64M1.SchDoc			
Size	Number	Revision	
A4	PCBS-COMMON	1.1	
Date:	2019-07-27	Sheet *	of *
File:	C:\Users\...\micro-ATMEGA64M1.SchDoc Drawn By: Dylan Vogel		

POWER INPUTS

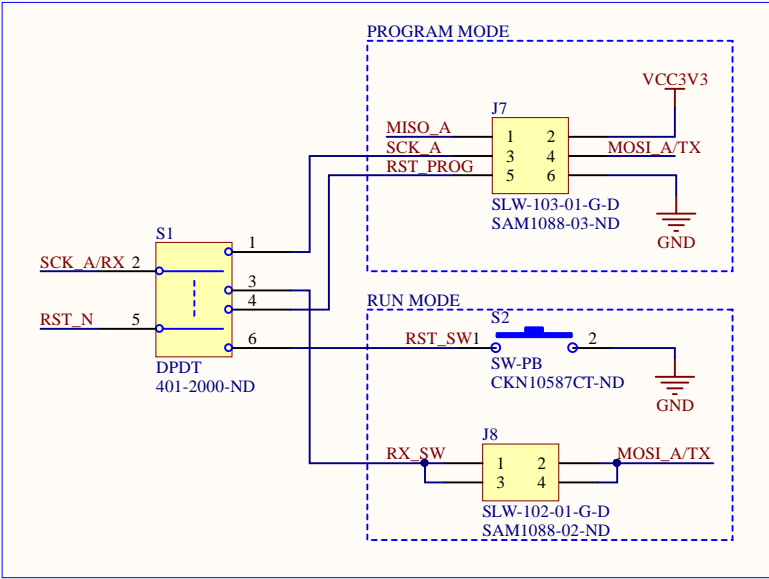


ATMEGA32M1

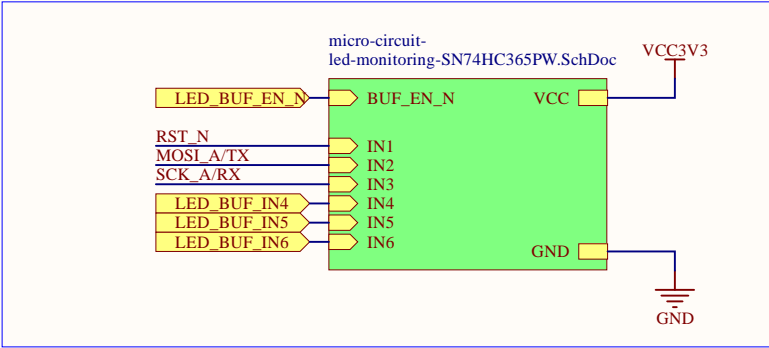


Specific No-ERCs placed for I/O Port and Bidirectional Sheet Entry

MODE SELECT CIRCUITRY



LED MONITORING

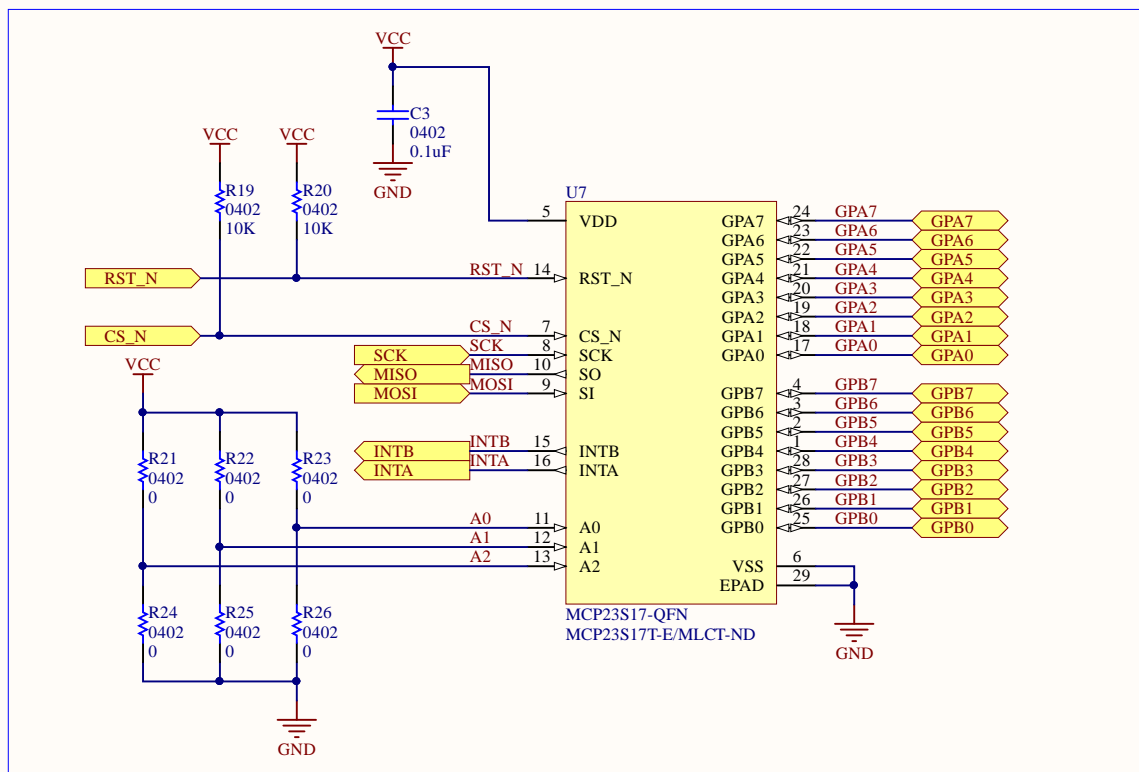
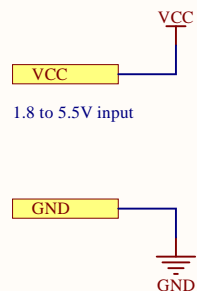


This schematic extends the functionality already included in the micro-ATMEGA32M1 schematc, adding a mode select switch, programming header, reset button and LED indication for TX, RX and RSTn.

- IN[4:6] of the LED buffer have been left unconnected, but are broken out on ports LED\_BUF\_IN[4:6]. They can be connected in the schematic which includes this sheet up to an additional 3 lines. Highly recommend more blinking lights.

Title			
micro-circuit-ATMEGA64M1.SchDoc			
Size	Number	Revision	
A4	PCBS-COMMON	1.1	
Date:	2019-07-27	Sheet *	of *
File:	C:\Users\...\micro-circuit-ATMEGA64M1.SchDoc	Drawn By:	Dylan Vogel

## POWER INPUTS



## ADDRESS:

### CHANNEL SELECTION

ONLY SOLDER ONE 0 OHM FROM EACH PAIR  
 PEX ADDRESS = A2 A1 A0  
 VCC == 1 GND == 0

This schematic implements the MCP23S17 SPI port expander, and does some common-sense things like adding a bypass capacitor to the power supply and pull-up resistors to RST\_N and CS\_N.

Multiple port expanders can be connected to the same CS\_N line, and accessed via a device address that is used during software communication. This address is set in hardware via the A2, A1 and A0 pins. Soldering a 0 ohm resistor to VCC will set that bit to 1, and soldering to GND will set that bit to 0.

In the schematic which includes this file, you should make some note of the relevant hardware address that should be soldered during manufacturing.

Title			
pex-MCP23S17.SchDoc			
Size	Number	Revision	
A4		PCBS-COMMON	
Date:	2019-07-27	Sheet *	of *
File:	C:\Users\...\pex-MCP23S17.SchDoc	Drawn By:	Dylan Vogel

