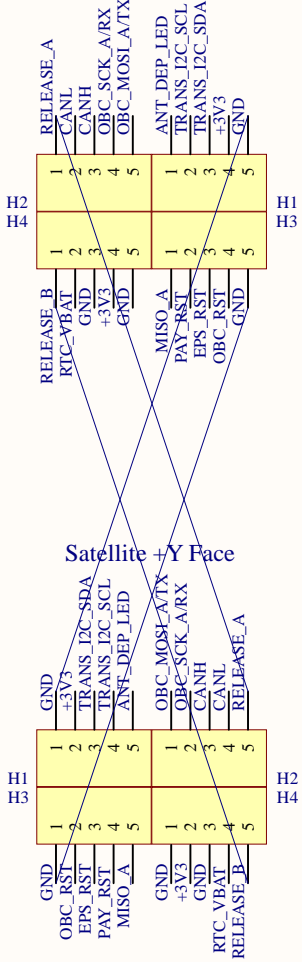


OBC PCB

View looking from the BOTTOM of the satellite UP stacked on top of EPS PCB

Satellite +X Face

Satellite +Y Face

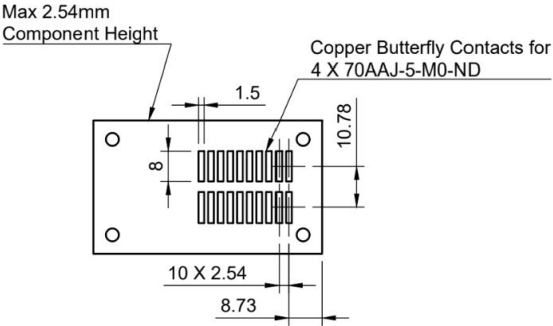
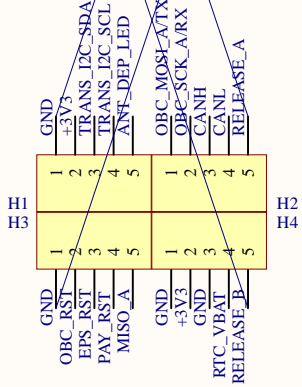


EPS PCB

View looking from the TOP of the satellite DOWN

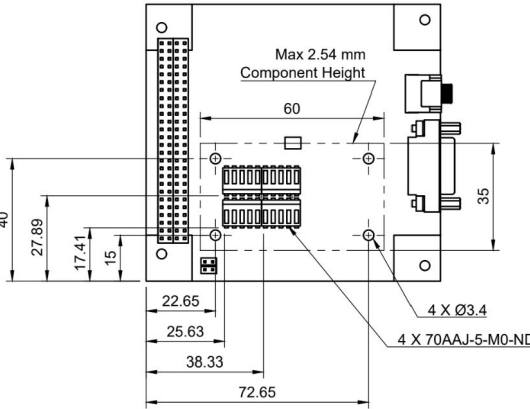
Satellite +X Face

Satellite +Y Face



OBC (BOTTOM VIEW)

Butterfly Connector (70AAJ-5-M0-ND)
5x1 pins per connector, 2x2 connectors, 10x2 pins total
Note use of the 5-pin variant (4-pin is shown in datasheet)

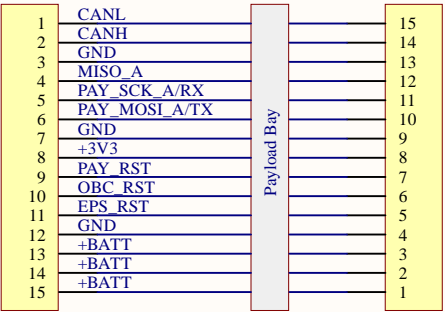


OBC Interfacing (TOP VIEW)

Title			
EPS-OBC Interface			
Size	Number	Revision	
A4	1	v1.0	
Date:	2019-07-19	Sheet	1 of 8
File:	C:\Users\...\eps-obc.SchDoc	Drawn By:	Jaden Reimer

EPS PCB

Hirose DF13 15-Pin Header:
<https://www.digikey.ca/product-detail/en/hirose-electric-co-ltd/DF13A-15-P-1.25H-21/H125988CT-ND/948972>
6



PAY-SSM PCB

Hermetic connector (15 pins, Glenair 177-705H or 177-706H)
<https://www.datasheets360.com/pdf/2123725778547446062>

Premade wires (15 pins, 28 AWG)
Similar to <https://www.digikey.ca/short/j037h5>
Connections not flipped within cable's wires
Needs to be hand-crimped on the payload bay side for the hermic connector

Title			
EPS-PAY Interface			
Size	Number		Revision
A4	2		v1.0
Date:	2019-07-19		Sheet 2 of 8
File:	C:\Users\...\eps-pay.SchDoc		Drawn By: Jaden Reimer

EPS PCB

Mini DSUB-25 Connector

Buffer needed on EPS for C and D gate signals

1	GND	1
2	MISO_A	2
3	EPS_MOSI_A/TX	3
4	EPS_SCK_A/RX	4
5	EPS_RST	5
6	OBC_MOSI_A/TX	6
7	OBC_SCK_A/RX	7
8	OBC_RST	8
9	PAY_MOSI_A/TX	9
10	PAY_SCK_A/RX	10
11	PAY_RST	11
12	CANH	12
13	CANL	13
14	TRANS_I2C_SDA	14
15	TRANS_I2C_SCL	15
16	C_GATE	16
17	D_GATE	17
18	RELEASE_A	18
19	RELEASE_B	19
20	GND	20
21	+3V3	21
22	+5V	22
23	GND	23
24	+PACK	24
25	RTC_VBAT	25

Systems PCB

Outside of satellite
Only for testing/debugging

DSUB-25 Connector

Spliced Cable
Connections are flipped within the cable's wires,
so the pin numbers match on both ends

Title EPS-SYS Interface		
Size A4	Number 3	Revision v1.0
Date: File:	2019-07-19 C:\Users\...\eps-sys.SchDoc	Sheet 3 of 8 Drawn By: Jaden Reimer

Transceiver stacked on top of
EPS PCB using header pins

Transceiver customized to use +5V supply,
not +3.3V

Comms signals routed from OBC through EPS board

WARNING: In UHF Manual and Protocol Rev. 2, the connector pinout
diagram on p. 11, for each of H1 and H2, rows 1 and 2 are flipped
i.e. H1 and H2 are placed correctly, but the bottom left in the image
should be H1, pin 1, and the top left should be H2, pin 2

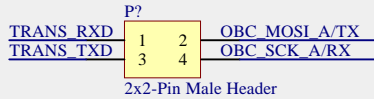
Header layout based on UHF_UTAT_Conn_Pinout.pdf
(add En UHF Opt. and En UHF just in case)

RxD and TxD are the UART lines with respect to the transceiver
(i.e. transceiver receives UART on RxD and transmits UART on TxD)

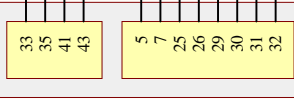
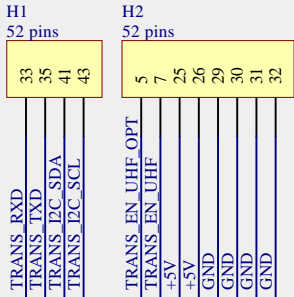
RELEASE_A and RELEASE_B can be used as Antenna Deployment
GPIO from OBC

Modified version of PC104-Plus connector
dimensions (notably 2mm pitch)

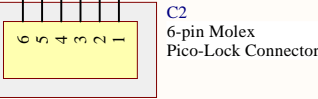
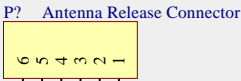
Use thick traces and all available header
pins for +5V and GND



OBC UART - Transceiver Connection
To use the transceiver permanently,
short pin 1 to pin 2, short pin 3 to pin 4



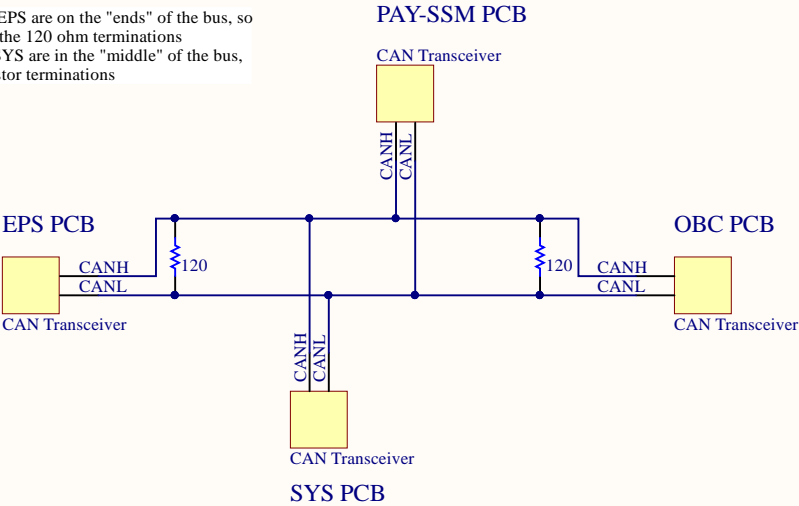
Transceiver



Antenna

Title			
Communications			
Size	Number		Revision
A4	4		v1.0
Date:	2019-07-19		Sheet 4 of 8
File:	C:\Users\...\com.SchDoc		Drawn By: Jaden Reimer

OBC and EPS are on the "ends" of the bus, so they have the 120 ohm terminations
PAY and SYS are in the "middle" of the bus, so no resistor terminations



Title		
CAN Bus		
Size	Number	Revision
A4	5	v1.0
Date:	2019-07-19	Sheet 5 of 8
File:	C:\Users\...\can.SchDoc	Drawn By: Jaden Reimer

A

A

B

B

C

C

D

D

2-Pos Right Angle Battery Connector
Samtec SAM9552-ND:
<https://www.digikey.ca/products/en?keywords=sam9552-nd>

Flight model connectors should have gold mating finish

+BATT is the raw voltage across the battery pack (ignoring connection to EPS)

+PACK is the voltage from the battery pack to the EPS board (after deployment switches and RBF pin)

If the battery pack is connected to the EPS electronics (i.e. DS1, DS2, RBF all connected), +PACK = +BATT

If the battery pack is disconnected from the EPS electronics (i.e. one or more of DS1, DS2, RBF disconnected), +PACK = 0

Protection Circuit Limits:
Max charge = 4.190V, Charge release = 4.090V
Max discharge = 2.70V, Discharge release = 3.00V

Absolute Maximum Battery Voltage Range: 2.5V-4.2V

Satellite faces

Solar Panel PCBs

EPS PCB

OBC PCB

MISO_A is universal across all subsystems

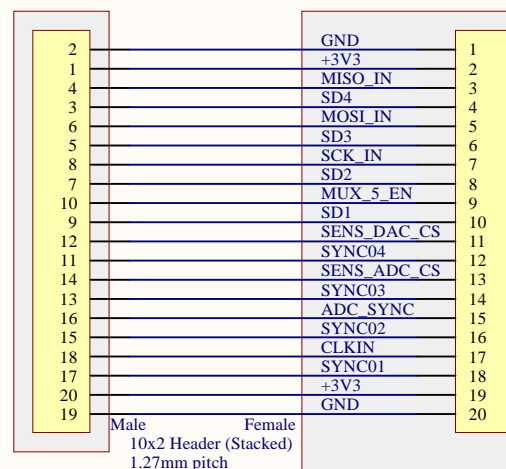
Heaters in battery pack

Thermistors in battery pack

Title			
BUS (EPS and OBC)			
Size	Number		Revision
A4	6		v1.0
Date:	2019-07-19		Sheet 6 of 8
File:	C:\Users\...\bus.SchDoc		Drawn By: Jaden Reimer

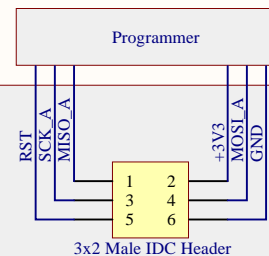
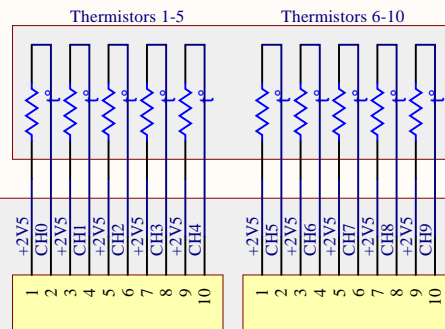
PAY-Optical PCB

(stacked on top of PAY-SSM)

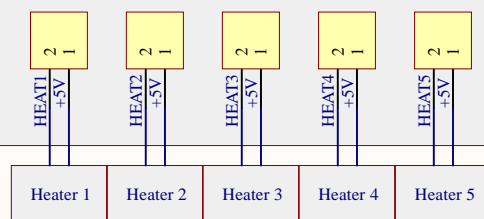


Start thermistor numbering from 0
to match ADC channel numbering

Thermistors (in microfluidics chips)

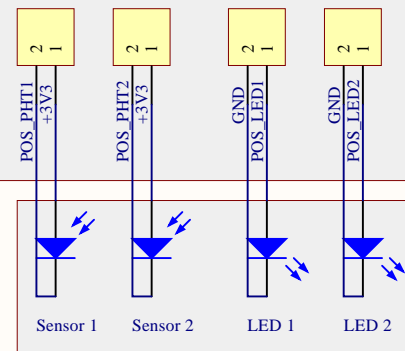


PAY-SSM PCB



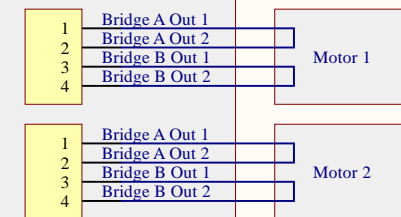
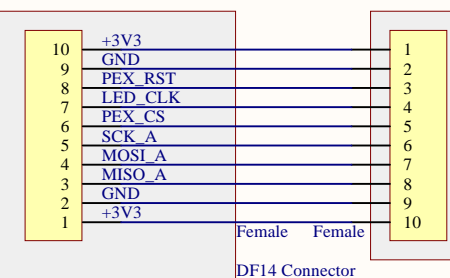
2-pin DF13 connector:
<https://www.digikey.ca/product-detail/en/hirose-electric-co-ltd/DF13A-2P-1.25H-21/H125743CT-ND/8594822>

Flight model connectors should have gold mating finish



Positioning - Photodiode Setup

PAY-LED PCB (x2)



Actuation Plate Setup

Title			
Payload			
Size	Number		Revision
A4	7		v1.0
Date:	2019-07-19		Sheet 7 of 8
File:	C:\Users\...\pay.SchDoc		Drawn By: Jaden Reimer

