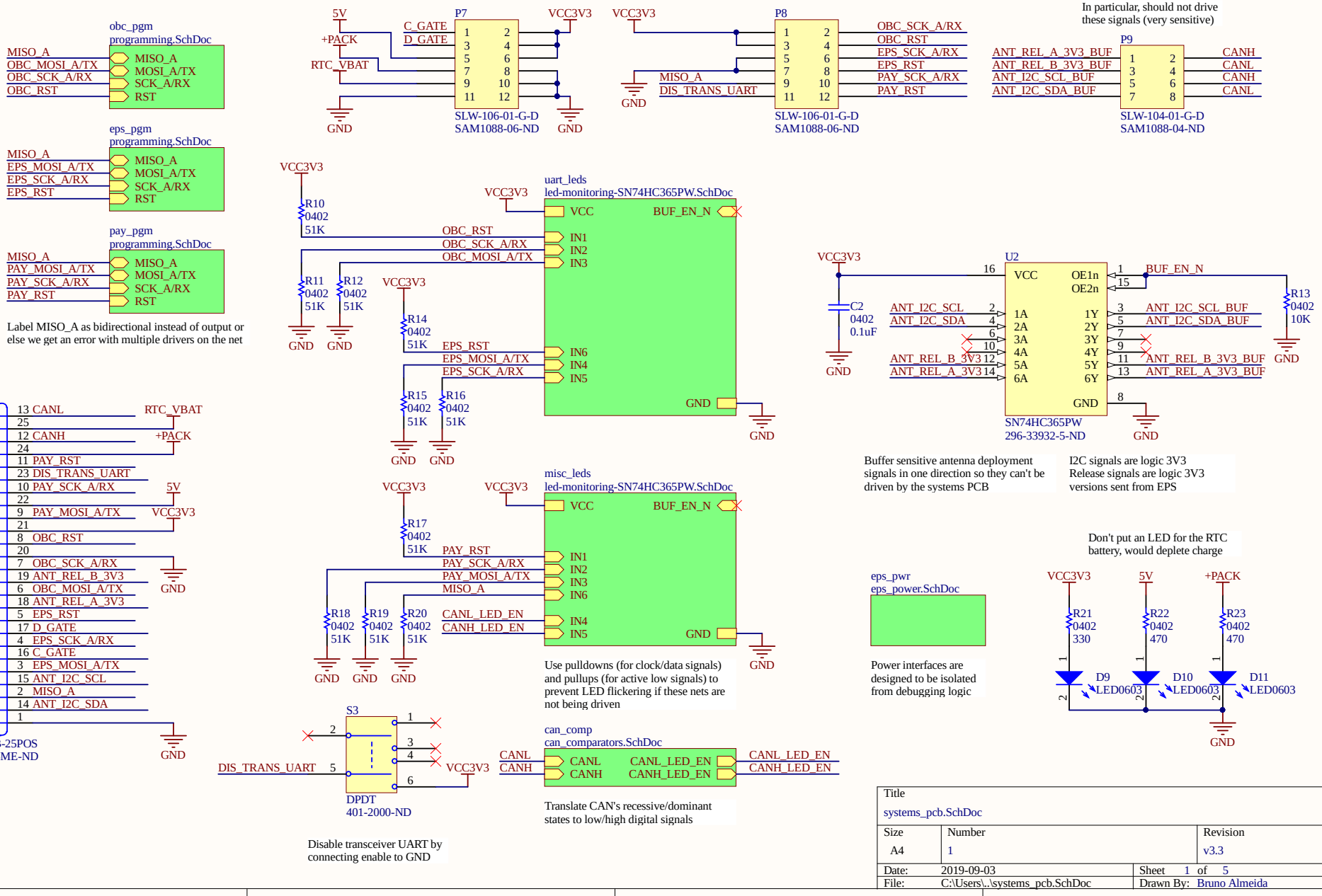

obc_pgm
programming.SchDoc
MISO_A
OBC_MOSI_A/TX
OBC_SCK_A/RX
OBC_RST
MISO_A
MOSI_A/TX
SCK_A/RX
RST
eps_pgm
programming.SchDoc
MISO_A
EPS_MOSI_A/TX
EPS_SCK_A/RX
EPS_RST
MISO_A
MOSI_A/TX
SCK_A/RX
RST
pay_pgm
programming.SchDoc
MISO_A
PAY_MOSI_A/TX
PAY_SCK_A/RX
PAY_RST
MISO_A
MOSI_A/TX
SCK_A/RX
RST
Label MISO_A as bidirectional instead of output or else we get an error with multiple drivers on the net
5V
+PACK
RTC_VBAT
C_GATE
D_GATE
P7
VCC3V3
SLW-106-01-G-D
SAM1088-06-ND
GND
VCC3V3
MISO_A
DIS_TRANS_UART
P8
OBC_SCK_A/RX
OBC_RST
EPS_SCK_A/RX
EPS_RST
PAY_SCK_A/RX
PAY_RST
SLW-106-01-G-D
SAM1088-06-ND
In particular, should not drive these signals (very sensitive)
P9
ANT_REL_A_3V3_BUF
ANT_REL_B_3V3_BUF
ANT_I2C_SCL_BUF
ANT_I2C_SDA_BUF
CANH
CANL
CANH
CANL
SLW-104-01-G-D
SAM1088-04-ND
VCC3V3
R10
0402
51K
OBC_RST
OBC_SCK_A/RX
OBC_MOSI_A/TX
R11
0402
51K
R12
0402
51K
R14
0402
51K
EPS_RST
EPS_MOSI_A/TX
EPS_SCK_A/RX
R15
0402
51K
R16
0402
51K
uart_leds
led-monitoring-SN74HC365PW.SchDoc
VCC
BUF_EN_N
IN1
IN2
IN3
IN6
IN4
IN5
GND
VCC3V3
C2
0402
0.1uF
U2
ANT_I2C_SCL
ANT_I2C_SDA
ANT_REL_B_3V3
ANT_REL_A_3V3
BUF_EN_N
ANT_I2C_SCL_BUF
ANT_I2C_SDA_BUF
ANT_REL_B_3V3_BUF
ANT_REL_A_3V3_BUF
R13
0402
10K
SN74HC365PW
296-33932-5-ND
Buffer sensitive antenna deployment signals in one direction so they can't be driven by the systems PCB
I2C signals are logic 3V3
Release signals are logic 3V3 versions sent from EPS
J4
13 CANL
25
12 CANH
24
11 PAY_RST
23 DIS_TRANS_UART
10 PAY_SCK_A/RX
22
9 PAY_MOSI_A/TX
21
8 OBC_RST
20
7 OBC_SCK_A/RX
19 ANT_REL_B_3V3
6 OBC_MOSI_A/TX
18 ANT_REL_A_3V3
5 EPS_RST
17 D_GATE
4 EPS_SCK_A/RX
16 C_GATE
3 EPS_MOSI_A/TX
15 ANT_I2C_SCL
2 MISO_A
14 ANT_I2C_SDA
1
26
27
D-SUB-25POS
182-25ME-ND
RTC_VBAT
+PACK
5V
VCC3V3
GND
misc_leds
led-monitoring-SN74HC365PW.SchDoc
R17
0402
51K
PAY_RST
PAY_SCK_A/RX
PAY_MOSI_A/TX
MISO_A
R18
0402
51K
R19
0402
51K
R20
0402
51K
CANL_LED_EN
CANH_LED_EN
Use pulldowns (for clock/data signals) and pullups (for active low signals) to prevent LED flickering if these nets are not being driven
Don't put an LED for the RTC battery, would deplete charge
eps_pwr
eps_power.SchDoc
Power interfaces are designed to be isolated from debugging logic
R21
0402
330
R22
0402
470
R23
0402
470
D9
LED0603
D10
LED0603
D11
LED0603
S3
DIS_TRANS_UART
DPDT
401-2000-ND
Disable transceiver UART by connecting enable to GND
can_comp
can_comparators.SchDoc
CANL
CANH
CANL_LED_EN
CANH_LED_EN
Translate CAN's recessive/dominant states to low/high digital signals
Title
systems_pcb.SchDoc
Size
A4
Number
1
Revision
v3.3
Date: 2019-09-03
Sheet 1 of 5
File: C:\Users\..\systems_pcb.SchDoc
Drawn By: Bruno Almeida

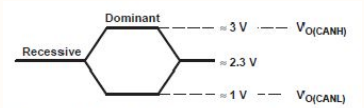
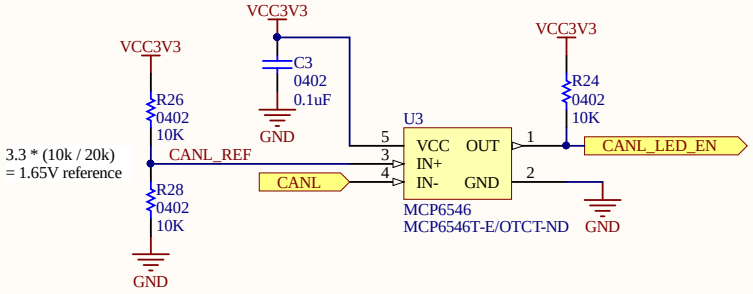
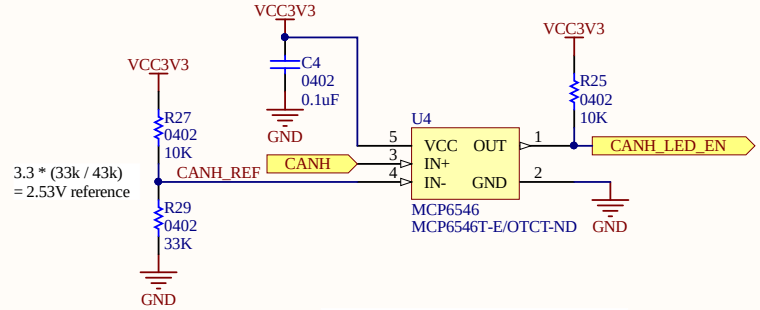


Figure 13. Bus Logic State Voltage Definitions

SN65HVD233D CAN transceiver logic voltages



If CANL < 1.65V, CANL_LED_EN = high
If CANL > 1.65V, CANL_LED_EN = low



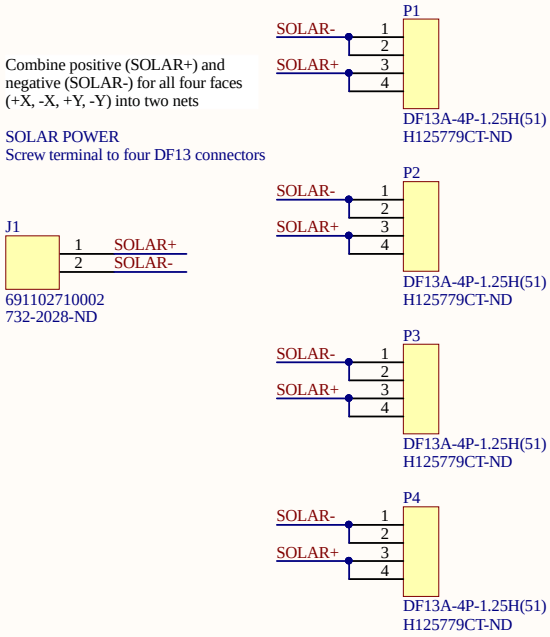
If CANH > 2.53V, CANH_LED_EN = high
If CANH < 2.53V, CANH_LED_EN = low

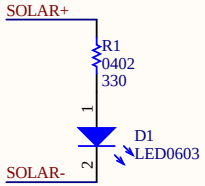
Comparators have open-drain outputs
Divider ratios can be adjusted based on experimental results

Title	can_comparators.SchDoc	
Size: A4	Number: 2	Revision: v3.3
Date: 2019-09-03		Sheet 2 of 5
File: C:\Users\..\can_comparators.SchDoc		Drawn By: Bruno Almeida

Combine positive (SOLAR+) and negative (SOLAR-) for all four faces (+X, -X, +Y, -Y) into two nets

SOLAR POWER
Screw terminal to four DF13 connectors

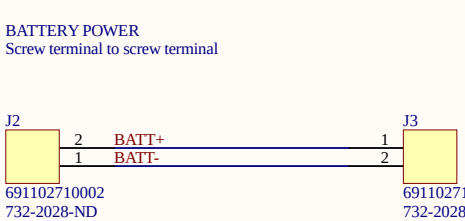


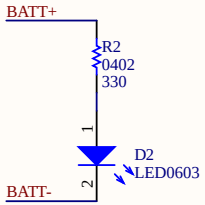


Should not unify the grounds here

On the EPS PCB, the ground will be unified between GND, SOLAR-, and BATT- subject to the deployment switch states

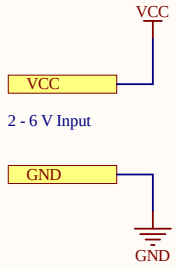
BATTERY POWER
Screw terminal to screw terminal



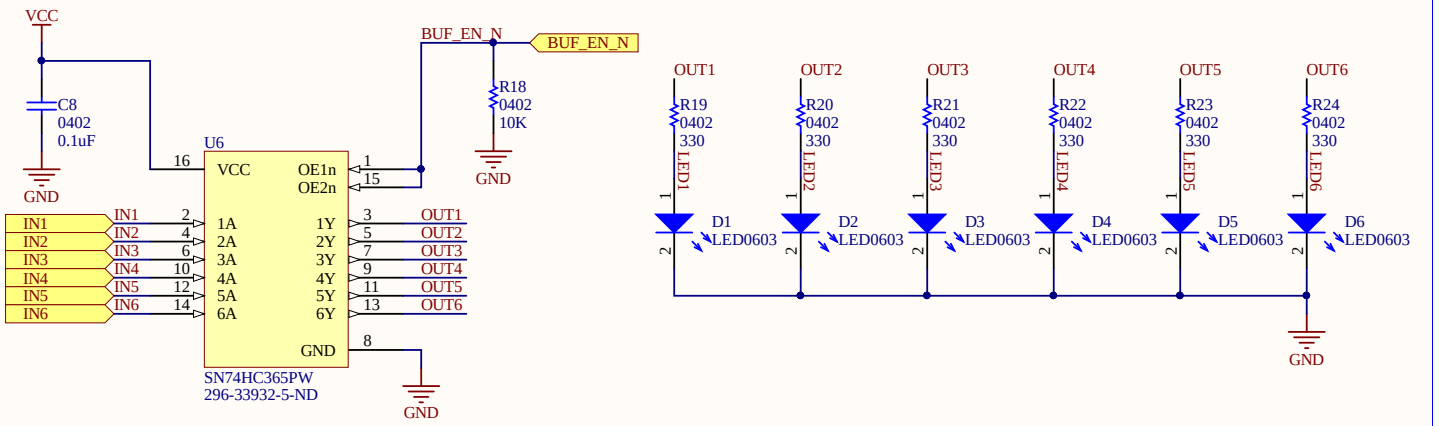


Title: eps_power.SchDoc		
Size: A4	Number: 3	Revision: v3.3
Date: 2019-09-03		Sheet 3 of 5
File: C:\Users\..\eps_power.SchDoc		Drawn By: Bruno Almeida

INPUT POWER



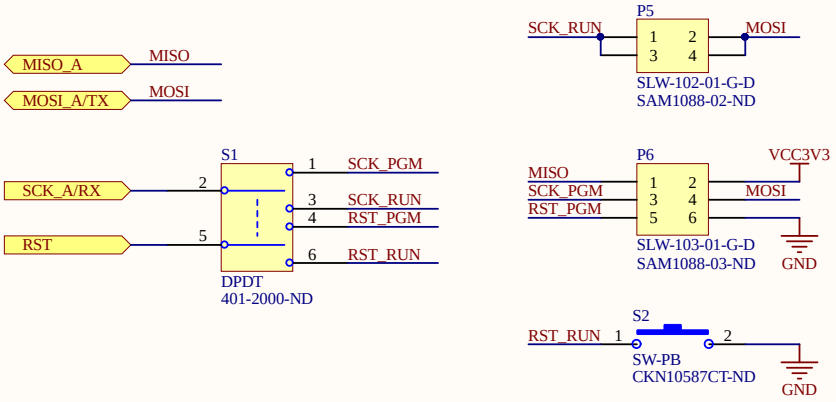
LED BUFFER



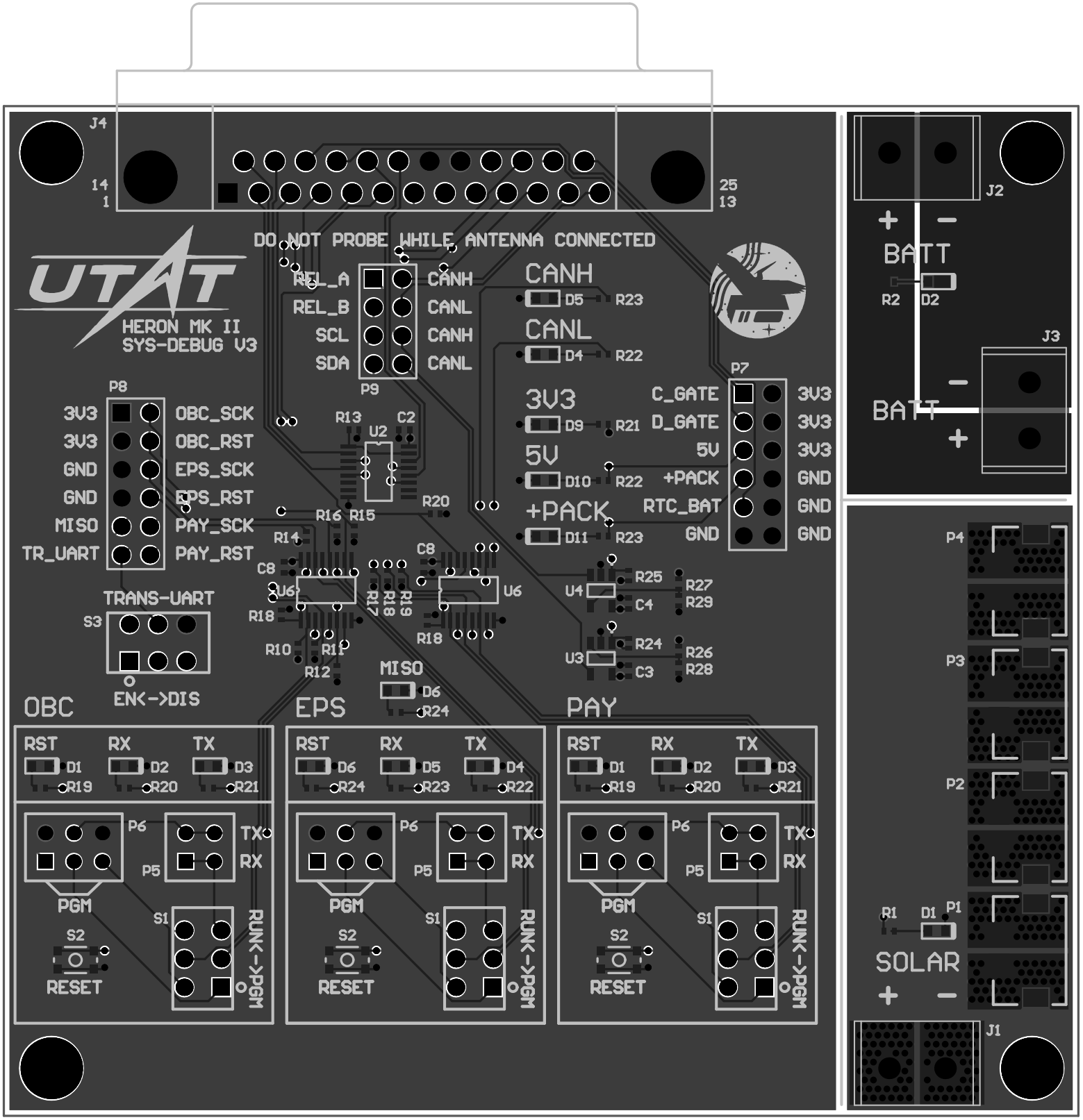
This schematic implements the SN74HC365PW non-inverting, tri-state hex buffer as an LED monitoring circuit. Connecting a signal to IN[1:6] will light up the corresponding LED on OUT[1:6].

- The BUF_EN_N input can be connected to a mircocontroller to control the buffer. An input HIGH will set the outputs to high-impedance and disable the LEDs.
- In the schematic symbol which references this schematic sheet, parameters LED[1:6] can be added to specify the colour of each LED. See the micro-circuit common sheet for an example of this.
- Unconnected inputs should be grounded if you don't want random flickering of the LEDs.

Title	led-monitoring-SN74HC365PW.SchDoc		
Size	Number		Revision
A4	PCBS-COMMON		1.1
Date:	2019-09-03	Sheet 4 of 5	
File:	C:\Users\..\led-monitoring-SN74HC365PW.SchDoc	Drawn By:	Dylan Vogel



Title	programming.SchDoc	
Size: A4	Number: 5	Revision: v3.3
Date: 2019-09-03	Sheet 5 of 5	
File: C:\Users\..\programming.SchDoc	Drawn By: Bruno Almeida	


J4
14
1
25
13
DO NOT PROBE WHILE ANTENNA CONNECTED
UTAT
HERON MK II
SYS-DEBUG V3
REL_A
REL_B
SCL
SDA
CANH
CANL
CANH
CANL
P9
CANH
D5
R23
CANL
D4
R22
3V3
D9
R21
5V
D10
R22
+PACK
D11
R23
P7
C_GATE
D_GATE
5V
+PACK
RTC_BAT
GND
3V3
3V3
3V3
GND
GND
GND
P8
3V3
3V3
GND
GND
MISO
TR_UART
OBC_SCK
OBC_RST
EPS_SCK
EPS_RST
PAY_SCK
PAY_RST
R13
C2
U2
R16
R15
R20
R14
C8
C8
U6
U6
R17
R18
R16
R18
R10
R11
R12
TRANS-UART
S3
EN<->DIS
MISO
D6
R24
U4
R25
C4
R27
R29
U3
R24
C3
R26
R28
OBC
EPS
PAY
RST
RX
TX
D1
D2
D3
R19
R20
R21
D6
D5
D4
R24
R23
R22
P6
P5
TX
RX
PGM
S1
S2
RESET
RUN<->PGM
J2
BATT
R2
D2
J3
BATT
P4
P3
P2
R1
D1
P1
SOLAR
J1