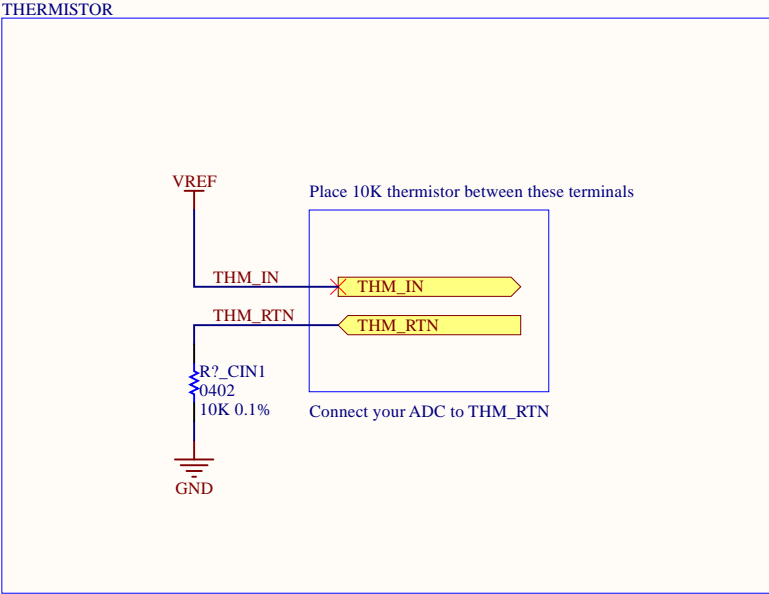
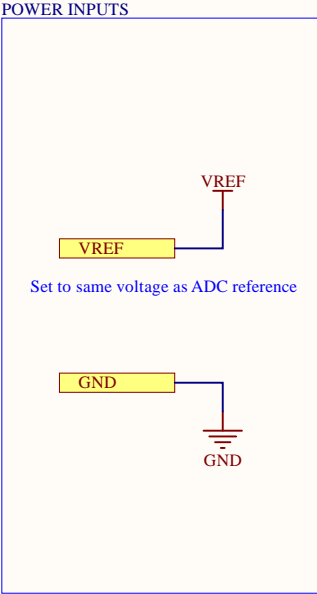
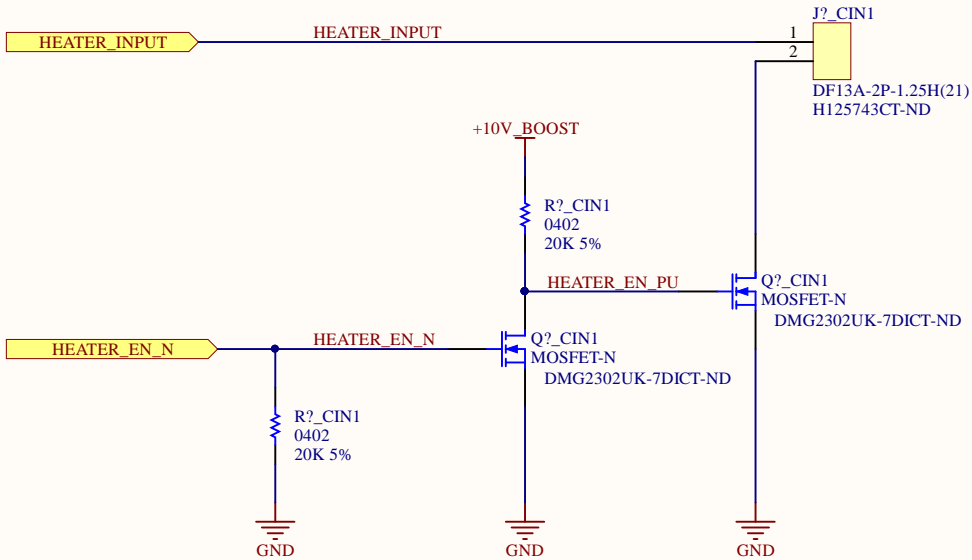
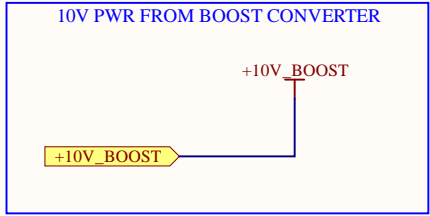


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| thermistor-input-10k.SchDoc | | | |
| Size | Number | Revision | |
| A4 | PCBS-COMMON | 1.1 | |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |



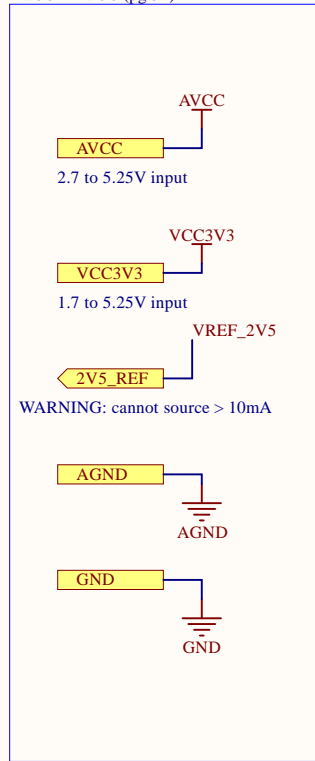
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| A4 | PCBS-COMMON | | 1.1 |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |



| Title | | |
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| Size | Number | Revision |
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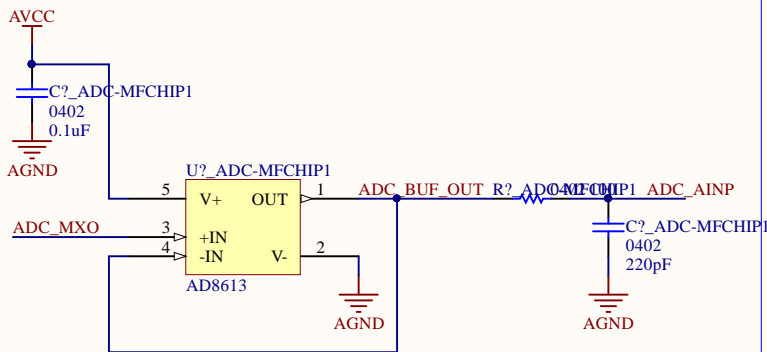
POWER PORTS

AVCC >= VCC (pg 51)



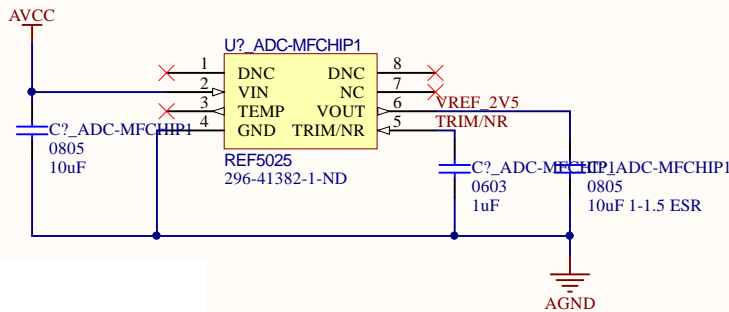
ADC INPUT BUFFER

See pg. 50 for discussion of unity buffer design procedure

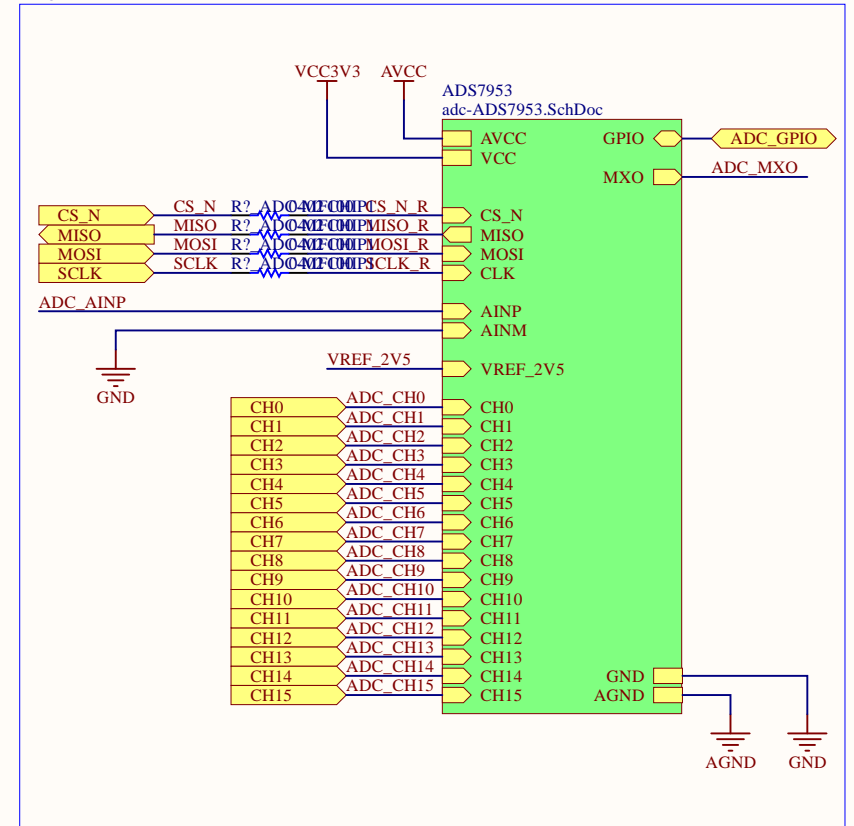


2V5 REFERENCE

Output cap should have ESR from 1 - 1.5 ohm (see pg. 21)



ADC



- This schematic implements the ADS7953 analog-to-digital converter with a 2.5V reference and a unity-gain buffer on the output of the internal multiplexer.
- Recommended input impedance should be < 1K. Higher source impedances possible with slower sampling.
 - Breaks out 2V5 for use as reference outside the circuit
 - All necessary bypassing and pull-ups implemented in the ADS7953 schematic
 - In most low-performance applications, AVCC and VCC can be tied together
 - In the layout, the pins tied to AGND should be put on a local GND pour and then tied to the global ground plane with low-impedance.
 - 100 ohm resistors on the SPI input help to isolate the ADC from digital noise

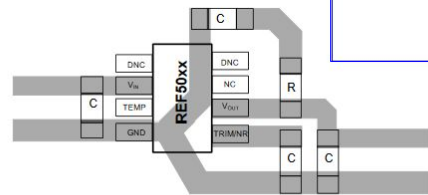


Figure 44. Layout Example

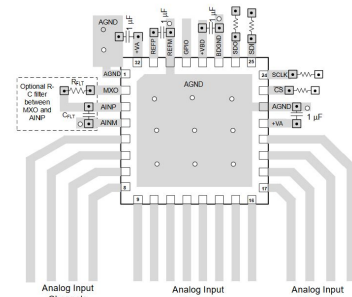
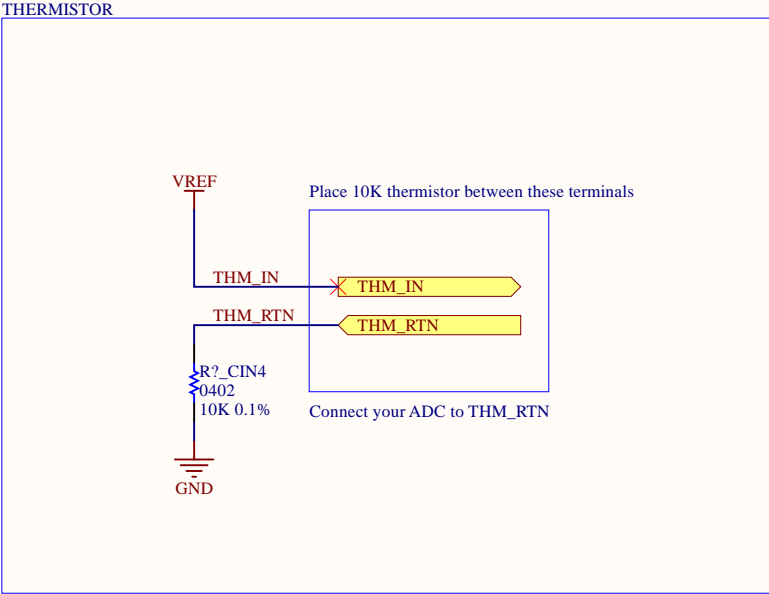
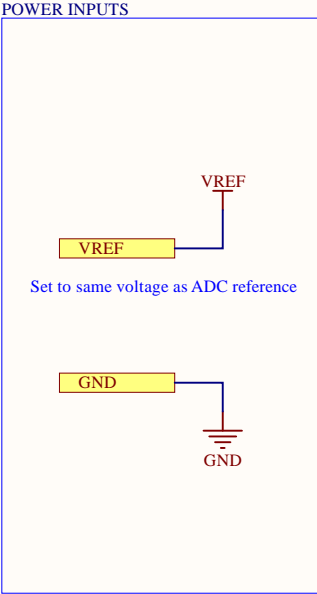
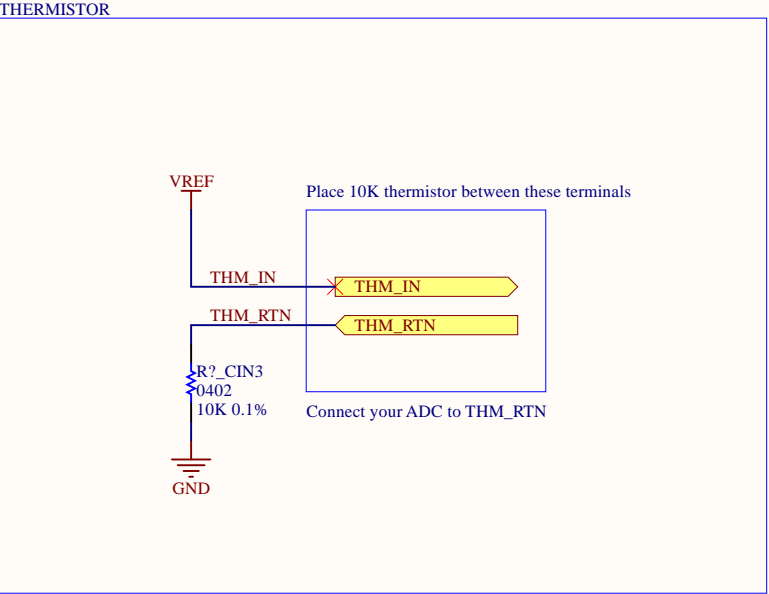
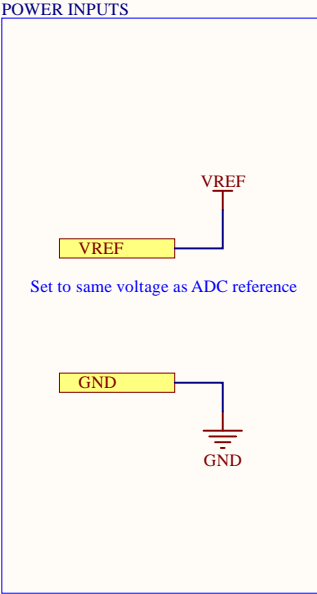


Figure 70. Recommended Layout for the VQFN Packaged Device

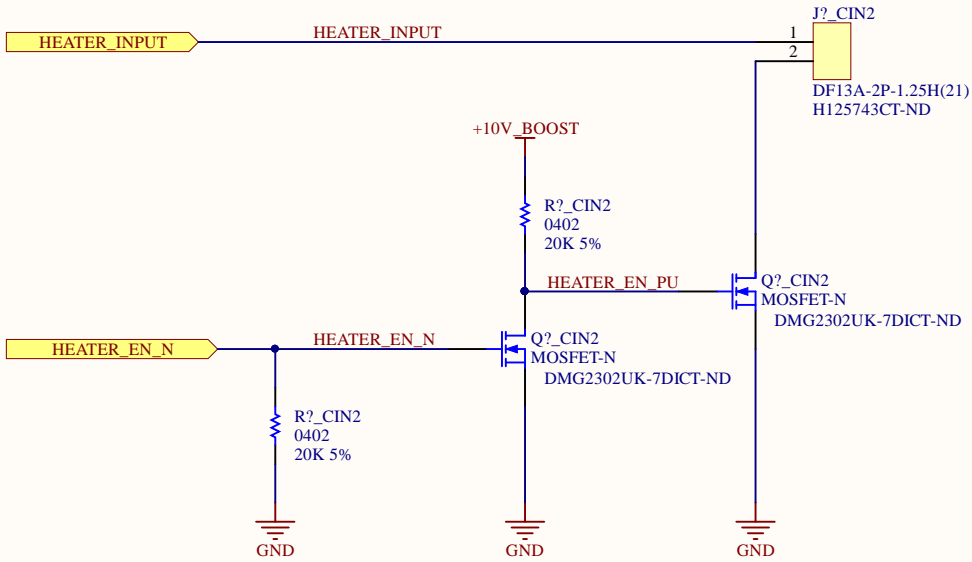
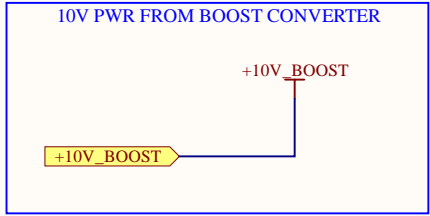
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| Title | | | |
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| Size | Number | Revision | |
| A4 | PCBS-COMMON | 1.1 | |
| Date: | 7/20/2019 | Sheet * of * | |
| File: | C:\Users\...\adc-circuit-ADS7953.SchDoc | Drawn By: | Dylan Vogel |



| | | | |
|-----------------------------|------------------------------------------|-----------|----------------------|
| Title | | | |
| thermistor-input-10k.SchDoc | | | |
| Size | Number | Revision | |
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| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |



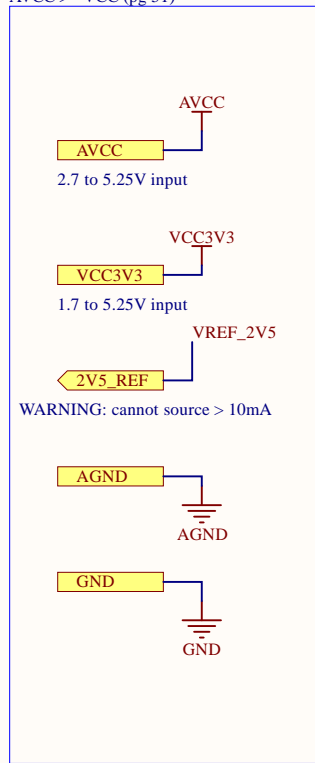
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| Size | Number | | Revision |
| A4 | PCBS-COMMON | | 1.1 |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |



| Title | | |
|-------|----------------------------------------|-----------|
| Size | Number | Revision |
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| Date: | 7/20/2019 | Sheet of |
| File: | C:\Users\...\heaters-connectors.SchDoc | Drawn By: |

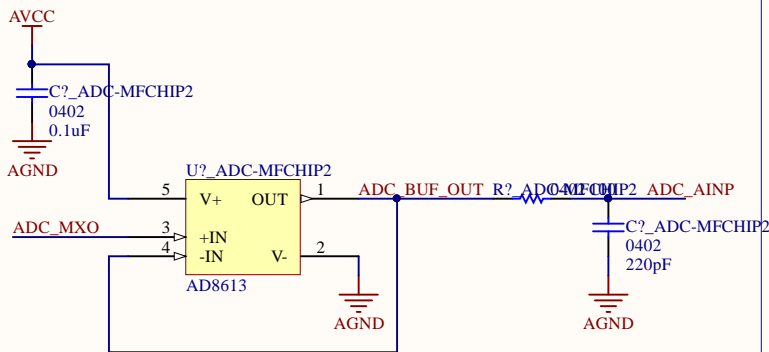
POWER PORTS

AVCC >= VCC (pg 51)



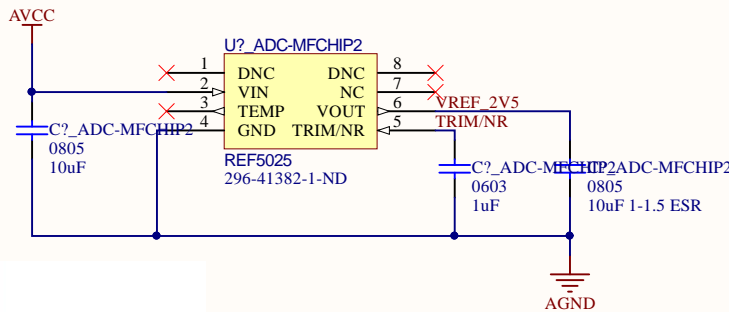
ADC INPUT BUFFER

See pg. 50 for discussion of unity buffer design procedure

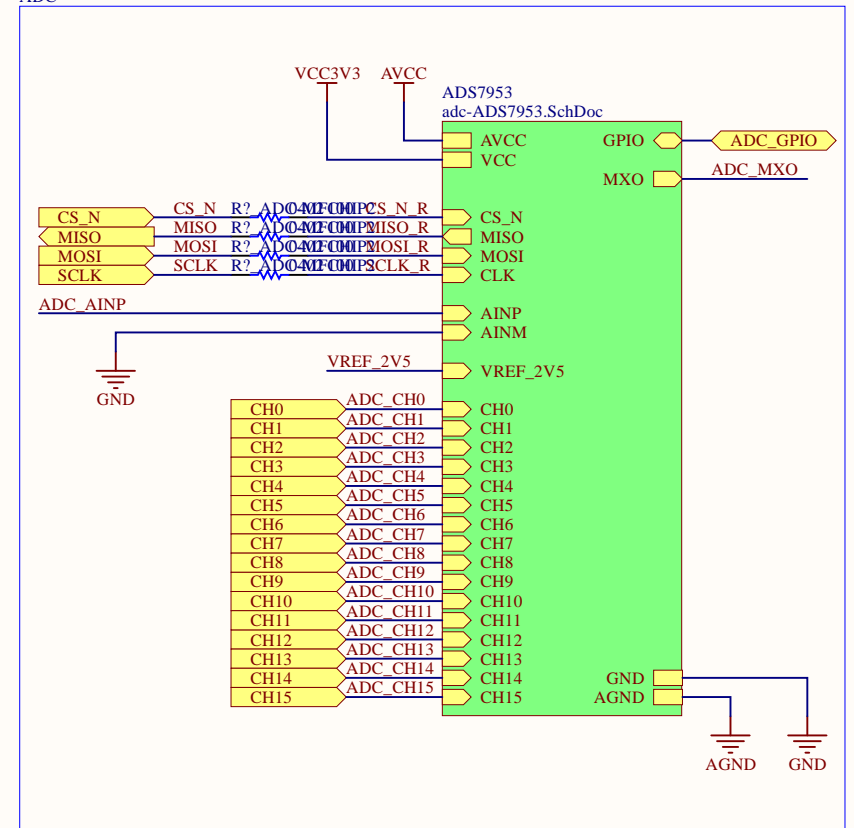


2V5 REFERENCE

Output cap should have ESR from 1 - 1.5 ohm (see pg. 21)



ADC



This schematic implements the ADS7953 analog-to-digital converter with a 2.5V reference and a unity-gain buffer on the output of the internal multiplexer.

- Recommended input impedance should be < 1K. Higher source impedances possible with slower sampling.
- Breaks out 2V5 for use as reference outside the circuit
- All necessary bypassing and pull-ups implemented in the ADS7953 schematic
- In most low-performance applications, AVCC and VCC can be tied together
- In the layout, the pins tied to AGND should be put on a local GND pour and then tied to the global ground plane with low-impedance.
- 100 ohm resistors on the SPI input help to isolate the ADC from digital noise

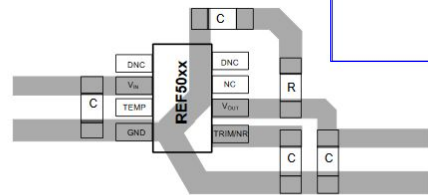


Figure 44. Layout Example

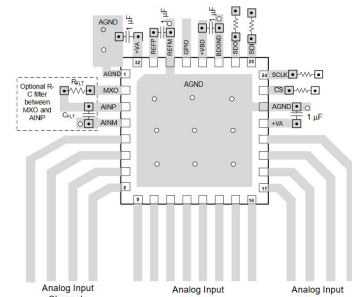
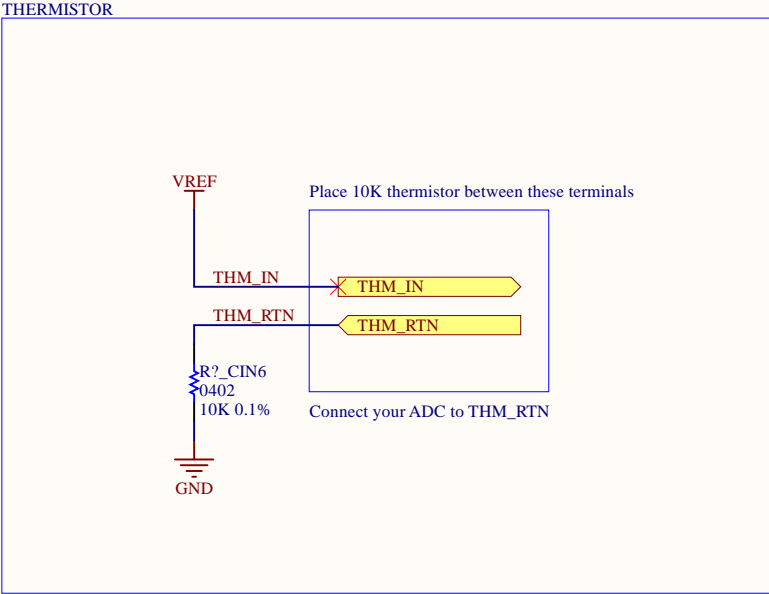
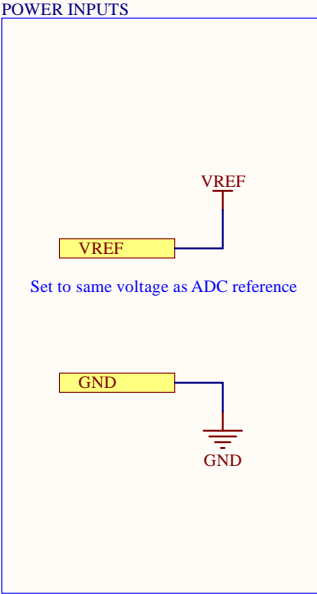
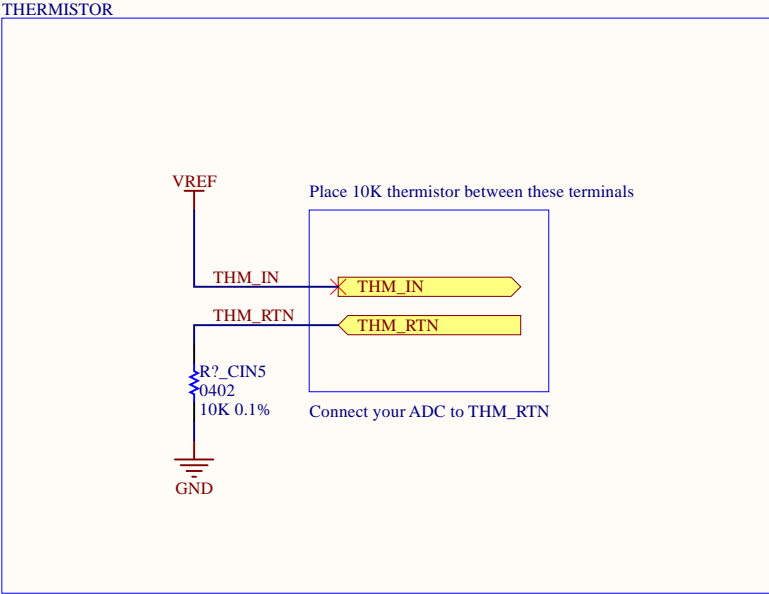
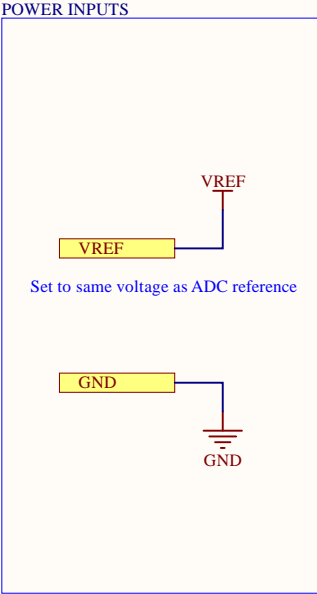


Figure 70. Recommended Layout for the VQFN Packaged Device

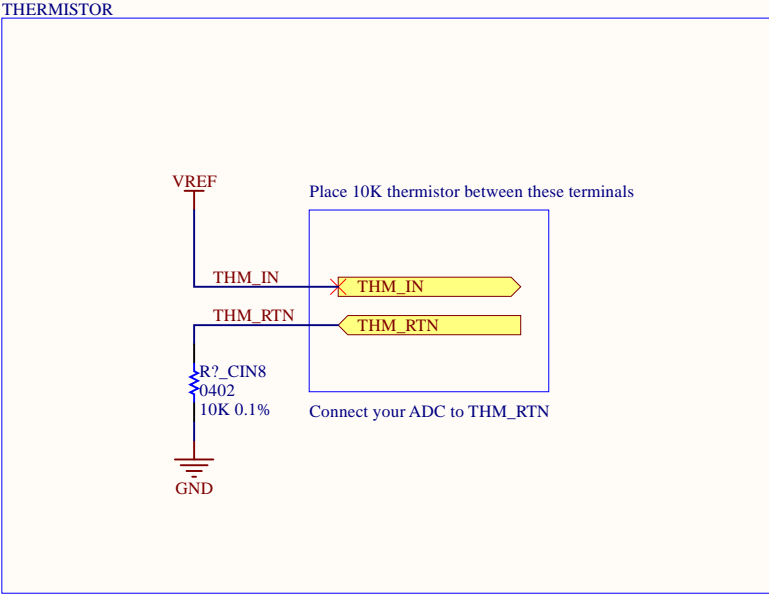
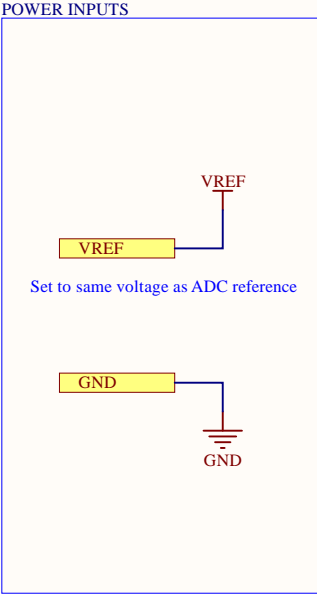
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| A4 | PCBS-COMMON | 1.1 | |
| Date: | 7/20/2019 | Sheet * of * | |
| File: | C:\Users\...\adc-circuit-ADS7953.SchDoc | Drawn By: | Dylan Vogel |



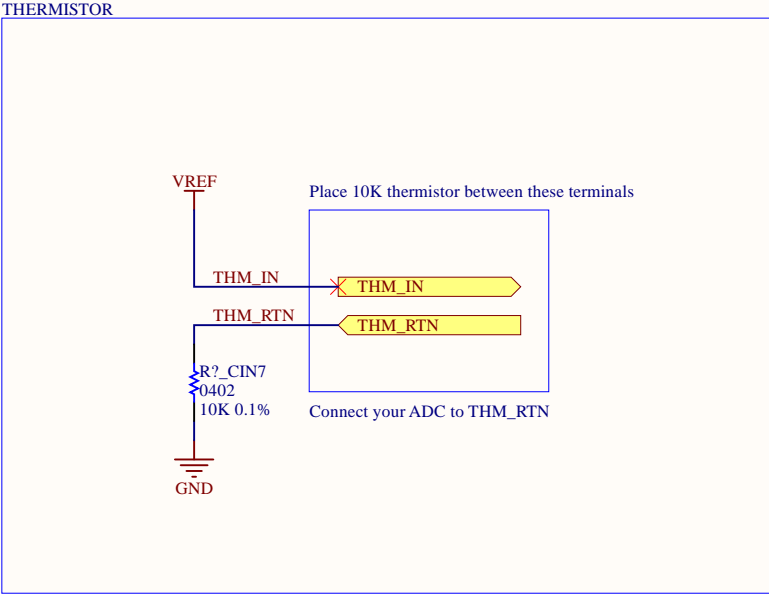
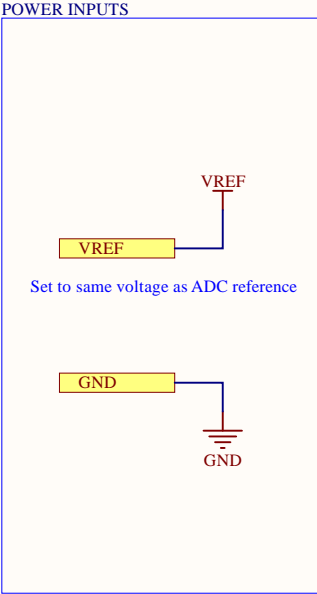
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| thermistor-input-10k.SchDoc | | | |
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| A4 | PCBS-COMMON | | 1.1 |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |



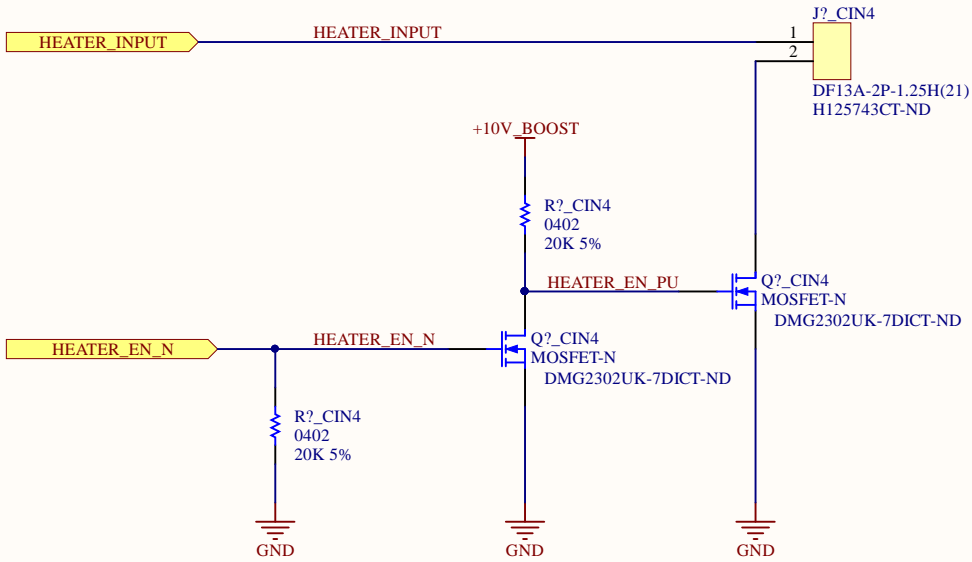
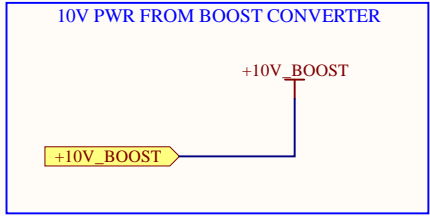
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| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |



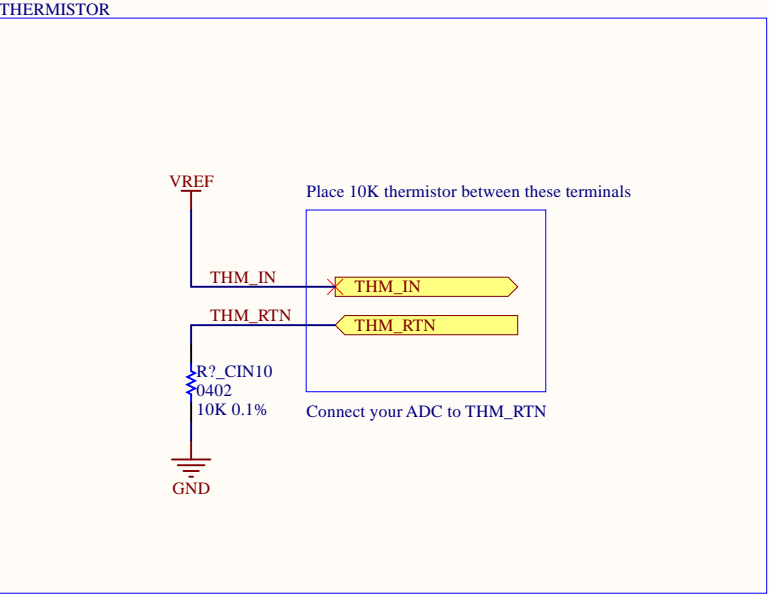
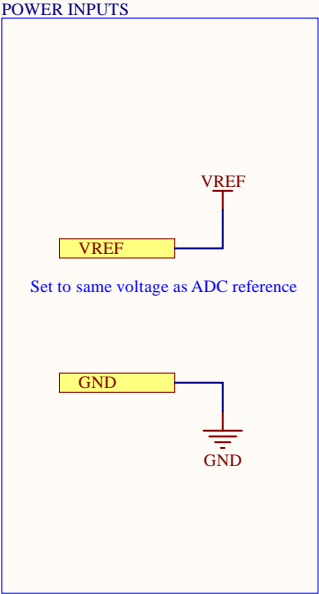
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| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |



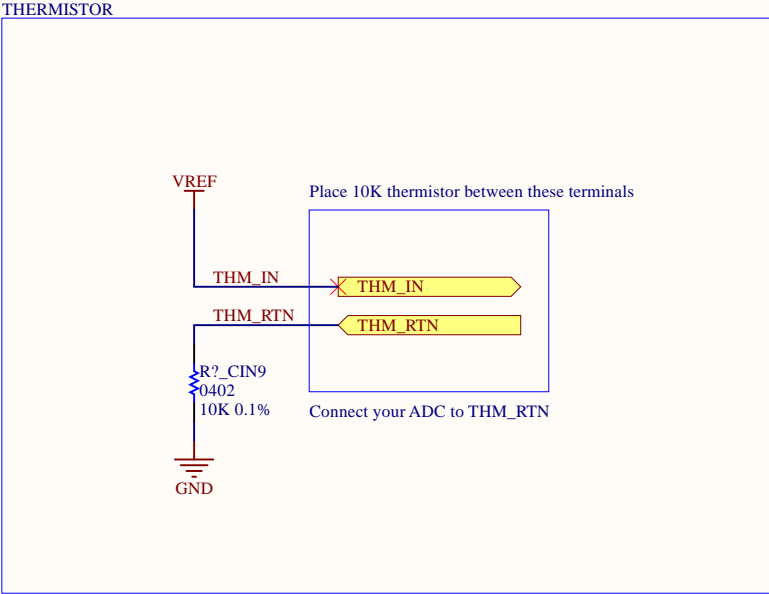
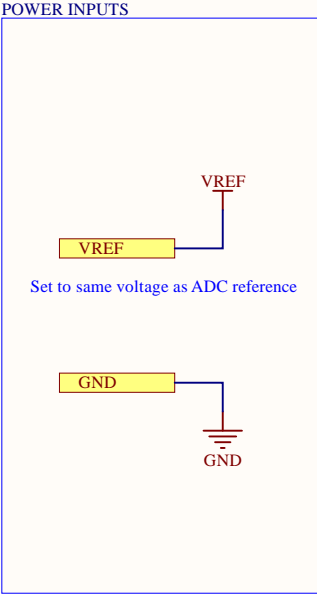
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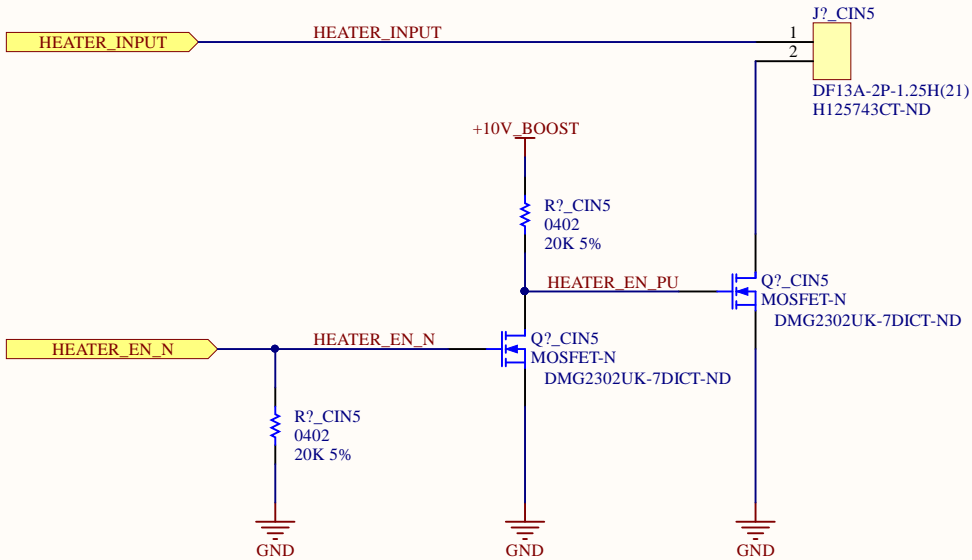
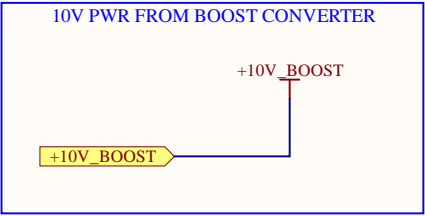
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| Size | Number | Revision |
| A4 | | |
| Date: | 7/20/2019 | Sheet of |
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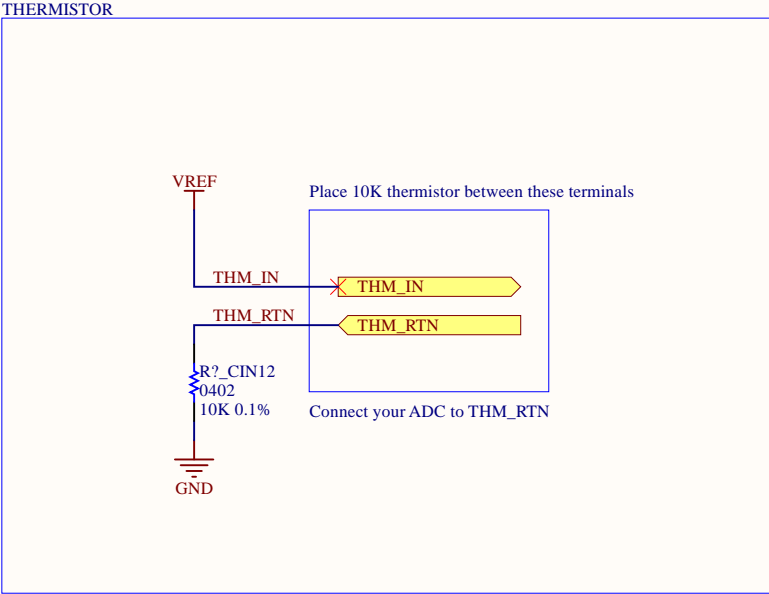
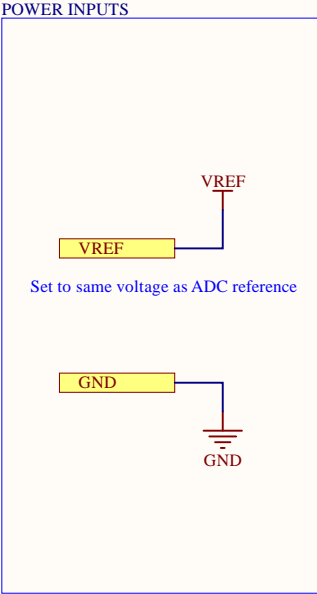
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| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |



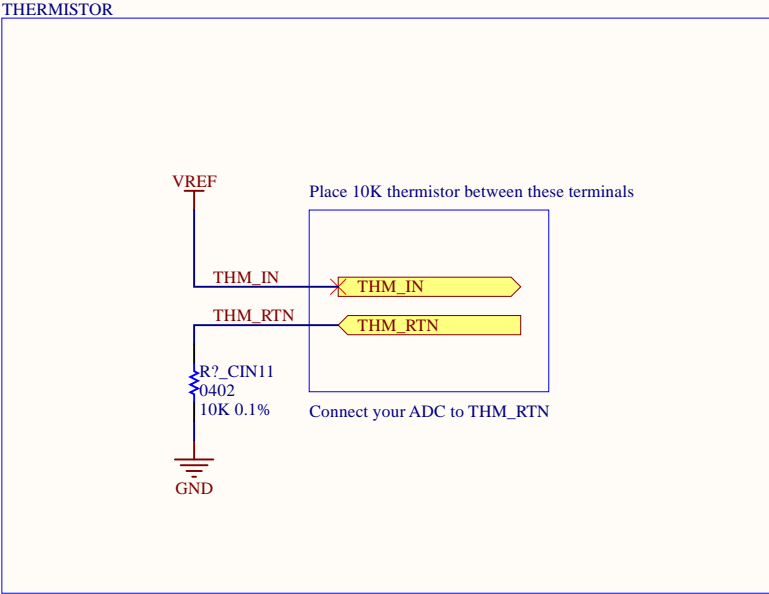
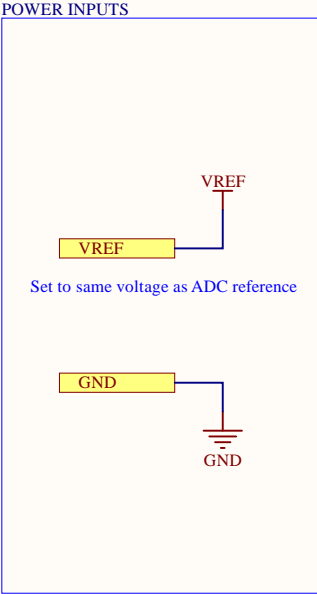
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| Title | | | |
| thermistor-input-10k.SchDoc | | | |
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| A4 | PCBS-COMMON | | 1.1 |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |



| Title | | |
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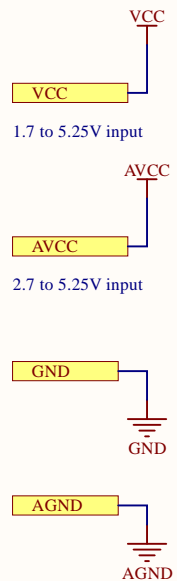


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| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |

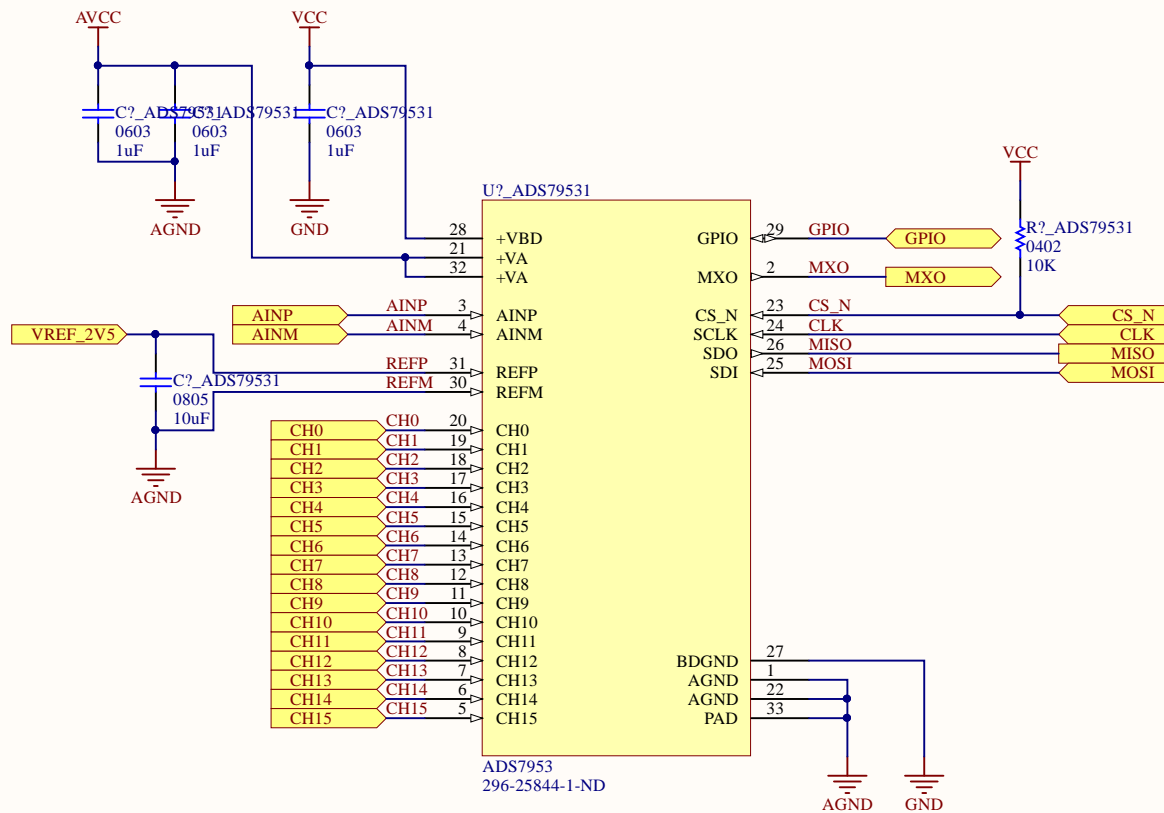


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| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\thermistor-input-10k.SchDoc | Drawn By: | B. Almeida, D. Vogel |

POWER INPUTS
AVCC >= VCC (pg 51)



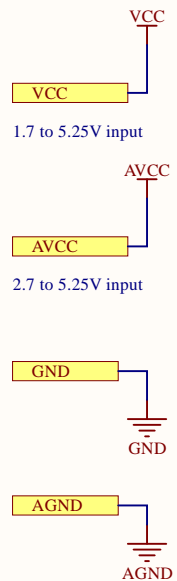
See pg 53, each +VA pin should have it's own 1uF



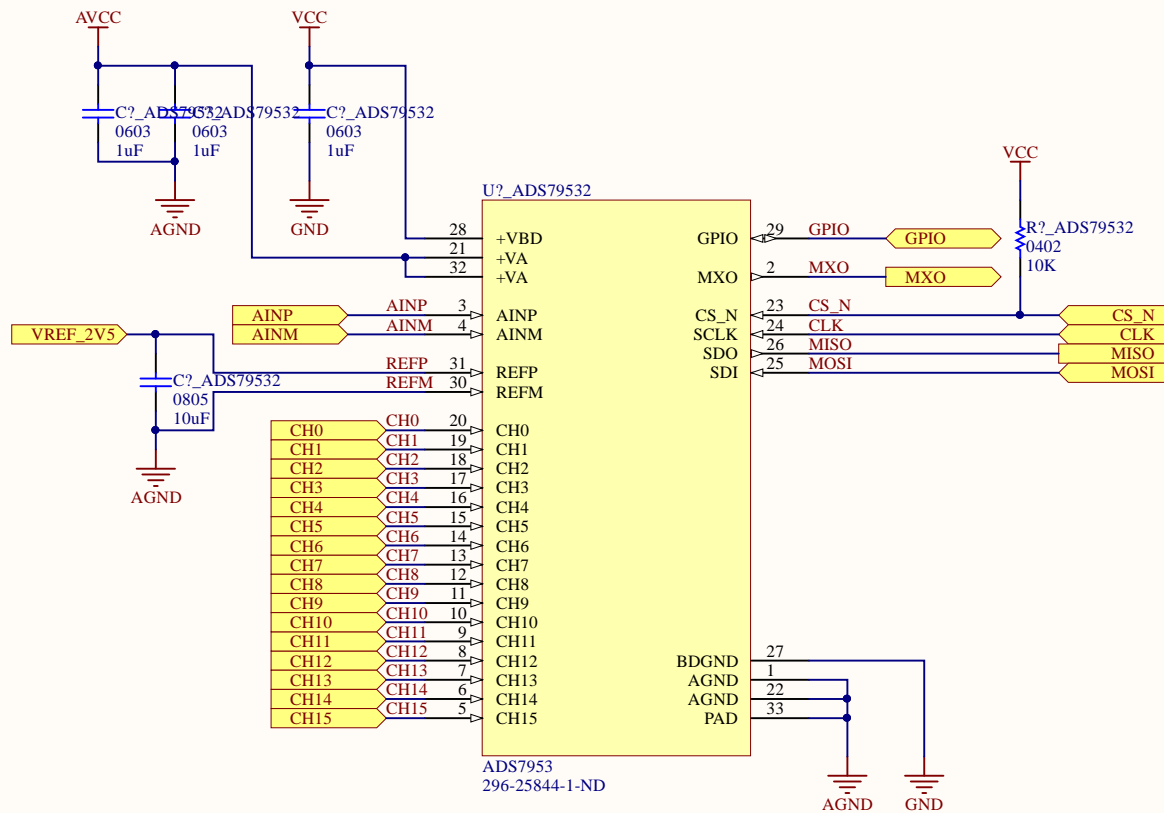
16 CHANNEL ADC

| | | | |
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| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\adc-ADS7953.SchDoc | Drawn By: | Dylan Vogel |

POWER INPUTS
AVCC >= VCC (pg 51)

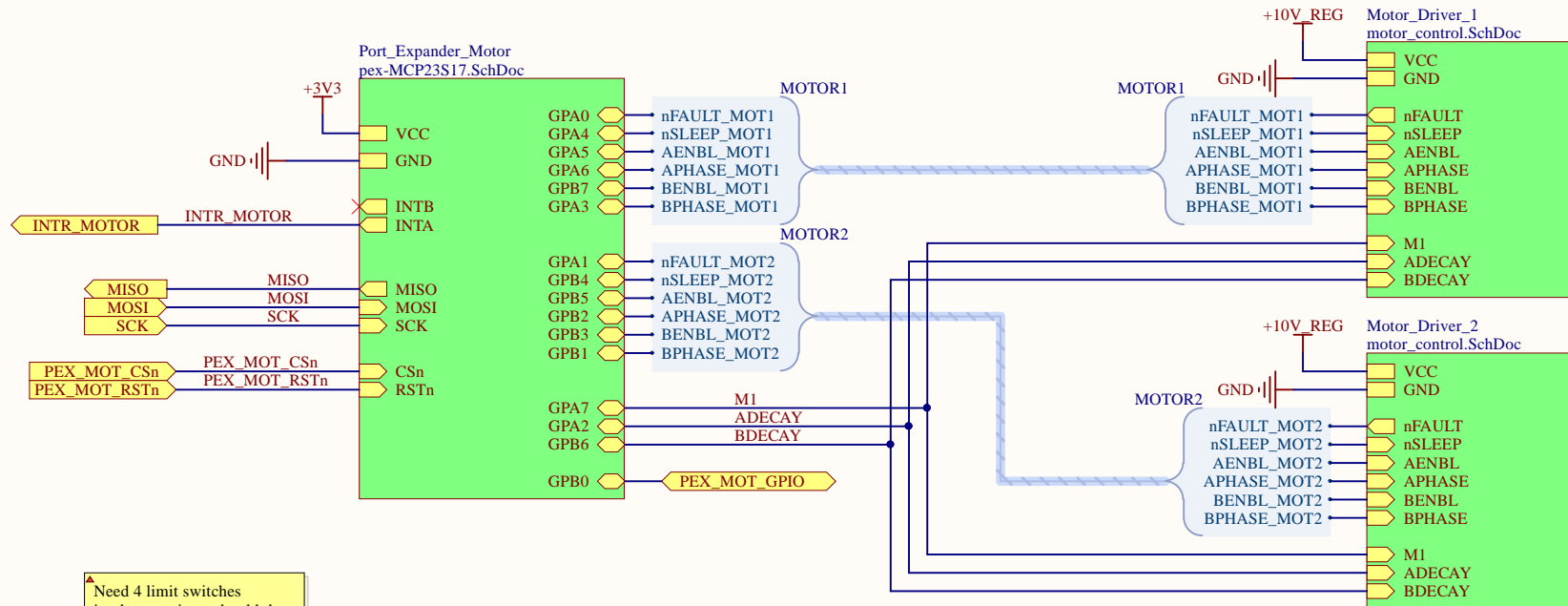


See pg 53, each +VA pin should have it's own 1uF

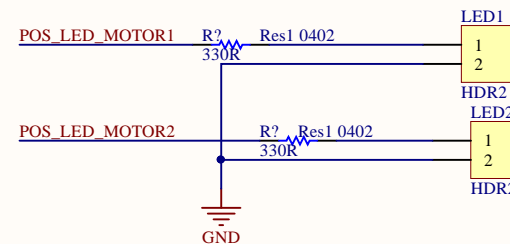
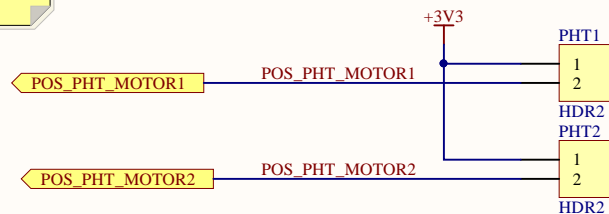


16 CHANNEL ADC

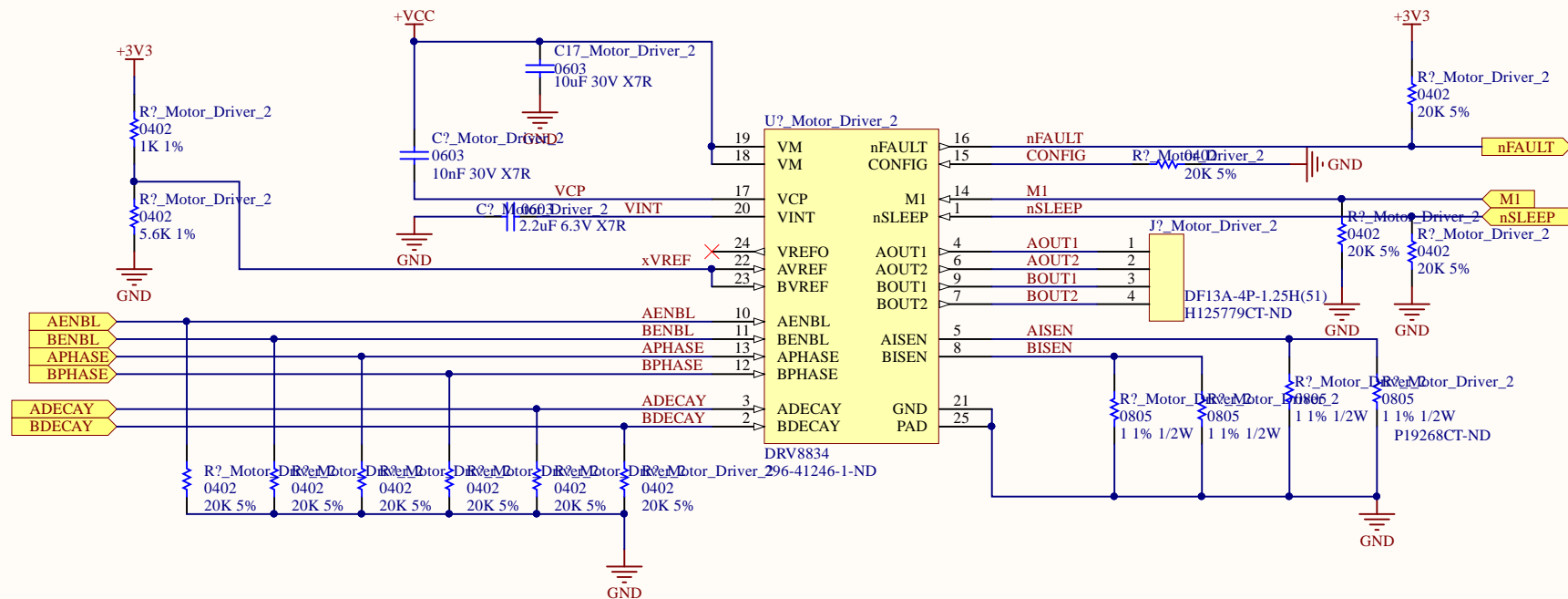
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| A4 | PCBS-COMMON | 1.1 | |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\adc-ADS7953.SchDoc | Drawn By: | Dylan Vogel |



Need 4 limit switches implementation - should they be MCU interrupt or some power cutting mechanism?



| | | | |
|-------|-------------------------------------|----------------|----------|
| Title | | pay-ssm.PrjPCB | |
| Size | Number | Revision | |
| A4 | | v1 | |
| Date: | 7/20/2019 | Sheet 3 | of 16 |
| File: | C:\Users\...\motors-overview.SchDoc | Drawn By: | Loma Lan |



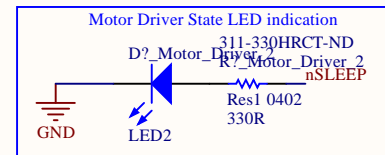
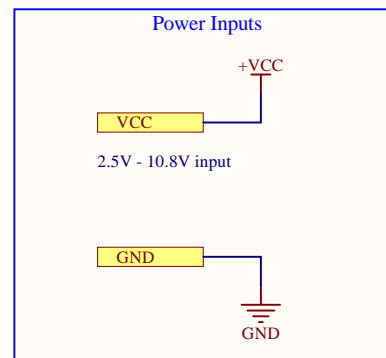
DRV8834 Motor Driver Notes

Datasheet: <http://www.ti.com/lit/ds/symlink/drv8834.pdf>

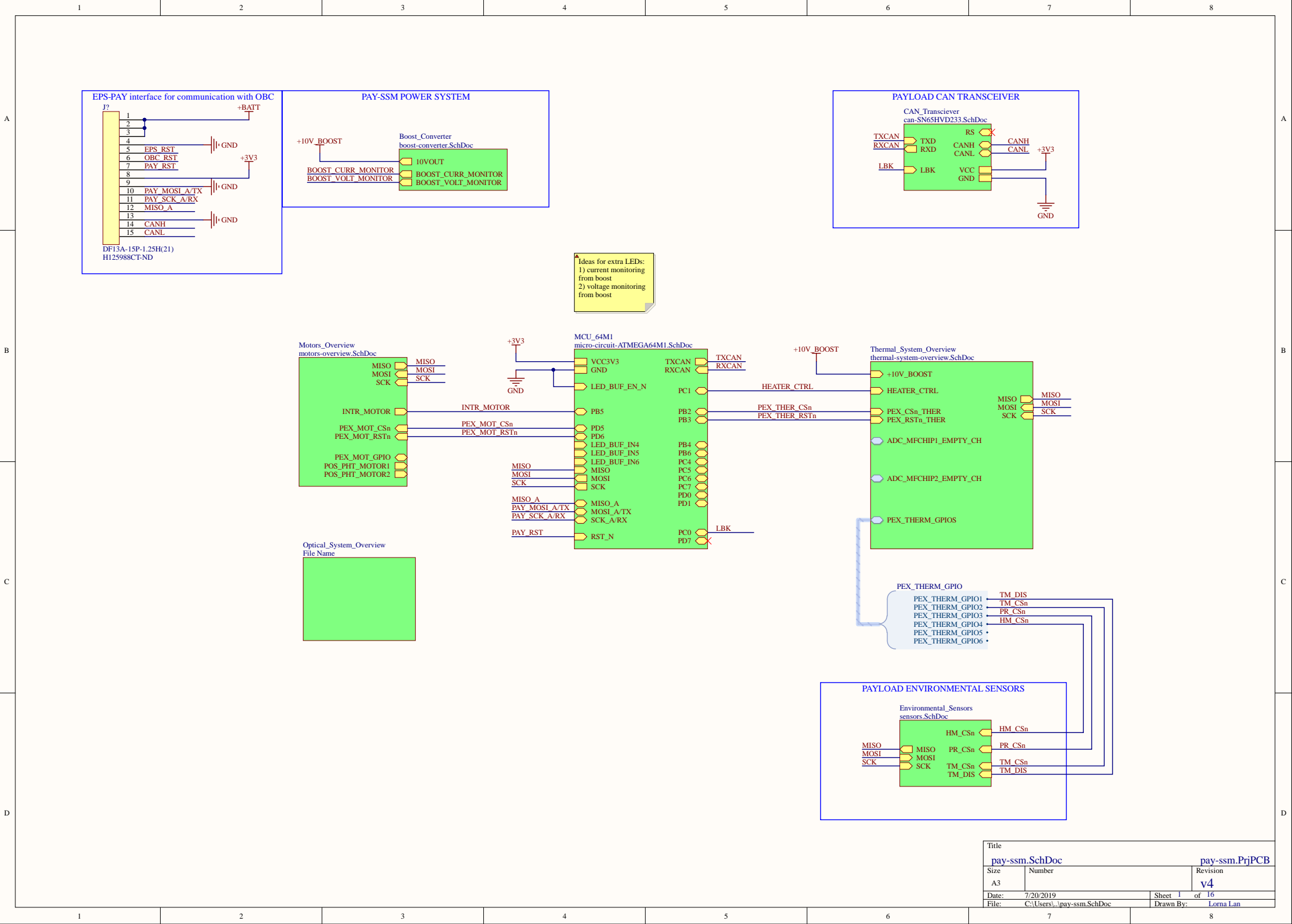
Indexer mode of this motor driver was tested to be not functioning, so everything is set in hardware to implement only the PHASE/ENABLE mode.

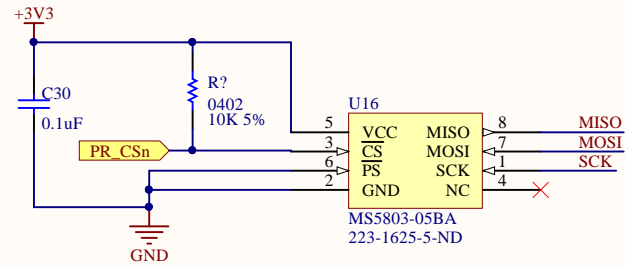
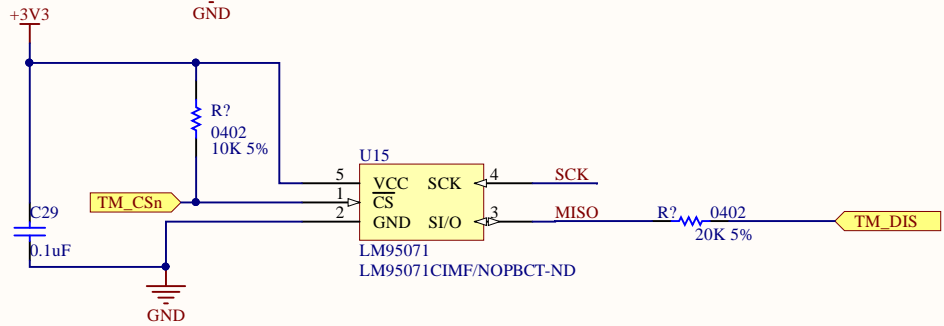
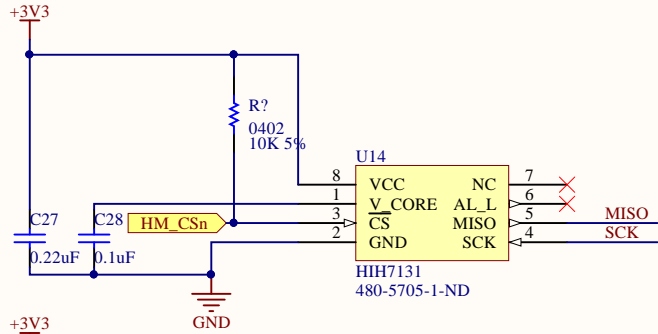
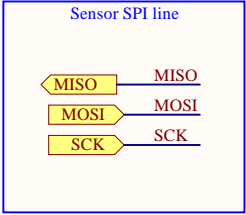
Implemented a voltage divider to set-up the xVREF voltage if want to modify xISEN and the resistor later. VREFO is left unconnected.

About decay settings: decay mode is selected by the voltage presented at the xDECAY pins in PHASE/ENABLE mode. It is also recommended with a pull-down to ground and a GPIO for setting.

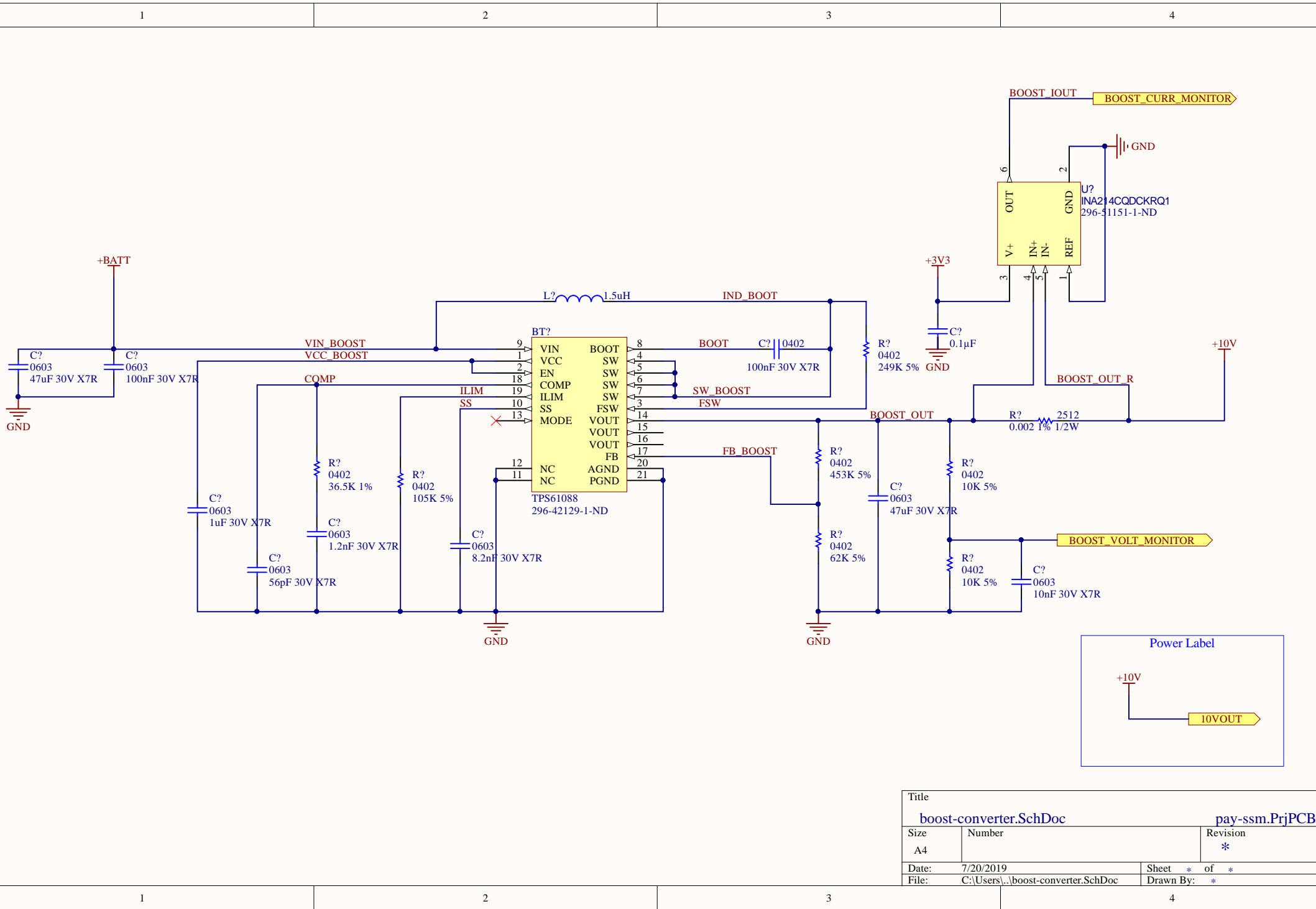


| | | |
|----------------------|-----------------------------------|----------------------------------|
| Title | | |
| motor_control.SchDoc | | pay-ssm.PrjPCB |
| Size | Number | Revision |
| A4 | | v2 |
| Date: | 7/20/2019 | Sheet 4 of 16 |
| File: | C:\Users\...\motor_control.SchDoc | Drawn By: Lorna Lan, Dylan Vogel |

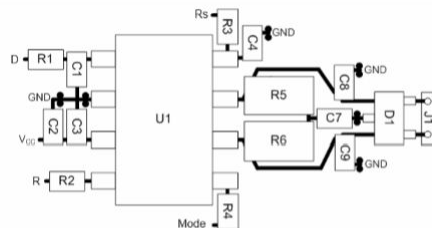
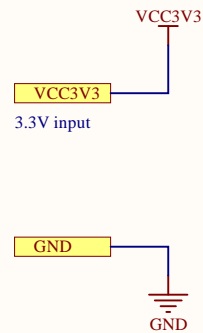




| | | | |
|-------|-----------------------------|----------------|------------------------|
| Title | | pay-ssm.PrjPCB | |
| Size | Number | Revision | |
| A4 | | v2 | |
| Date: | 7/20/2019 | Sheet 16 | of 16 |
| File: | C:\Users\...\sensors.SchDoc | Drawn By: | Lorna Lan, Dylan Vogel |



| | | |
|------------------------|-------------------------------------|----------------|
| Title | | |
| boost-converter.SchDoc | | pay-ssm.PrjPCB |
| Size | Number | Revision |
| A4 | | * |
| Date: | 7/20/2019 | Sheet * of * |
| File: | C:\Users\...\boost-converter.SchDoc | Drawn By: * |

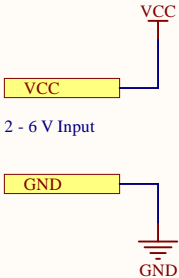


See pg. 28 of the datasheet for layout guidelines

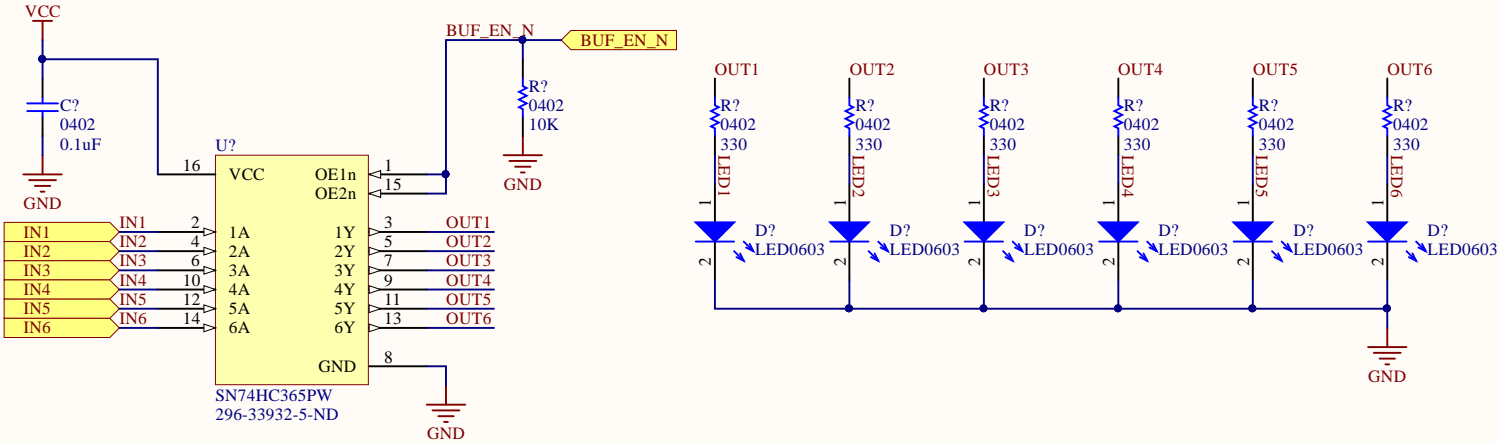
- Device is meant to be used in a 3.3 V system
- 100 Ohm current limiting resistors placed on the digital lines to minimize digital noise to the device
- Only two CAN transceivers on the bus should have 120 ohm terminations. Other devices should be placed on 'stub' networks where the terminations are left unsoldered

| | | |
|---------------------------------------------|---------------------------------|------------------------|
| Title can-SN65HVD233.SchDoc | | |
| Size A4 | Number PCBS-COMMON | Revision 1.2 |
| Date: 7/20/2019 | Sheet * of * | |
| File: C:\Users\...\can-SN65HVD233.SchDoc | Drawn By: Dylan Vogel | |

INPUT POWER



LED BUFFER

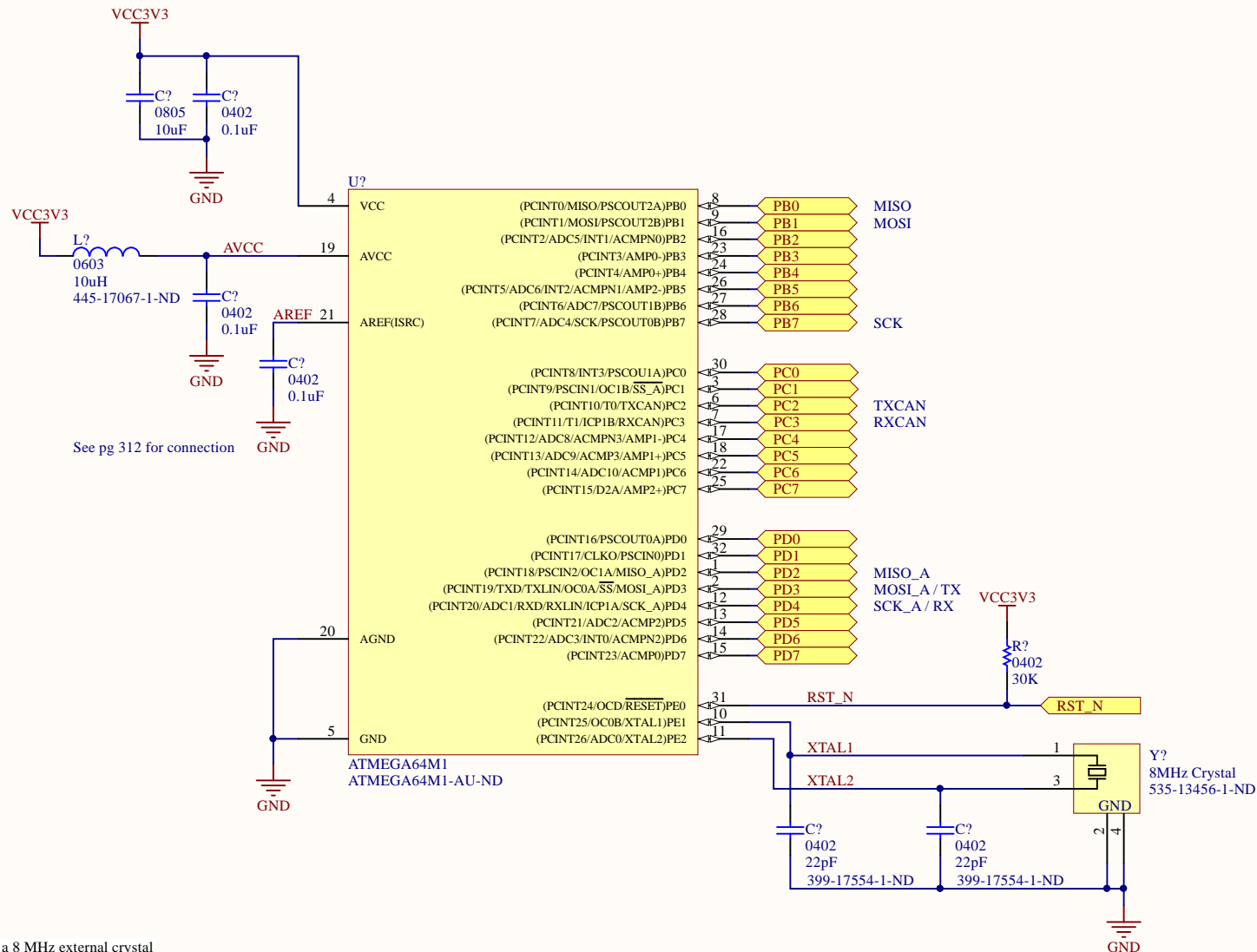
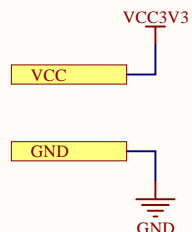


This schematic implements the SN74HC365PW non-inverting, tri-state hex buffer as an LED monitoring circuit. Connecting a signal to IN[1:6] will light up the corresponding LED on OUT[1:6].

- The BUF_EN_N input can be connected to a microcontroller to control the buffer. An input HIGH will set the outputs to high-impedance and disable the LEDs.
- In the schematic symbol which references this schematic sheet, parameters LED[1:6] can be added to specify the colour of each LED. See the micro-circuit common sheet for an example of this.
- Unconnected inputs should be grounded if you don't want random flickering of the LEDs.

| | | | |
|-----------------------------------|------------------------------------------------|----------|-------------|
| Title | | | |
| led-monitoring-SN74HC365PW.SchDoc | | | |
| Size | Number | Revision | |
| A4 | PCBS-COMMON | 1.1 | |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\led-monitoring-SN74HC365PW.SchDoc | By: | Dylan Vogel |

POWER INPUT



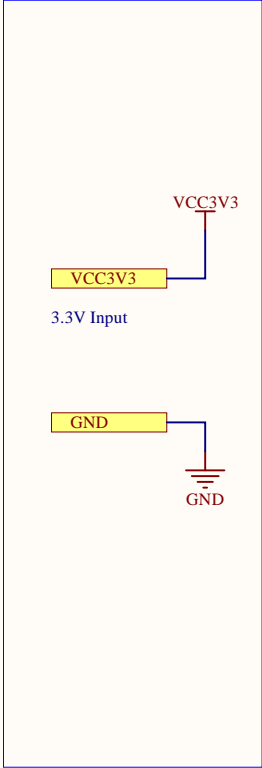
See pg 312 for connection

This schematic implements the ATMEGA64M1 microcontroller with a 8 MHz external crystal and necessary power connections.

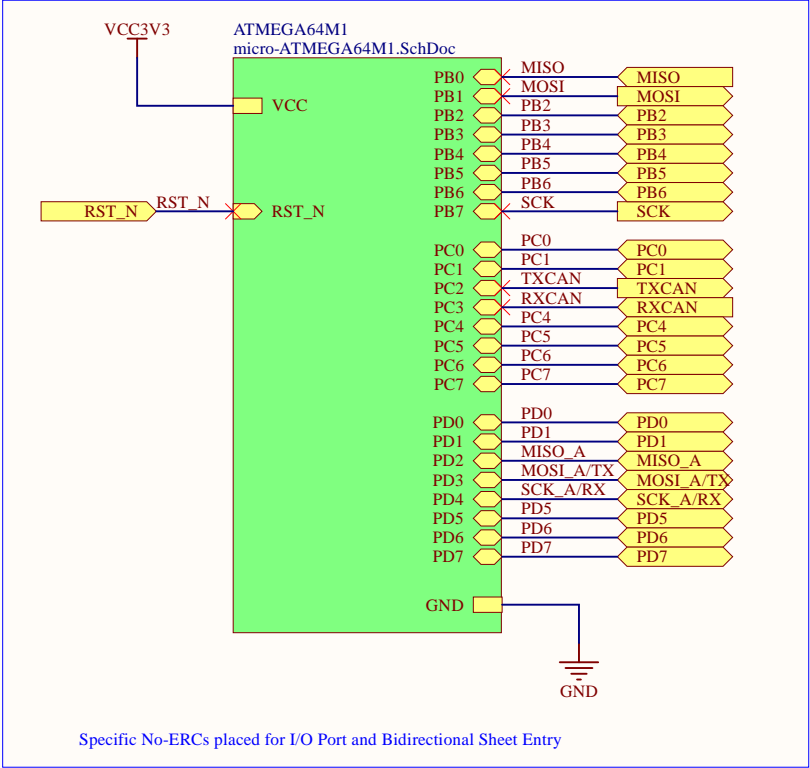
- Crystal is connected in a Pierce configuration, values of the capacitors were calculated based on the capacitance of the crystal and ESR.
- I would read through 18.5.2 and 18.6.2 of the complete 64M1 datasheet if you're interested in the motivation behind the ADC input connections. They recommend connecting AVCC through a RC lowpass network to minimize noise.
- If the ADC functionality of the device is used, either AVCC or the internal 2.56 V source can be selected in software as the reference voltage.

| | | | |
|-------------------------|------------------------------------------------------------|----------|------|
| Title | | | |
| micro-ATMEGA64M1.SchDoc | | | |
| Size | Number | Revision | |
| A4 | PCBS-COMMON | 1.1 | |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\micro-ATMEGA64M1.SchDoc Drawn By: Dylan Vogel | | |

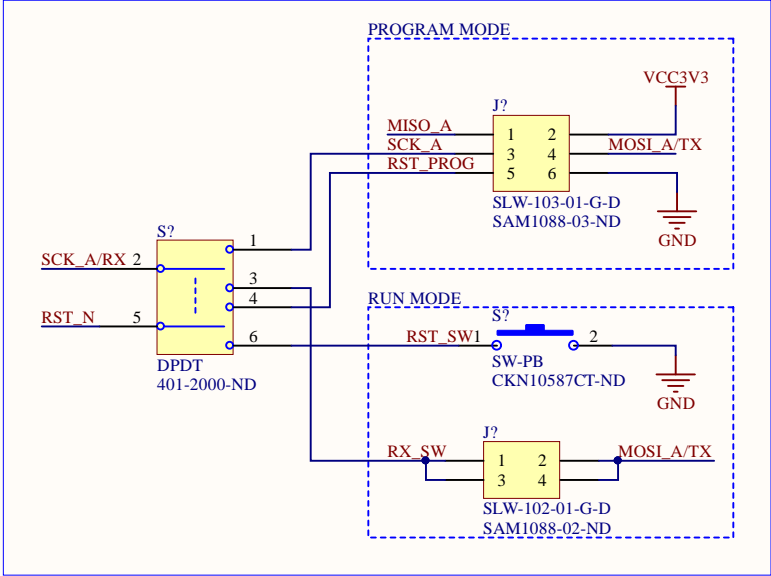
POWER INPUTS



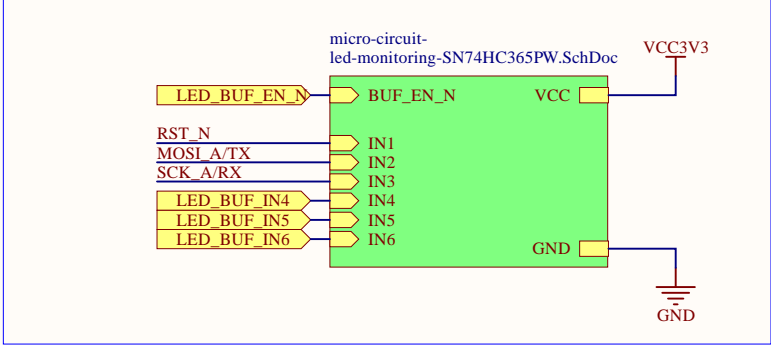
ATMEGA32M1



MODE SELECT CIRCUITRY



LED MONITORING

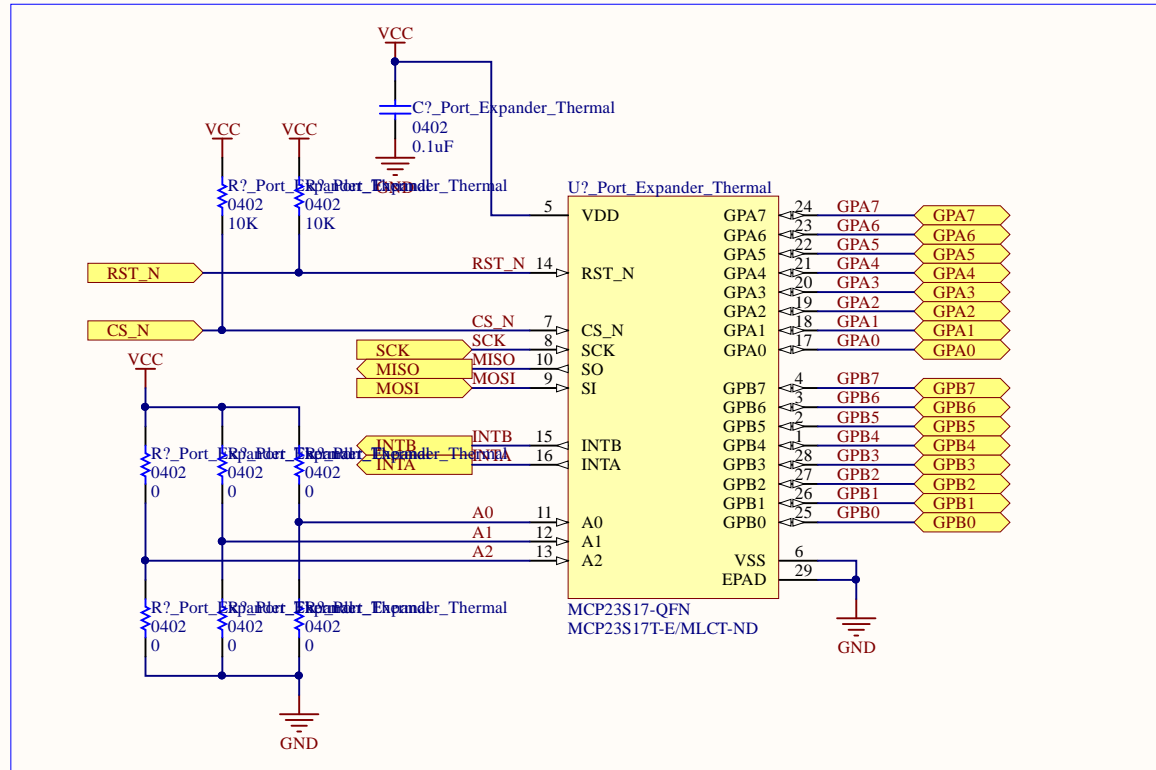
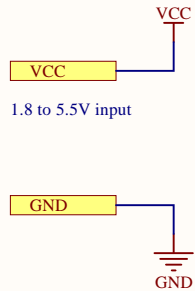


This schematic extends the functionality already included in the micro-ATMEGA32M1 schematic, adding a mode select switch, programming header, reset button and LED indication for TX, RX and RSTn.

- IN[4:6] of the LED buffer have been left unconnected, but are broken out on ports LED_BUF_IN[4:6]. They can be connected in the schematic which includes this sheet up to an additional 3 lines. Highly recommend more blinking lights.

| | | | |
|---------------------------------|----------------------------------------------|-----------|-------------|
| Title | | | |
| micro-circuit-ATMEGA64M1.SchDoc | | | |
| Size | Number | Revision | |
| A4 | PCBS-COMMON | 1.1 | |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\micro-circuit-ATMEGA64M1.SchDoc | Drawn By: | Dylan Vogel |

POWER INPUTS



ADDRESS:

CHANNEL SELECTION

ONLY SOLDER ONE 0 OHM FROM EACH PAIR
 PEX ADDRESS = A2 A1 A0
 VCC == 1 GND == 0

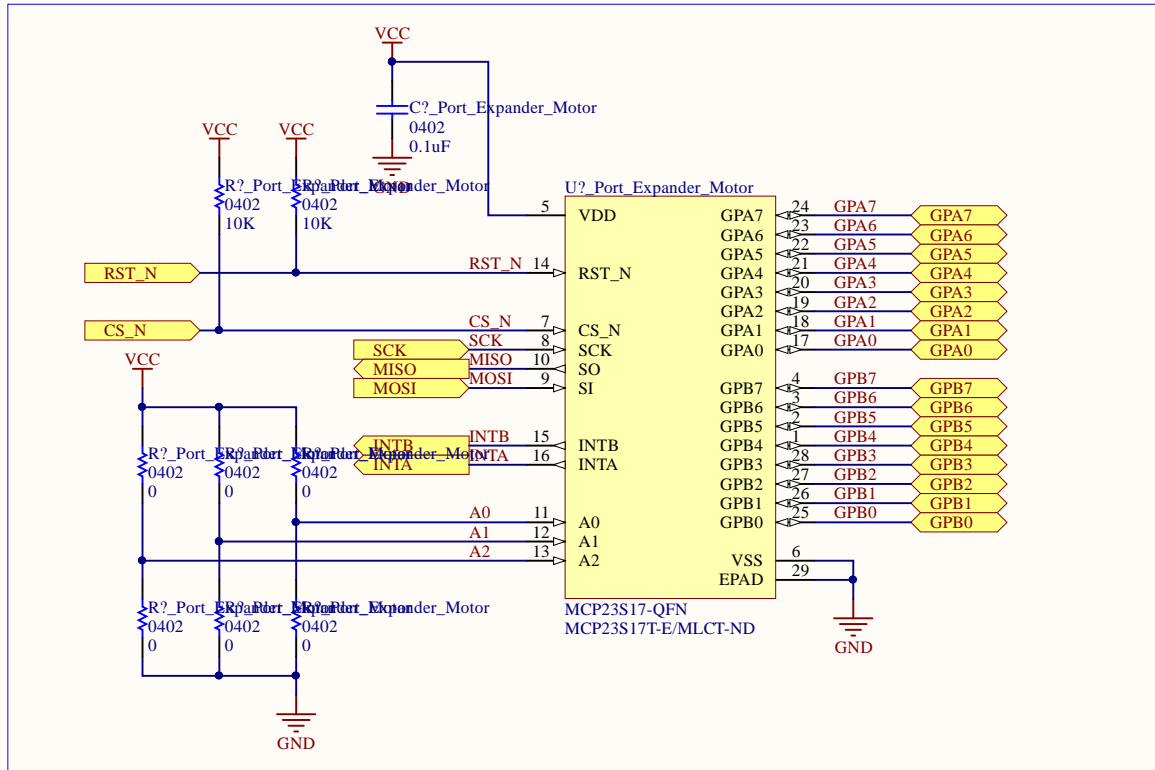
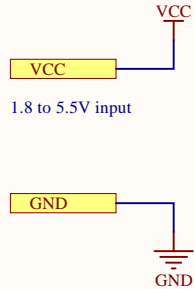
This schematic implements the MCP23S17 SPI port expander, and does some common-sense things like adding a bypass capacitor to the power supply and pull-up resistors to RST_N and CS_N.

Multiple port expanders can be connected to the same CS_N line, and accessed via a device address that is used during software communication. This address is set in hardware via the A2, A1 and A0 pins. Soldering a 0 ohm resistor to VCC will set that bit to 1, and soldering to GND will set that bit to 0.

In the schematic which includes this file, you should make some note of the relevant hardware address that should be soldered during manufacturing.

| | | | |
|---------------------|----------------------------------|-----------|-------------|
| Title | | | |
| pex-MCP23S17.SchDoc | | | |
| Size | Number | | Revision |
| A4 | PCBS-COMMON | | 1.1 |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\pex-MCP23S17.SchDoc | Drawn By: | Dylan Vogel |

POWER INPUTS



ADDRESS:

CHANNEL SELECTION

ONLY SOLDER ONE 0 OHM FROM EACH PAIR
PEX ADDRESS = A2 A1 A0
VCC == 1 GND == 0

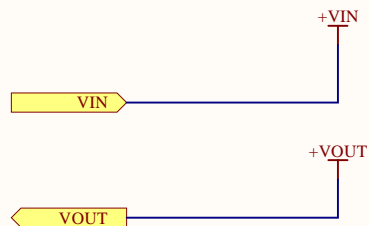
This schematic implements the MCP23S17 SPI port expander, and does some common-sense things like adding a bypass capacitor to the power supply and pull-up resistors to RST_N and CS_N.

Multiple port expanders can be connected to the same CS_N line, and accessed via a device address that is used during software communication. This address is set in hardware via the A2, A1 and A0 pins. Soldering a 0 ohm resistor to VCC will set that bit to 1, and soldering to GND will set that bit to 0.

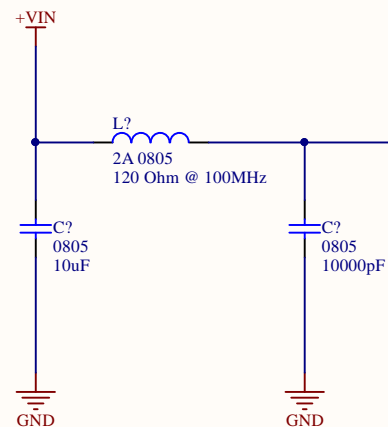
In the schematic which includes this file, you should make some note of the relevant hardware address that should be soldered during manufacturing.

| | | | |
|---------------------|----------------------------------|-----------|-------------|
| Title | | | |
| pex-MCP23S17.SchDoc | | | |
| Size | Number | | Revision |
| A4 | PCBS-COMMON | | 1.1 |
| Date: | 7/20/2019 | Sheet * | of * |
| File: | C:\Users\...\pex-MCP23S17.SchDoc | Drawn By: | Dylan Vogel |

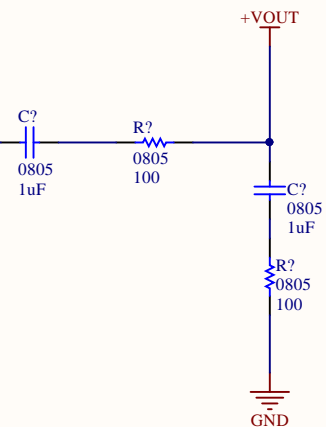
POWER PORTS



PI- FILTER



HIGH/LOW-PASS FILTER



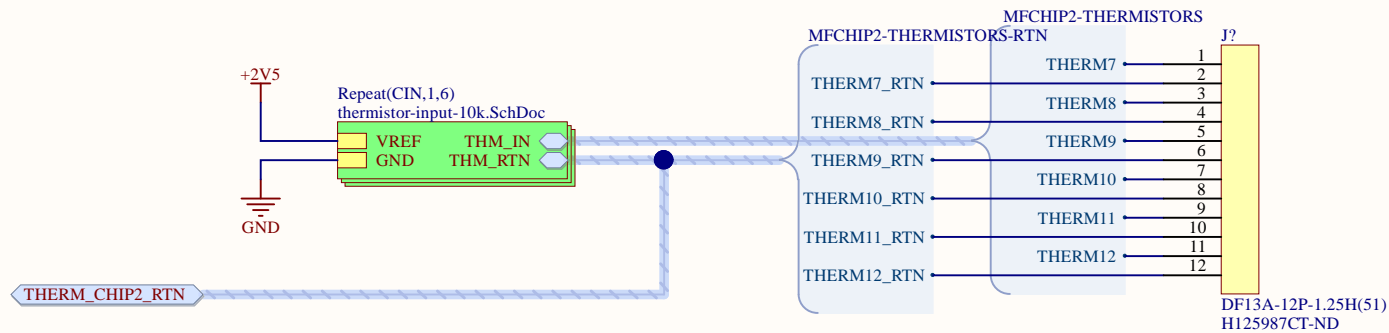
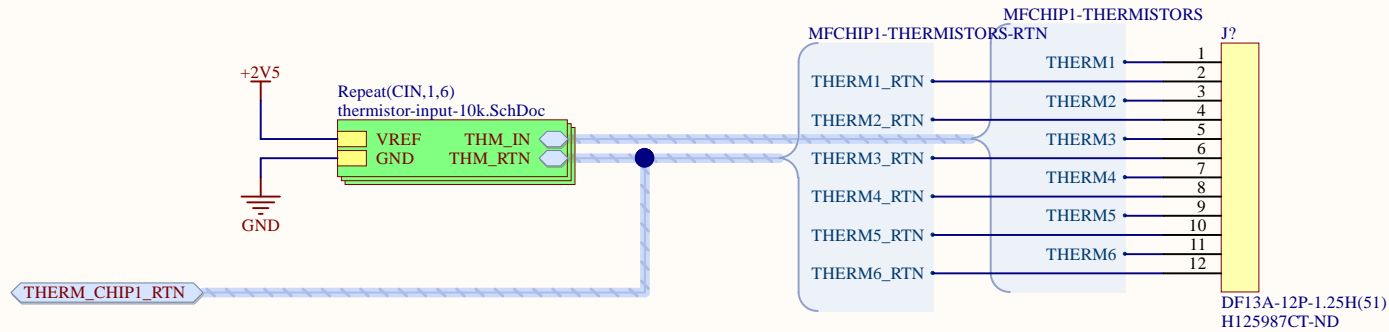
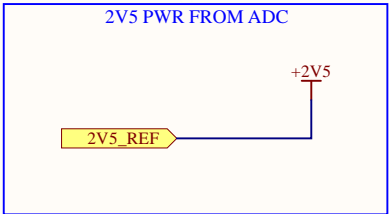
▲ **LOW-PASS FILTER:**
1) Place resistor on the horizontal line ONLY
2) Place capacitor on the vertical line ONLY

Other blanks fill in with 0 ohms jumper resistor

HIGH-PASS FILTER:
1) Place capacitor on the horizontal line ONLY
2) Place resistor on the vertical line ONLY

Other blanks fill in with 0 ohms jumper resistor

| Title | | | |
|-------|-------------------------------------|--|-----------|
| Size | Number | | Revision |
| A4 | | | |
| Date: | 7/20/2019 | | Sheet of |
| File: | C:\Users\...\power-filtering.SchDoc | | Drawn By: |



| Title | | | |
|-------|--------------------------------------------|-------|----------|
| Size | Number | | Revision |
| A4 | | | |
| Date: | 7/20/2019 | Sheet | of |
| File: | C:\Users\...\thermistors-connectors.SchDoc | | |