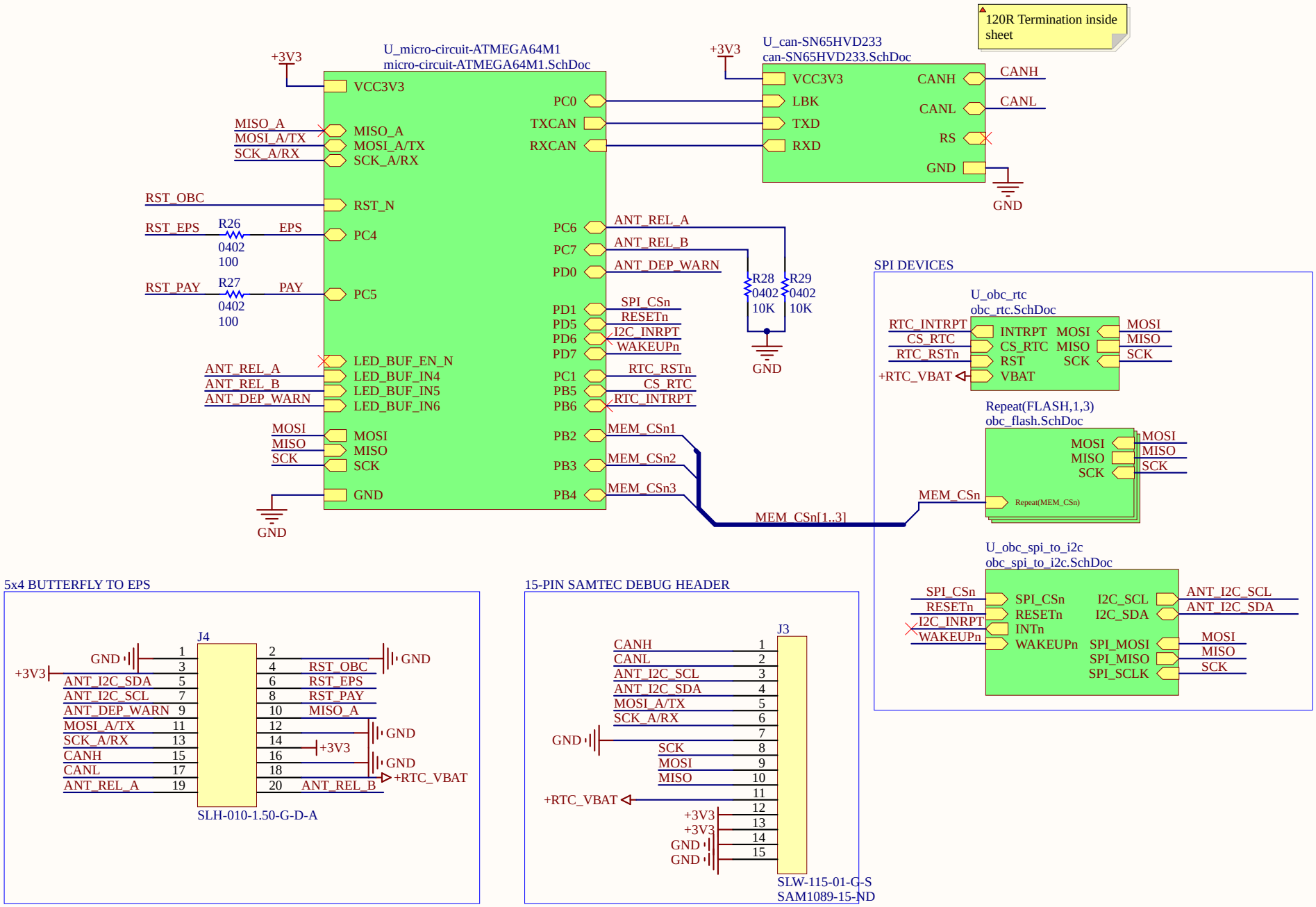
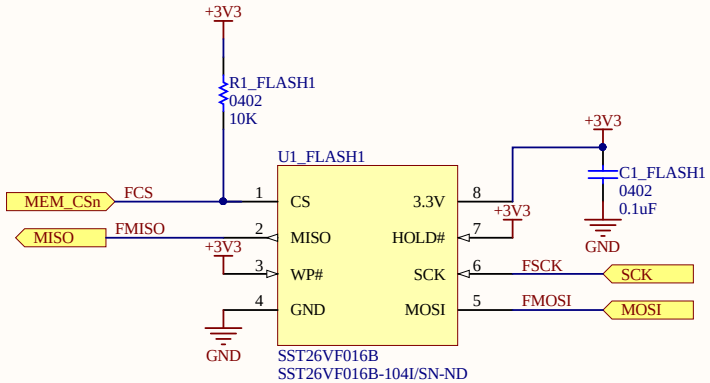
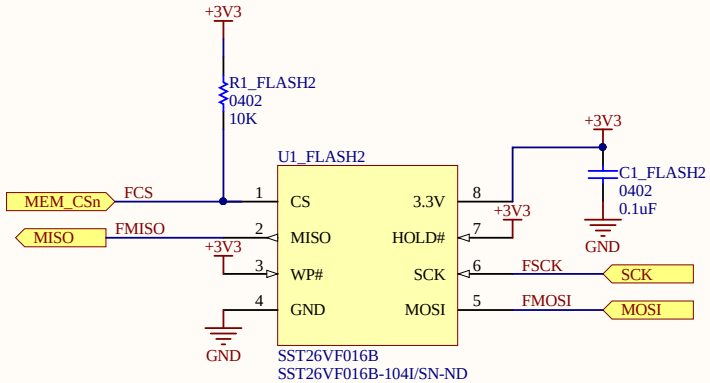
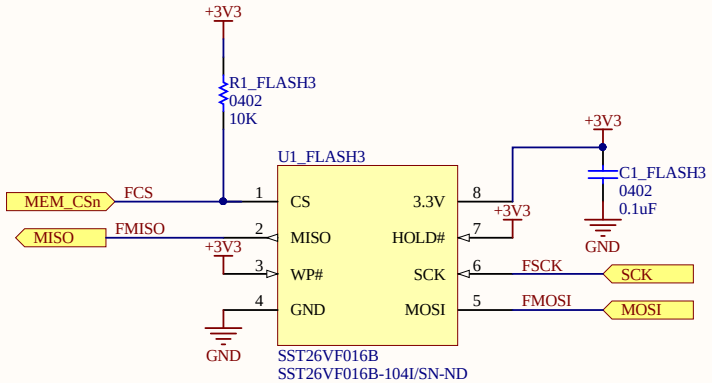

120R Termination inside sheet
U_micro-circuit-ATMEGA64M1
micro-circuit-ATMEGA64M1.SchDoc
+3V3
VCC3V3
MISO_A
MOSI_A/TX
SCK_A/RX
RST_OBC
RST_N
RST_EPS
R26
0402
100
EPS
PC4
RST_PAY
R27
0402
100
PAY
PC5
ANT_REL_A
ANT_REL_B
ANT_DEP_WARN
LED_BUF_EN_N
LED_BUF_IN4
LED_BUF_IN5
LED_BUF_IN6
MOSI
MISO
SCK
GND
PC0
TXCAN
RXCAN
PC6
PC7
PD0
PD1
PD5
PD6
PD7
PC1
PB5
PB6
PB2
PB3
PB4
SPI_CSn
RESETn
I2C_INRPT
WAKEUPn
RTC_RSTn
CS_RTC
RTC_INTRPT
MEM_CSn1
MEM_CSn2
MEM_CSn3
R28
0402
10K
R29
0402
10K
U_can-SN65HVD233
can-SN65HVD233.SchDoc
VCC3V3
LBK
TXD
RXD
RS
GND
CANH
CANL
SPI DEVICES
U_obc_rtc
obc_rtc.SchDoc
RTC_INTRPT
CS_RTC
RTC_RSTn
+RTC_VBAT
INTRPT
CS_RTC
RST
VBAT
MOSI
MISO
SCK
Repeat(FLASH,1,3)
obc_flash.SchDoc
MEM_CSn
Repeat(MEM_CSn)
MEM_CSn[1..3]
U_obc_spi_to_i2c
obc_spi_to_i2c.SchDoc
SPI_CSn
RESETn
I2C_INRPT
WAKEUPn
INTn
I2C_SCL
I2C_SDA
SPI_MOSI
SPI_MISO
SPI_SCLK
ANT_I2C_SCL
ANT_I2C_SDA
5x4 BUTTERFLY TO EPS
J4
GND
+3V3
ANT_I2C_SDA
ANT_I2C_SCL
ANT_DEP_WARN
MOSI_A/TX
SCK_A/RX
CANH
CANL
ANT_REL_A
RST_OBC
RST_EPS
RST_PAY
MISO_A
+RTC_VBAT
ANT_REL_B
SLH-010-1.50-G-D-A
15-PIN SAMTEC DEBUG HEADER
J3
SLW-115-01-G-S
SAM1089-15-ND
Title
OBC Main
UTAT SS
Size
A
Number
1
Revision
1.0
Date:
9/3/2019
Sheet 1 of 8
File:
C:\Users\..\obc_main.SchDoc
Drawn By:
Mohamed Hirole



Title: Flash Memory		UTAT SS
Size: A4	Number: 2	Revision: 2.0
Date: 9/3/2019		Sheet 2 of 8
File: C:\Users\..\obc_flash.SchDoc		Drawn By: Mohamed Hirole

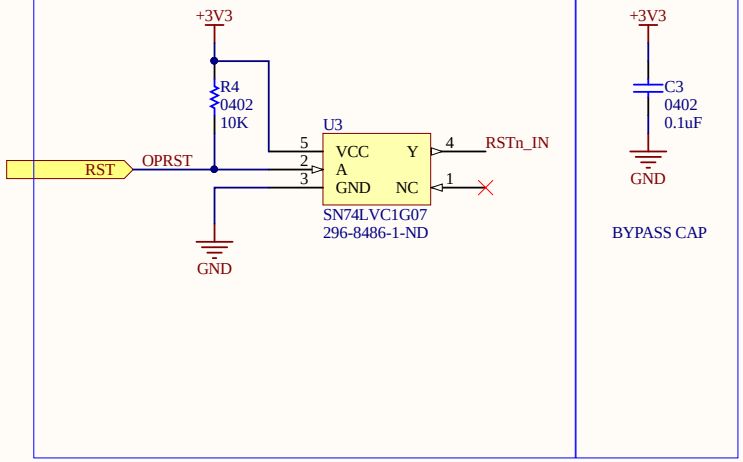


Title: Flash Memory		UTAT SS
Size: A4	Number: 2	Revision: 2.0
Date: 9/3/2019		Sheet 2 of 8
File: C:\Users\..\obc_flash.SchDoc		Drawn By: Mohamed Hirole

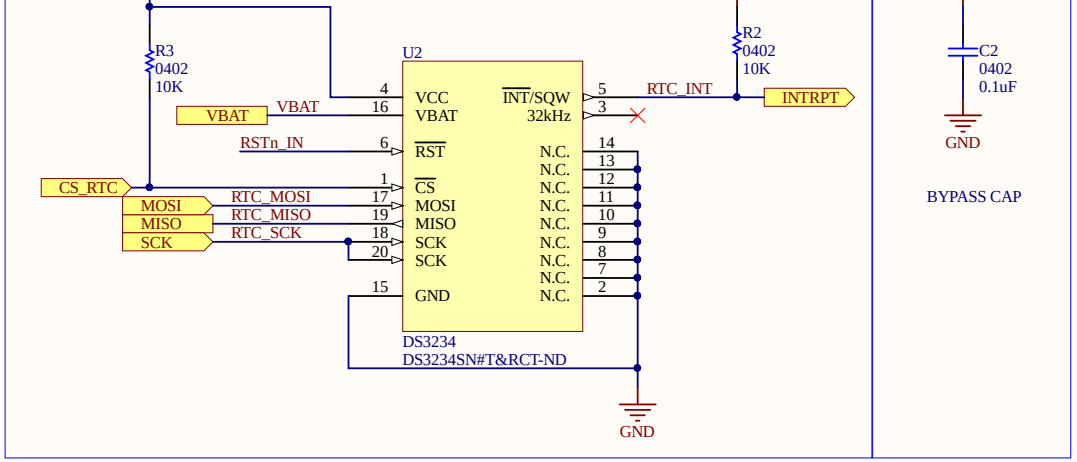


Title: Flash Memory		UTAT SS
Size: A4	Number: 2	Revision: 2.0
Date: 9/3/2019		Sheet 2 of 8
File: C:\Users\..\obc_flash.SchDoc		Drawn By: Mohamed Hirole

OPEN DRAIN RST BUFFER

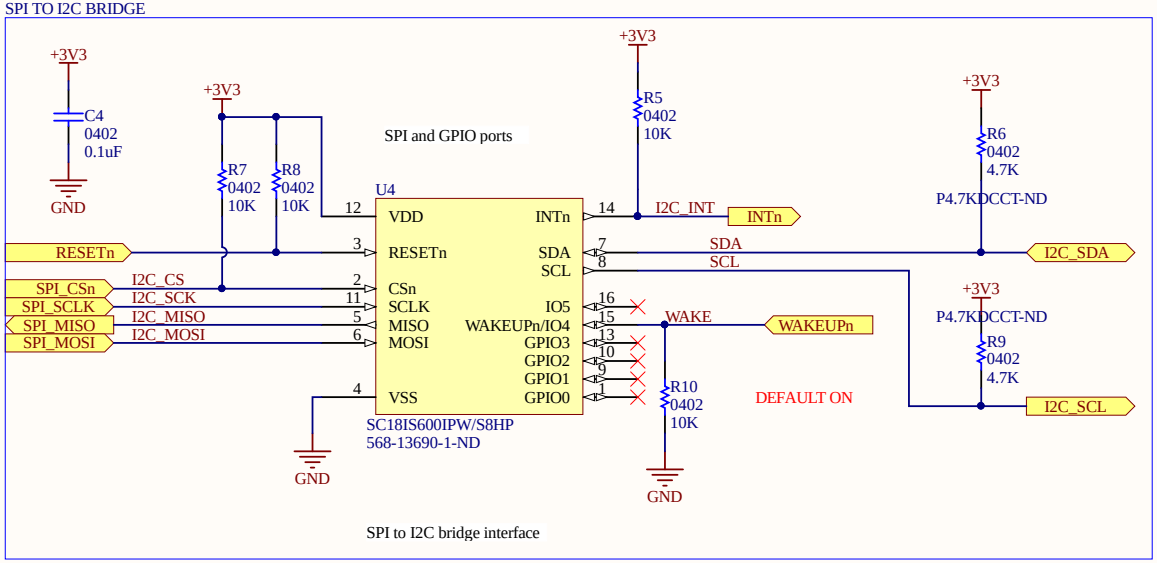


RTC



Title: Real Time Clock		UTAT SS
Size: A4	Number: 3	Revision: 2.0
Date: 9/3/2019		Sheet 3 of 8
File: C:\Users\..\obc_rtc.SchDoc		Drawn By: Mohamed Hirole

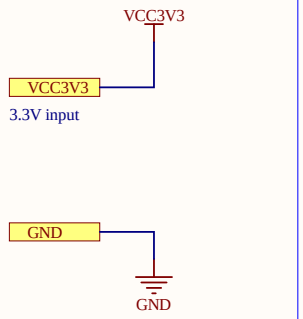
SPI TO I2C BRIDGE

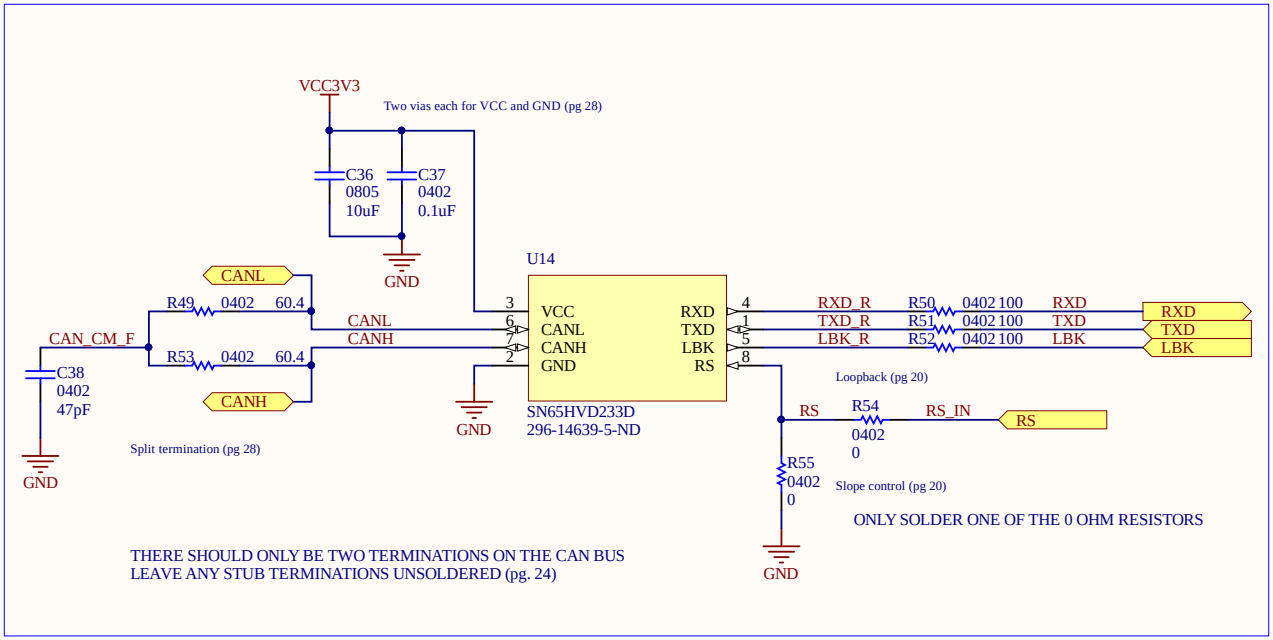


3.3V I2C signals

Title	SPI to I2C Bridge		UTAT SS
Size	Number		Revision
A4	4		1.0
Date:	9/3/2019	Sheet 4 of 8	
File:	C:\Users\..\obc_spi_to_i2c.SchDoc	Drawn By:	Mohamed Hirole

POWER INPUT





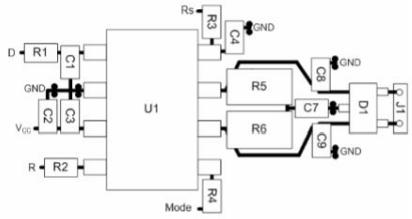


Figure 41. Layout Example Schematic

See pg. 28 of the datasheet for layout guidelines

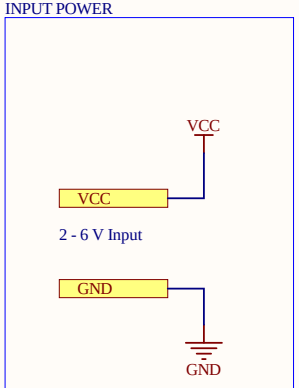
This schematic implements the SN65HVD233 CAN transciever with loopback control and two options for slope control.

A 0 Ohm resistor can be soldered to GND to permanently put the device in high speed mode (20 V / us slew), or a 0 Ohm resistor can be soldered to the RS port to control the device via an external microcontroller. Connecting the RS pin to a microcontroller allows the device to be put into low-power mode by setting the RS pin high.

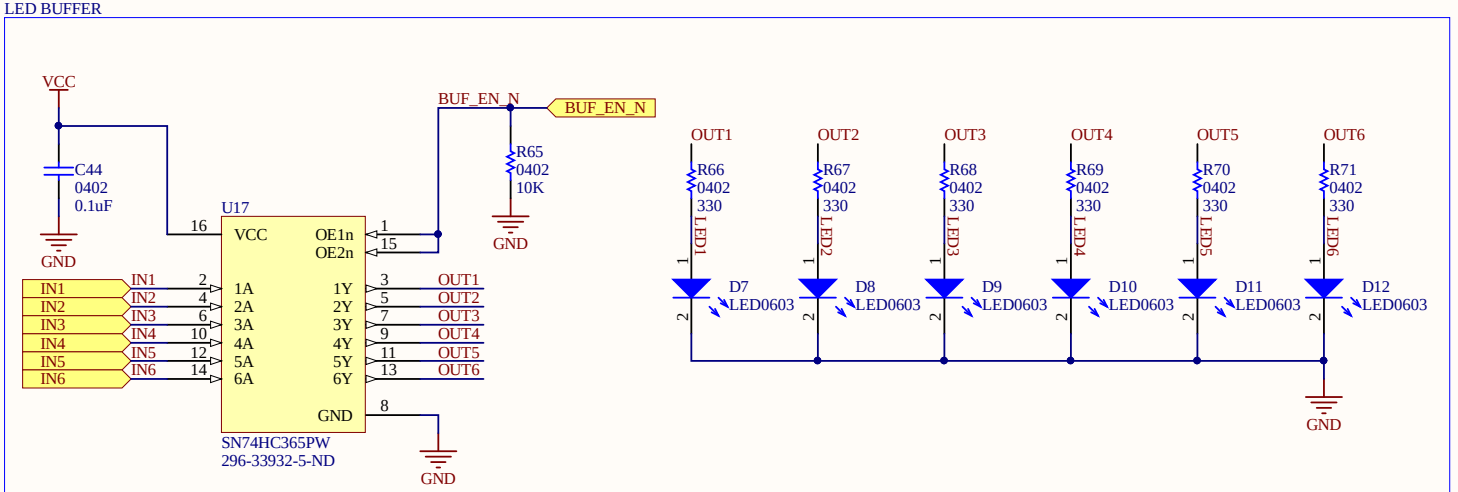
- Device is meant to be used in a 3.3 V system
- 100 Ohm current limiting resistors placed on the digital lines to minimize digital noise to the device
- Only two CAN transcievers on the bus should have 120 ohm terminations. Other devices should be placed on 'stub' networks where the terminations are left unsoldered

Title	can-SN65HVD233.SchDoc	
Size: A4	Number: PCBS-COMMON	Revision: 1.2
Date: 9/3/2019	Sheet * of *	
File: C:\Users\..\can-SN65HVD233.SchDoc	Drawn By: Dylan Vogel	

INPUT POWER



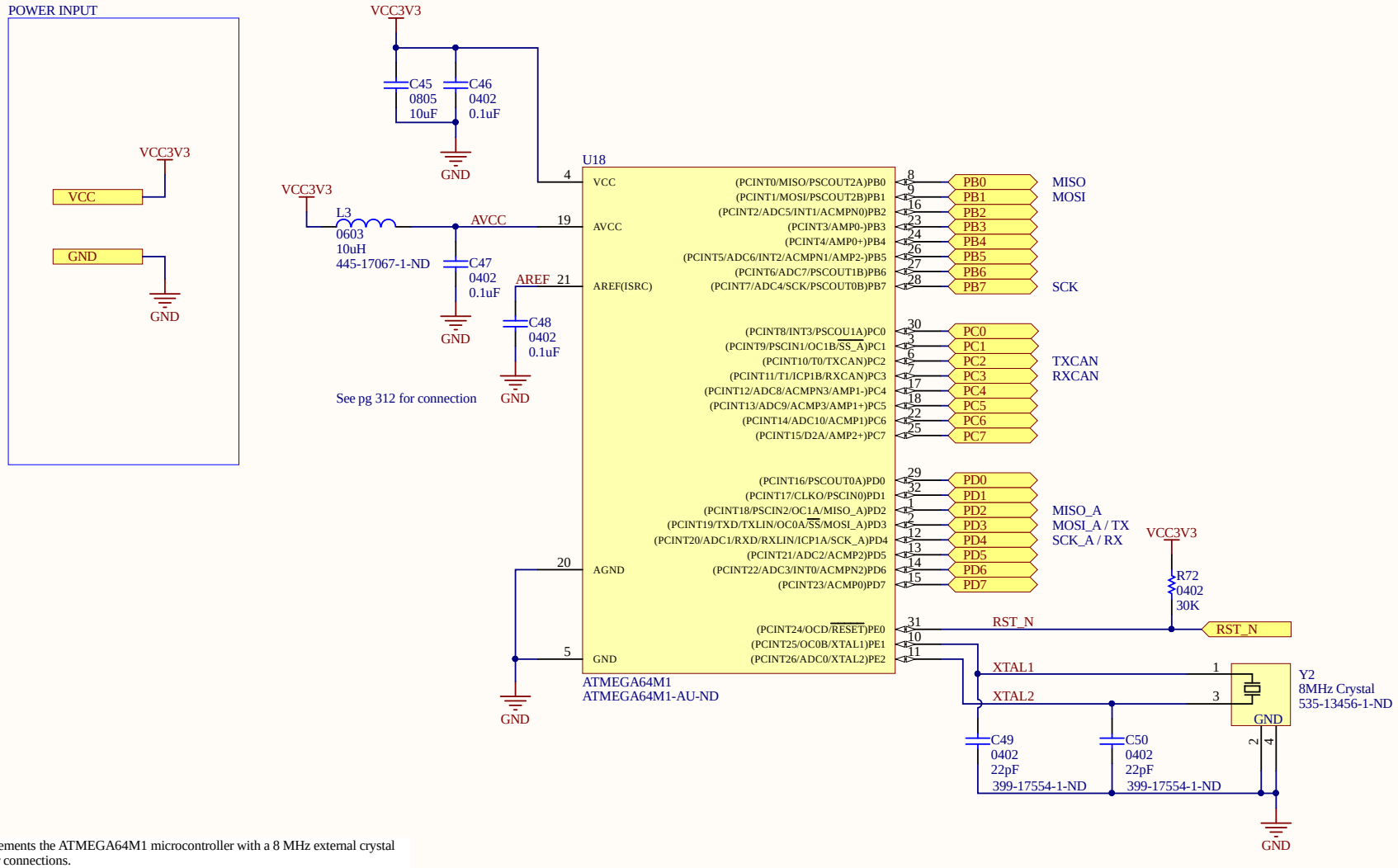
LED BUFFER



This schematic implements the SN74HC365PW non-inverting, tri-state hex buffer as an LED monitoring circuit. Connecting a signal to IN[1:6] will light up the corresponding LED on OUT[1:6].

- The BUF_EN_N input can be connected to a mircocontroller to control the buffer. An input HIGH will set the outputs to high-impedance and disable the LEDs.
- In the schematic symbol which references this schematic sheet, parameters LED[1:6] can be added to specify the colour of each LED. See the micro-circuit common sheet for an example of this.
- Unconnected inputs should be grounded if you don't want random flickering of the LEDs.

Title	led-monitoring-SN74HC365PW.SchDoc		
Size	Number		Revision
A4	PCBS-COMMON		1.1
Date:	9/3/2019	Sheet * of *	
File:	C:\Users\..\led-monitoring-SN74HC365PW.SchDoc	Drawn By:	Dylan Vogel

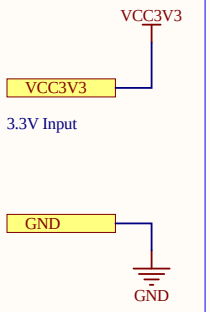


This schematic implements the ATMEGA64M1 microcontroller with a 8 MHz external crystal and necessary power connections.

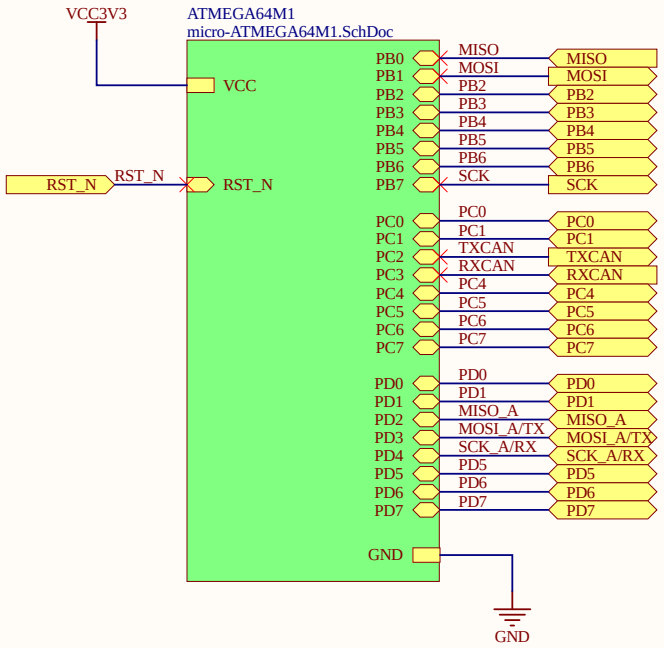
- Crystal is connected in a Pierce configuration, values of the capacitors were calculated based on the capacitance of the crystal and ESR.
- I would read through 18.5.2 and 18.6.2 of the complete 64M1 datasheet if you're interested in the motivation behind the ADC input connections. They recommend connecting AVCC through a RC lowpass network to minimize noise.
- If the ADC functionality of the device is used, either AVCC or the internal 2.56 V source can be seleted in software as the reference voltage.

Title	micro-ATMEGA64M1.SchDoc		
Size	Number		Revision
A4	PCBS-COMMON		1.1
Date:	9/3/2019	Sheet *	of *
File:	C:\Users\..\micro-ATMEGA64M1.SchDoc	Drawn By:	Dylan Vogel

POWER INPUTS

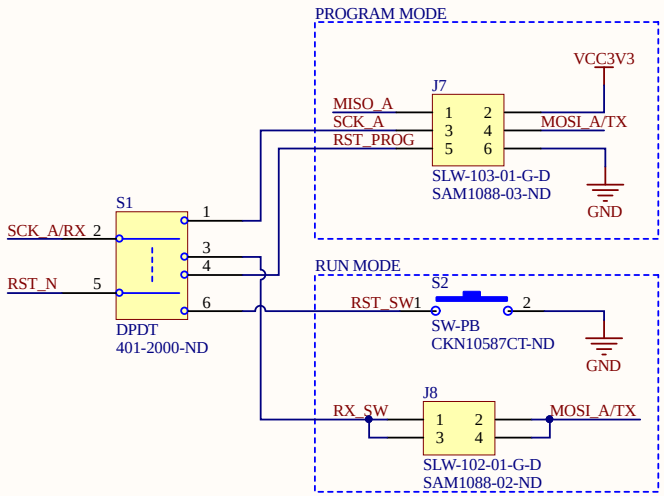


ATMEGA32M1

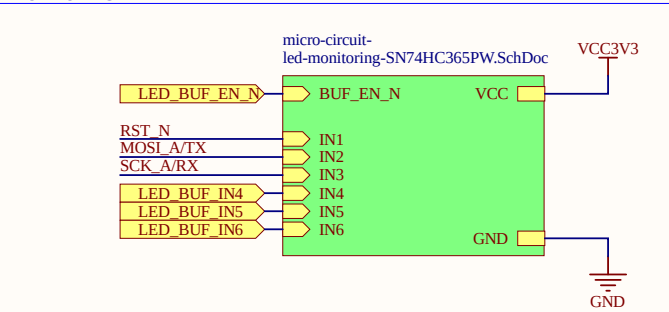


Specific No-ERCs placed for I/O Port and Bidirectional Sheet Entry

MODE SELECT CIRCUITRY



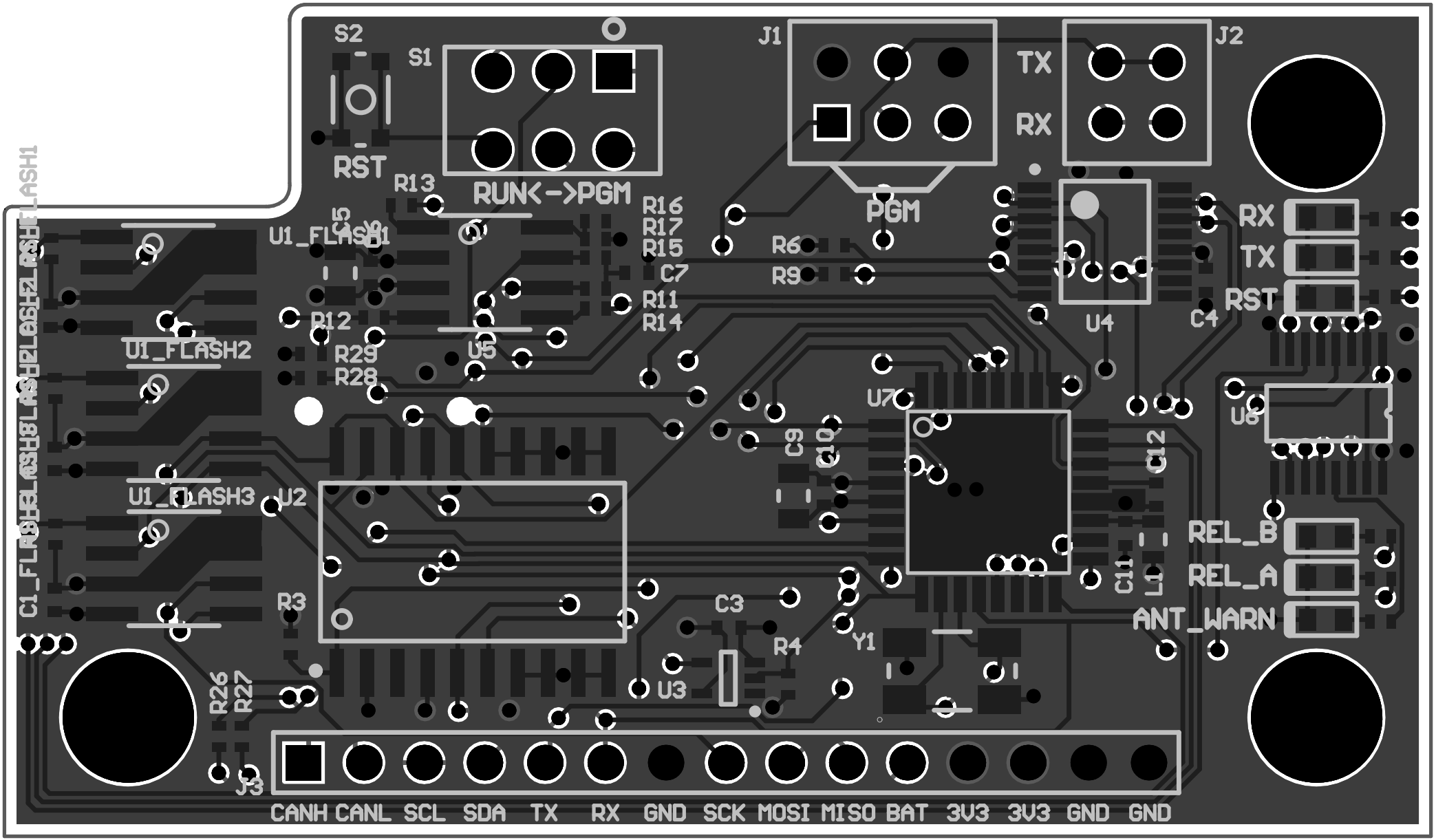
LED MONITORING



This schematic extends the functionality already included in the micro-ATMEGA32M1 schematc, adding a mode select switch, programming header, reset button and LED indication for TX, RX and RSTn.

- IN[4:6] of the LED buffer have been left unconnected, but are broken out on ports LED_BUF_IN[4:6]. They can be connected in the schematic which includes this sheet to monitor up to an additional 3 lines. Highly recommend more blinking lights.

Title	micro-circuit-ATMEGA64M1.SchDoc		
Size	Number		Revision
A4	PCBS-COMMON		1.1
Date:	9/3/2019	Sheet *	of *
File:	C:\Users\..\micro-circuit-ATMEGA64M1.SchDoc	Drawn By:	Dylan Vogel


S2
S1
RST
RUN<->PGM
J1
TX
RX
PGM
J2
R13
R16
R17
R15
C7
R11
R14
R6
R9
U4
C4
RX
TX
RST
U1_FLASH1
U1_FLASH2
U1_FLASH3
R12
R29
R28
U5
U7
U8
C9
C10
C12
C11
L1
REL_B
REL_A
ANT_WARN
U2
R3
C3
R4
Y1
U3
R26
R27
J3
CANH CANL SCL SDA TX RX GND SCK MOSI MISO BAT 3V3 3V3 GND GND

Board S