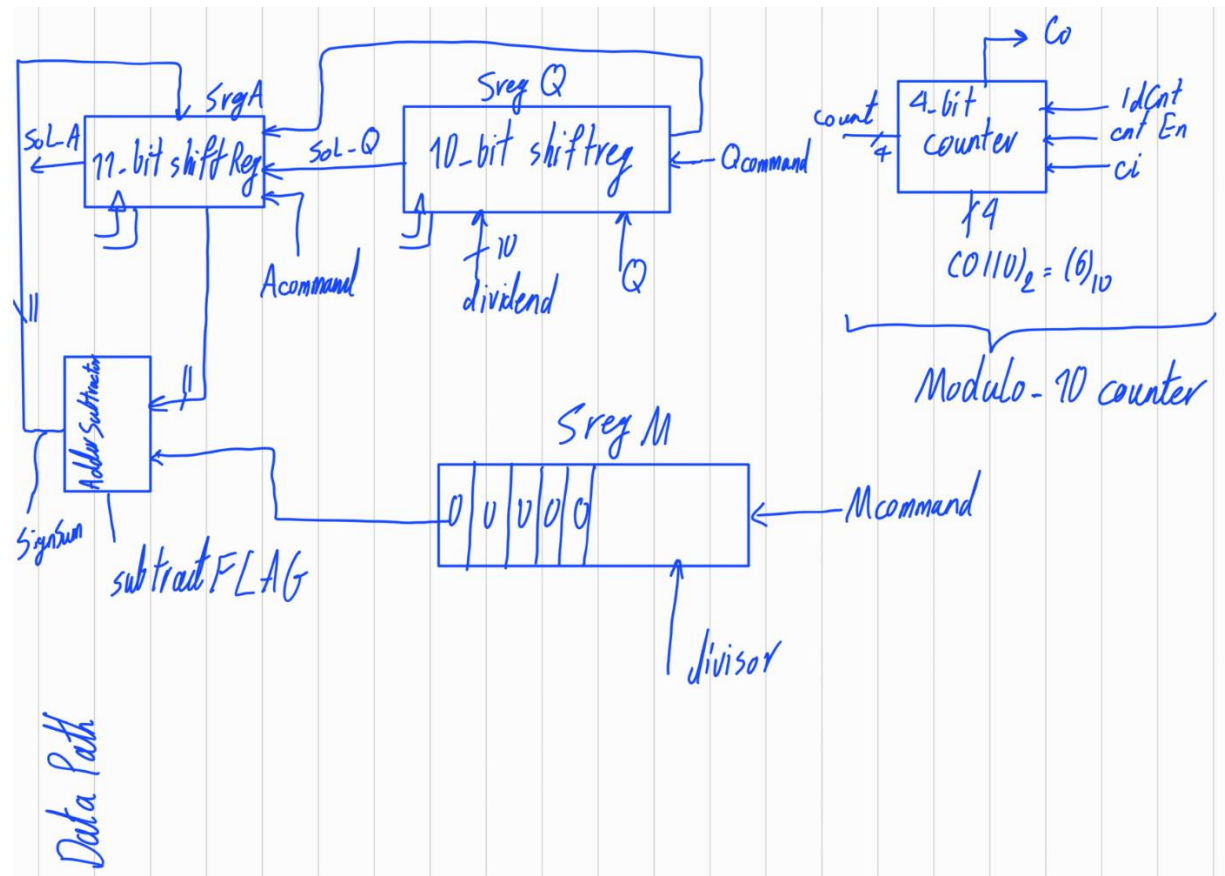




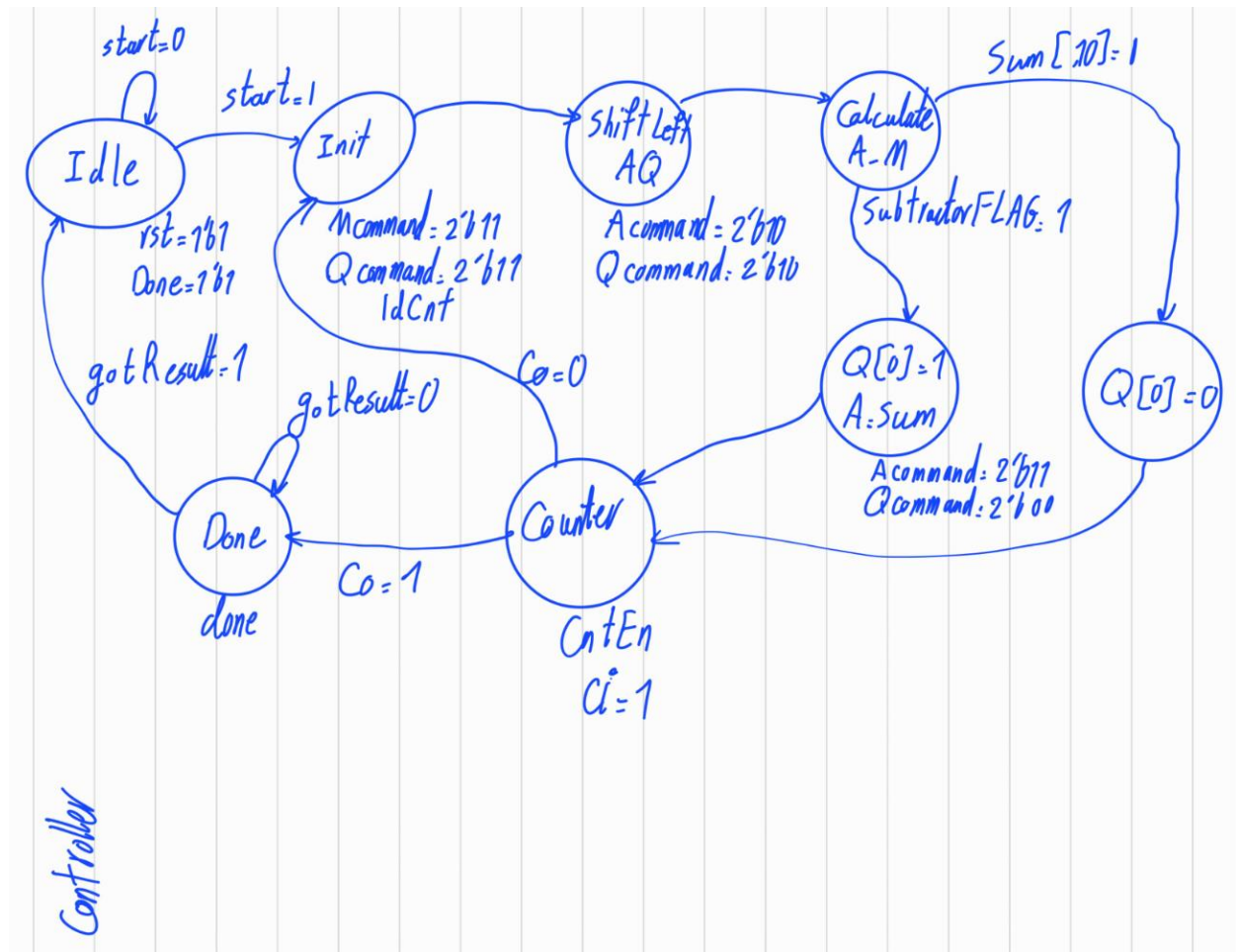
University of Tehran
Electrical and Computer Engineering Department
Computer Architecture
Computer Assignment #1

Name	Danial Saeedi Mohammad Ghare Hasanloo
Student No	810198571 810198461
Date	November 07, 2021

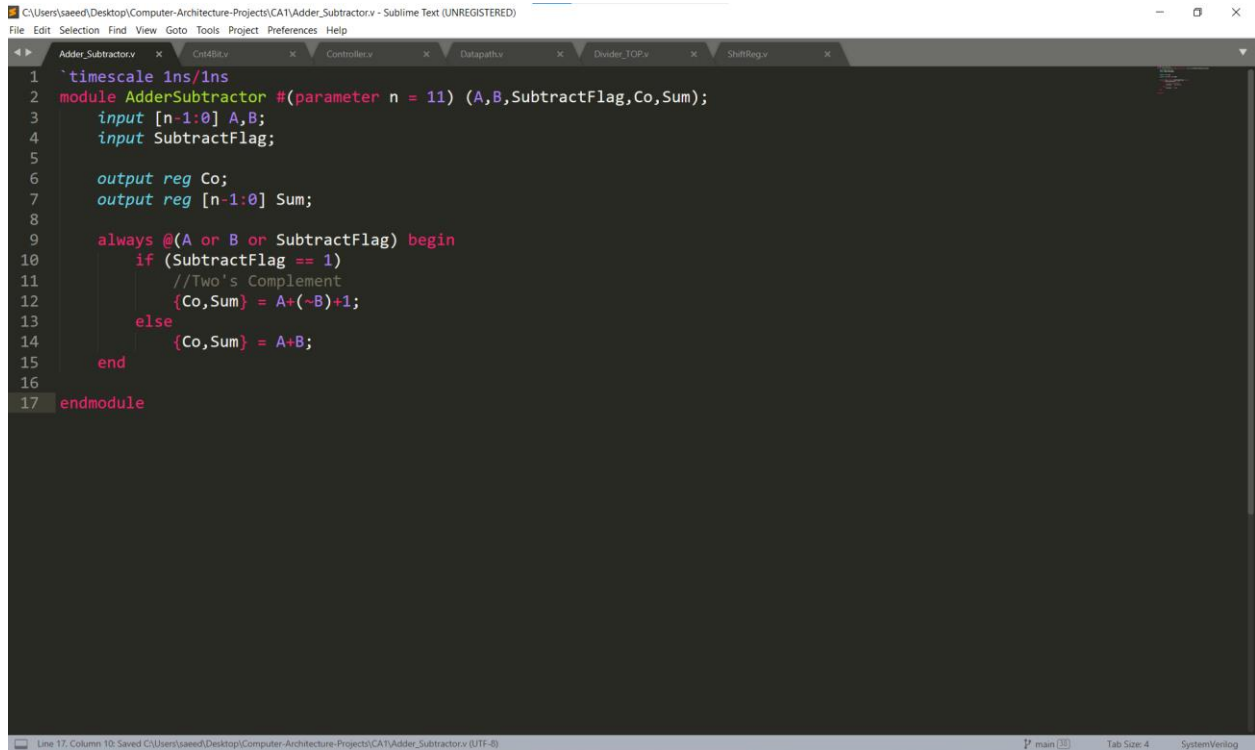
1. Datapath



2. Control Unit



Adder / Subtractor Module



The screenshot shows a Sublime Text editor window with the following Verilog code:

```
1 `timescale 1ns/1ns
2 module AdderSubtractor #(parameter n = 11) (A,B,SubtractFlag,Co,Sum);
3     input [n-1:0] A,B;
4     input SubtractFlag;
5
6     output reg Co;
7     output reg [n-1:0] Sum;
8
9     always @(A or B or SubtractFlag) begin
10         if (SubtractFlag == 1)
11             //Two's Complement
12             {Co,Sum} = A+(~B)+1;
13         else
14             {Co,Sum} = A+B;
15         end
16
17 endmodule
```

The editor interface includes a menu bar (File, Edit, Selection, Find, View, Goto, Tools, Project, Preferences, Help), a tab bar with several open files (Adder_Subtractor.v, Cnt4Bit.v, Controller.v, Datapath.v, Divider_TOP.v, ShiftReg.v), and a status bar at the bottom indicating the current line and column (Line 17, Column 10) and the file path.

Modulo-10 Counter

```

1  `timescale 1ns/1ns
2  module upcnt4(input [3:0] PI, input clk,rst,cntEn,ld,Ci,output reg[3:0] P0, output Co);
3      always @(posedge clk, posedge rst) begin
4          if(rst)
5              P0 <= 4'b0;
6          else begin
7              if (ld)
8                  P0 <= PI;
9              else if(cntEn)
10                 P0 <= Ci ? (P0 + 1) : P0;
11          end
12      end
13      assign Co = (cntEn) ? &{P0,Ci} : 1'b0;
14  endmodule

```

Universal Shift Register

```
CAUsers\saee\Desktop\Computer-Architecture-Projects\CAT\ShiftReg.v - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

1 `timescale 1ns/1ns
2 module ShiftReg #(parameter n = 11) (input [n-1:0] PI, input clk, rst, SiR, input [1:0] m, output SoL, output reg [n-1:0] PO)
3     assign SoL = PO[n-1];
4
5     always @(posedge clk, posedge rst) begin
6         if(rst)
7             PO <= 0;
8         else
9             case(m)
10                2'b00 : PO <= PO;
11                2'b01 : PO[0] <= SiR;
12                2'b10 : PO <= {PO[n-2:0], SiR};
13                2'b11 : PO <= PI;
14            endcase
15        end
16    endmodule

Line 16, Column 10      77 main  Tab Size: 4  SystemVerilog
```

Data Path Module

Quotient is stored at Q and the remainder is stored at A.

```
C:\Users\saeed\Desktop\Computer-Architecture-Projects\CAT1\DataPath.v - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

DataPath.v x Divider_TOP.v x Testbench.v x
1 `timescale 1ns/1ns
2 module DataPath(clk,rst, QCommand, ACommand, MCommand,subtractFlag,cntEn,ldCnt,Ci,SiR_Q, dividend, divisor, out_Q, out_A, out_M,Co,SignSum);
3     parameter n = 10;
4     input clk,rst;
5     input [1:0] QCommand,ACommand, MCommand;
6     input subtractFlag;
7     input cntEn,ldCnt,Ci,SiR_Q;
8     input [n-1:0] dividend;
9     input [4:0] divisor;
10
11     output [9:0] out_Q;
12     output [10:0] out_A;
13     output [10:0] out_M;
14     output Co;
15     output SignSum;
16
17     wire Sol_Q;
18     wire Sol_A;
19     wire [10:0] sum;
20
21     assign SignSum = sum[10];
22
23     // Register Q
24     ShiftReg #(.n(n)) sregQ (.clk(clk), .rst(rst),.PI(dividend),.SiR(SiR_Q),.m(QCommand),.Sol(Sol_Q), .PO(out_Q));
25
26     // Register A
27     ShiftReg #(.n(11)) sregA (.clk(clk), .rst(rst),.PI(sum),.SiR(Sol_Q),.m(ACommand),.Sol(Sol_A), .PO(out_A));
28
29     // Register M
30     wire Sol_M;
31     ShiftReg #(.n(11)) sregM (.clk(clk), .rst(rst),.PI({6'b0,divisor}),.SiR(0),.m(MCommand),.Sol(Sol_M), .PO(out_M));
32
33     // Adder/Subtractor
34     wire Co2;
35     AdderSubtractor #(.n(11)) adder_subtractor (.A(out_A),.B(out_M),.SubtractFlag(subtractFlag),
36     .Co(Co2), .Sum(sum));
37
38     // Counter
39     wire [3:0] count;
40     upcnt4 M10C (.PI(4'b0110), .clk(clk), .rst(rst), .cntEn(cntEn), .ld(ldCnt), .Ci(Ci),.PO(count), .Co(Co));
41
42 endmodule
43

Line 10, Column 1 main Tab Size: 4 SystemVerilog
```

Control Unit Module

C:\Users\saee\Desktop\Computer-Architecture-Projects\CAT\Controler.v - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

```
1 `timescale 1ns/1ns
2 module Controller(clk,rst,start,getResult,Co,SignSum, SiR_Q, QCommand, ACommand, MCommand,subtractFlag,cntEn,ldCnt,Ci, done);
3     input clk,rst,start,getResult,Co,SignSum;
4
5     output reg [1:0] QCommand,ACommand, MCommand;
6     output reg subtractFlag;
7     output reg cntEn,ldCnt,Ci, SiR_Q, done;
8
9     reg [2:0] ps;
10    reg [2:0] ns;
11    parameter [2:0] Idle = 3'b000;
12    parameter [2:0] Init = 3'b001;
13    parameter [2:0] Shifleft_AQ = 3'b010;
14    parameter [2:0] CalculateA_M = 3'b011;
15    parameter [2:0] PositiveA_M = 3'b100;
16    parameter [2:0] NegativeA_M = 3'b101;
17    parameter [2:0] Counter = 3'b110;
18    parameter [2:0] Done = 3'b111;
19
20    always @(posedge clk, posedge rst) begin
21        if (rst)
22            ps <= Idle;
23        else
24            ps <= ns;
25    end
26
27    always @(ps or start or Co or SignSum)
28    begin
29        case(ps)
30            Idle: ns = start ? Init: Idle;
31            Init: ns = Shifleft_AQ;
32            Shifleft_AQ: ns = CalculateA_M;
33            CalculateA_M: ns = SignSum ? NegativeA_M: PositiveA_M;
34            NegativeA_M: ns = Counter;
35            PositiveA_M: ns = Counter;
36            Counter: ns = Co ? Done: Shifleft_AQ;
37            Done: ns = getResult ? Idle : Done;
38        endcase
39    end
40
41    always @(ps)
42    begin
43        QCommand = 2'b00;
```

```
40
41    always @(ps)
42    begin
43        QCommand = 2'b00;
44        ACommand = 2'b00;
45        MCommand = 2'b00;
46        (subtractFlag,cntEn,ldCnt,Ci,SiR_Q,done) = 6'b000000;
47        case (ps)
48            Idle: done = 1'b1;
49            Init: begin
50                MCommand = 2'b11;
51                QCommand = 2'b11;
52                ldCnt = 1'b1;
53            end
54            Shifleft_AQ: begin
55                QCommand = 2'b10;
56                ACommand = 2'b10;
57            end
58            CalculateA_M: subtractFlag = 1'b1;
59            NegativeA_M: begin
60                SiR_Q = 0;
61                QCommand = 2'b01;
62                subtractFlag = 1'b1;
63            end
64            PositiveA_M: begin
65                SiR_Q = 1;
66                QCommand = 2'b01;
67                ACommand = 2'b11;
68                subtractFlag = 1'b1;
69            end
70            Counter: begin
71                (cntEn, Ci) = 2'b11;
72                subtractFlag = 1'b1;
73            end
74            Done: begin
75                (cntEn, Ci) = 2'b11;
76                subtractFlag = 1'b1;
77                done = 1'b1;
78            end
79        endcase
80    end
81 endmodule
```

Line 22, Column 24

main

Tab Size: 4

SystemVerilog

Top Module

```
C:\Users\saeeed\Desktop\Computer-Architecture-Projects\CAT1\Divider_TOP.v - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

1 `timescale 1ns/1ns
2 module RestoringDivision(clk,rst,start,getResult,dividend, divisor, Q, M, A, done, divByZero);
3     input clk,rst,start,getResult;
4     input [9:0] dividend;
5     input [4:0] divisor;
6
7     output [9:0] Q;
8     output [10:0] A;
9     output [10:0] M;
10    output done;
11
12    output divByZero;
13
14    assign divByZero = (divisor == 5'b0) ? 1 : 0;
15
16    // Wires
17    wire [1:0] QCommand, ACommand, MCommand;
18    wire subtractFlag;
19    wire cntEn, ldCnt, Ci, SiR_Q, Co, SignSum;
20    // Data Path
21    DataPath dp(clk,rst, QCommand, ACommand, MCommand,subtractFlag,cntEn,ldCnt,Ci,SiR_Q, dividend, divisor, Q, A, M,Co,SignSum);
22
23    // Control Unit
24    Controller cu(clk,rst,start,getResult,Co,SignSum, SiR_Q, QCommand, ACommand, MCommand,subtractFlag,cntEn,ldCnt,Ci, done);
25 endmodule

Line 18, Column 23  main (2) Tab Size: 4 SystemVerilog
```

Testbench

```

CAUsers\saad\Desktop\Computer-Architecture-Projects\CAT\Testbench.v - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

Testbench.v
1 `timescale 1ns/1ns
2 module Testbench();
3     parameter n = 10;
4     reg [9:0] dividend;
5     reg [4:0] divisor;
6
7     reg rst, start, gotResult, clk;
8
9     wire [9:0] Q;
10    wire [10:0] A;
11    wire [10:0] M;
12    wire done;
13
14    RestoringDivision RD(clk,rst,start,gotResult,dividend, divisor, Q, M, A, done);
15
16    initial begin
17        start = 1'b0;
18        rst = 1'b0;
19        clk = 1'b0;
20        gotResult = 1'b0;
21        #13 rst = 1'b1;
22        #20 rst = 1'b0;
23        #13 start = 1'b1;dividend = 10'b1001000011; divisor = 5'b011111;
24        #1000 start = 1'b0; gotResult = 1'b1;
25        #200 rst = 1'b1; gotResult = 1'b0;
26        #20 rst = 1'b0; start = 1'b1; dividend = 10'b0001000011; divisor = 5'b00101;
27        #1000 $stop;
28    end
29
30    always
31    begin
32        #10 clk = ~clk;
33    end

```

Figure 1 Testbench.v

